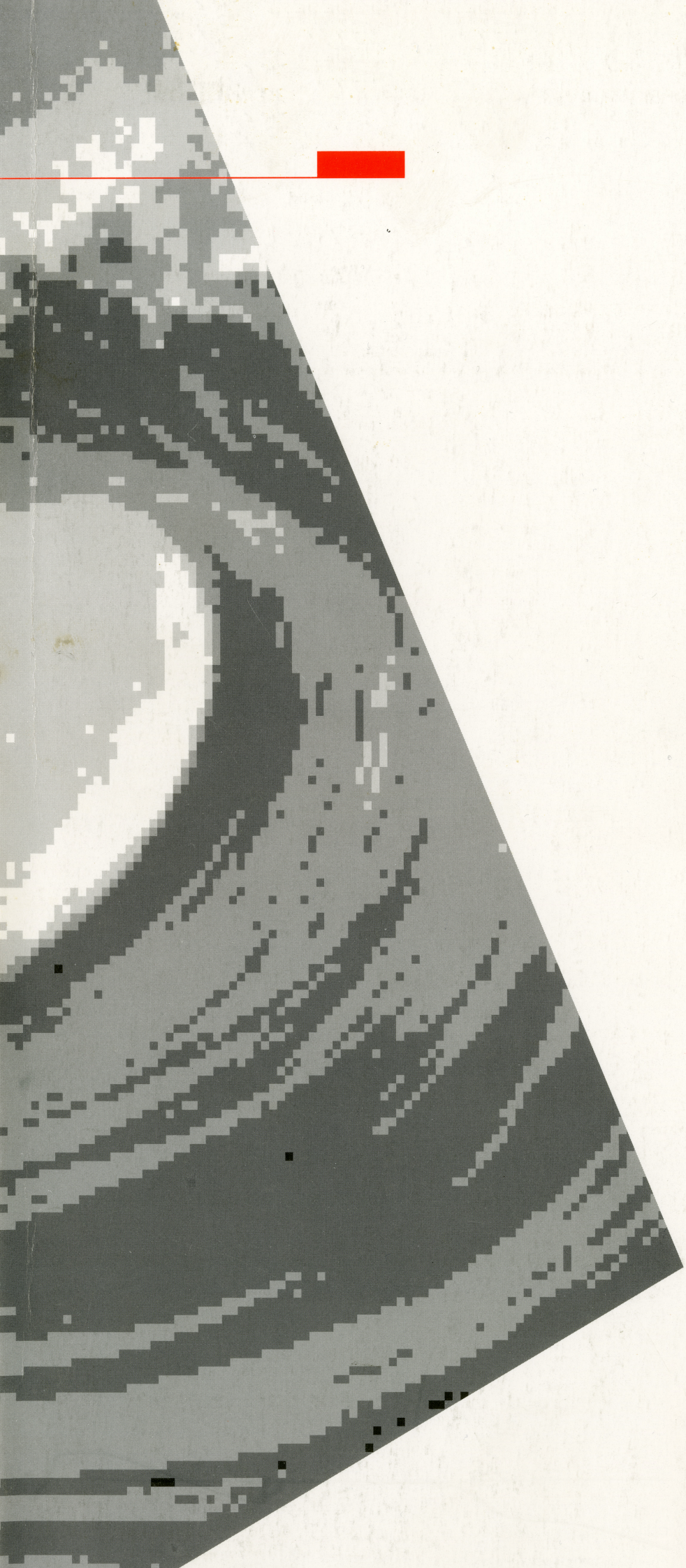


RE 201
Dual Channel Audio Analyzer
Service Manual

Volume III

LIST OF FIGURES

Section **Page**

1 General Information

Fig. 1.1 Interior Top View 7
Fig. 1.2 Mounting Analog Options 9

2 Principles of Operation

Fig. 2.1 RE201 Simplified Block Diagram 2
Fig. 2.2 Spectra for Different Windows 6
Fig. 2.3 ZOOM Spectrum 7
Fig. 2.4 Measurement Setup Block Diagram 14
Fig. 2.5 NORMAL Setup 15
Fig. 2.6 Peak Measurements 16
Fig. 2.7 Phase Measurements 17
Fig. 2.8 RMS75 Measurements 18
Fig. 2.9 THD or IM Using Filter Option 18
Fig. 2.10 SINAD Measurements 19
Fig. 2.11 Wow & Flutter Measurements 20

3 Circuit Descriptions

Fig. 3.1.1 Interior Bottom View 3

Fig. 3.2.1 Analog Section Board Positioning 6
Fig. 3.2.2 Static CPU Block Diagram 9
Fig. 3.2.3 TMS 9995 Memory Timing 11
Fig. 3.2.4 TMS 9995 CRU Interface Timing 13
Fig. 3.2.5 Static CPU Component Layout 16
Fig. 3.2.6 Analog Frontend Block Diagram 18
Fig. 3.2.7 Analog Frontend Component Layout 21
Fig. 3.2.8 Phase Detector Block Diagram 24
Fig. 3.2.9 Analog Motherboard Component Layout 25
Fig. 3.2.10 Linear Power Supply Component Layout ... 26
Fig. 3.2.11 I/O & Memory Bus Interface Block Diagram 28
Fig. 3.2.12 Memory Bus Interface Timing 29
Fig. 3.2.13 GPIO Timing 30
Fig. 3.2.14 BNO DC Connector 31
Fig. 3.2.15 I/O & Memory Bus Interface Component Layout 32
Fig. 3.2.16 Keyboard Block Diagram 34

Fig. 3.3.1 Digital Section Board Positioning 36
Fig. 3.3.2 Main CPU Block Diagram 39
Fig. 3.3.3 Dot Character Font 42
Fig. 3.3.4 Graphics Character 43
Fig. 3.3.5 Main CPU Component Layout 44
Fig. 3.3.6 Arithmetical Unit Block Diagram 49

Fig. 3.3.7 Rectangular Window 52
Fig. 3.3.8 Sine Window 52
Fig. 3.3.9 FTBH Window 52
Fig. 3.3.10 Sample Collection Cycle 53
Fig. 3.3.11 Butterfly 54
Fig. 3.3.12 Butterfly Operation Timing 55
Fig. 3.3.13 RMS Unit 56
Fig. 3.3.14 RMS Unit Operation 57
Fig. 3.3.15 SC and S/H Signal Timing 58
Fig. 3.3.16 Digital Motherboard Block Diagram 61
Fig. 3.3.17 Digital Motherboard Component Layout ... 62
Fig. 3.3.18 Switch Mode Power Supply Block Diagram . 64
Fig. 3.3.19 Generation of Synchronization Pulses ... 65
Fig. 3.3.20 Switch Mode Power Supply Component Layout 66

Fig. 3.4.1 CRT Section Block Diagram 68
Fig. 3.4.2 CRT Driver Jumpers 70

4 Maintenance

Fig. 4.2.1 Phase Measurement Test Set-up 6

Fig. 4.3.1 Top Plate Securing Screws 12
Fig. 4.3.2 Right Side Structure 14
Fig. 4.3.3 Analog Frontend on Extender Board 16
Fig. 4.3.4 Removing the Fan 17
Fig. 4.3.5 Analog Motherboard Connectors and Screws 18
Fig. 4.3.6 I/O & Memory Bus Interface Connectors and Stands 20
Fig. 4.3.7 Linear Power Supply Connectors and Screws 21
Fig. 4.3.8 Keyboard Connector and Screws 22
Fig. 4.3.9 Digital Section Shielding Boxes Screws . 24
Fig. 4.3.10 Digital Motherboard Connectors and Screws 25
Fig. 4.3.11 CRT Section Screws and Adjustment Holes 27
Fig. 4.3.12 CRT Section Dismantled 28
Fig. 4.3.13 Handling the Tube 30

Fig. 4.4.1 Interior CRT Section View 41

5 Troubleshooting

6 Parts Lists and Schematic Diagrams

4.2.4 Phase Measurements 6
4.2.5 DC Measurements 6
4.2.6 Keyboard 7
4.2.7 Rear Panel Outputs 8
4.2.8 IEEE488 Bus Interface 9
4.3 Dismantling 11
4.3.1 Removing Outer Covers and Panels ... 11
4.3.2 Analog Section 13
4.3.3 Digital Section 19
4.3.4 CRT Section 26
4.4 Adjustment 31
4.4.1 Linear Power Supply 901-406 32
4.4.2 Switch Mode Power Supply 901-022 ... 33
4.4.3 Analog Frontend 901-421 33
4.4.4 Phase Detector - Analog Motherboard 37
4.4.5 DC Inputs 38
4.4.6 CRT Section..... 39

5 Troubleshooting

5.1 Power-up Errors 1
5.2 Selftest Errors 2
5.2.1 Analog Section Selftest 2
5.2.2 Digital Section Selftest 6
5.3 Errors Observed During Operation 7

6 Parts Lists and Schematic Diagrams

6.1 Parts Lists 1

TABLE OF CONTENTS

Section Page

1 General Information

1.1 Introduction 1
1.2 Installation 3
1.2.1 RE201 Installation 3
1.2.2 Installation of Analog Options 6
1.3 Equipment and Accessories 11
1.3.1 Equipment Supplied with the RE201 .. 11
1.3.2 Options 12
1.3.3 Accessories 15
1.4 Specifications 16

2 Principles of Operation

2.1 Principles of Operation 1
2.2 The Fast Fourier Transform 3
2.3 Microprocessors 7
2.4 Start of Measurements, Sequences and Setups . 9
2.5 Actual Measurement Setups 12

3 Circuit Descriptions

3.1 Interconnections 1
3.2 Analog Section 4
3.2.1 Analog Section Configuration 4
3.2.2 Static CPU 901-788 7
3.2.3 Analog Frontend 901-421 17
3.2.4 Analog Motherboard 901-405 23
3.2.5 Linear Power Supply 901-406 26
3.2.6 I/O & Memory Bus Interface 901-407 . 27
3.2.7 Keyboard 901-410 33
3.3 Digital Section 35
3.3.1 Main CPU 901-789 38
3.3.2 Arithmetical Unit 901-527 48
3.3.3 Digital Motherboard 901-790 60
3.3.4 Switch Mode Power Supply 63
3.4 CRT Section 67
3.4.1 CRT Driver 901-417 67
3.4.2 Tube Unit 901-414 71

4 Maintenance

4.1 Recommended Test Equipment 1
4.2 Performance Tests 2
4.2.1 Selftest 3
4.2.2 Test of Analog Frontend 3
4.2.3 Frequency Accuracy 5

1 GENERAL INFORMATION

The purpose of the present Technical Manual for the RE201 Dual Channel Audio Analyzer is to provide all information necessary to:

* understand the principles of operation for the RE201
* carry out preventive maintenance and regular adjustments
* perform troubleshooting to board level

In order to fulfill these objectives, the Technical Manual presents detailed descriptions of electrical and mechanical features of the RE201 Basic Unit; separate technical manuals are supplied for each option. All operating instructions and other information concerning operational aspects can be found in the RE201 Operation Manual.

1.1 Introduction

The RE201 Dual Channel Audio Analyzer is a modular, combined analog and digital test instrument, designed for verification of performance of sound reproduction equipment such as radios, record players, tape recorders, compact disc players and audio matrices.

The instrument provides a wide range of measuring capabilities:

* Level - RMS, DC, peak, selective, average
* Frequency, absolute and relative
* Phase
* Harmonic Distortion
* Intermodulation Distortion
* Difference Frequency Distortion
* Transient Intermodulation Distortion
* Crosstalk

This comprehensive range of features has been incorporated in one single instrument to provide the convenience of avoiding the usual heap of individual instruments which often makes the test bench crowded and disorganized. Furthermore, more reliable and reproducible test results are ensured.

To enhance the measurement capabilities of the RE201 further, a wide range of accessories (options) is available. These options are configured as PC boards which are easily installed in the RE201. When an option is mounted, the capacity of the option is automatically available without any need for system reconfiguration. For further information regarding the options, please refer to section 1.3.2.

Organization of the Manual

The contents of this manual are divided into six main sections. The scope and contents of each of these are as follows:

Section 1, General Information

- provides a general overview of the manual, and comprises general information such as installation instructions, specifications and code numbers for equipment and accessories, including options.

Section 2, Principles of Operation

- explains the principles of operation for the RE201, without any details concerning actual circuit implementations. Description of the principles for the spectral analysis capabilities, the Fast Fourier Transform, is included.

Section 3, Circuit Descriptions

- presents detailed information about the actual circuit implementations in order to enable a thorough understanding of the instrument and to provide an aid in pinpointing faulty PC boards.

Section 4, Maintenance

- provides directions for dismantling and adjustments

Section 5, Troubleshooting

- provides instructions and hints to facilitate fault diagnosis to board level in conjunction with the contents of sections 2 and 3.

Section 6, Parts Lists and Schematic Diagrams

- comprises parts lists for all PC boards with reference designations, component values and RE code numbers, together with schematic diagrams including component layout drawings.

Besides these sections, constituting the Technical Manual for the Basic Unit without any options, room is allocated for the technical descriptions for the various options available. These are alphabetically ordered as follows:

* Audio Generator	901-500
* External Keyboard, RE905	906-032
* Filter Option	901-525
* Weighting Filters	901-526
* Wow & Flutter	901-456

For options mounted in the RE201 upon delivery from the factory, the technical manuals for the pertinent options have been inserted in the Technical Manual binder. For options delivered separately, the manual sections supplied with the option must be inserted in the binder.

The individual option manuals are self-contained, each comprising the same sections as the manual for the Basic Unit:

* General Information
* Principles of Operation
* Circuit Descriptions
* Maintenance
* Troubleshooting
* Parts list and schematic diagram

1.2 Installation

This section comprises two subsections:

* Installation of the RE201
* Installation of the analog options in the RE201

The latter subsection is a general installation guide for options mounted in the Analog Section of the RE201 (Filter Option, Weighting Filters and Wow & Flutter) and is included in this manual, because the installation procedure depends on the entire option configuration.

1.2.1 RE201 Installation

When unpacking the instrument, the accessories and the packing material should be inspected for any damage. If the RE201 and/or the accessories should be damaged, please notify the carrier and your local RE INSTRUMENTS representative or the factory. The packing material should be retained for inspection by the carrier in case of complaint. Refer to section 1.3.1 for a description of equipment and accessories.

If the RE201 is to be rack-mounted, the installation instructions supplied with the rack mounting kit should be followed.

Power Requirements

The RE201 will operate on either 115 V or 220 V AC line supplies. The required line voltage is selected by a slide switch on the rear panel.

In order to change the line voltage the locking plate must be removed by unscrewing the two securing screws. Switch the line switch to the required line voltage and replace the locking plate. Install the correct line fuse for the selected power source using one of the bayonet heads. For more information, refer to the Installation Guide delivered with the instrument.

Nominal AC voltage	Line fuse
115 V	2 A (slow blow)
220 V	1 A (slow blow)

***** Caution *****

Always make certain that the line voltage selector switch is set to the correct position and that a fuse having the correct rating is installed in the fuse holder before connecting the RE201 to any AC power source.

Power Application

The following procedure should be used to apply power:

1. Check that the line voltage selector located on the rear panel is set to the correct position

2. Check that the line fuse located on the rear panel has the proper value (shown close to the fuse itself)

3. Connect the power cord supplied with the instrument between the power connector on the rear panel of the instrument and the AC power receptacle.

   ***** Note *****

   The three-wire power cord will, when connected to an appropriate AC power outlet, ground the instrument structure. If the RE201 is connected to an AC outlet without a ground connection, the ground jack at the rear panel must be used to ground the instrument.

4. Set the power switch to ON.

```
*******************************
       *** RE201 TEST ***

CRT-RAM          [901-789] PASSED
EPROM            [901-789] PASSED
UARTS            [901-790] PASSED
EPROM            [901-789] PASSED
RAM              [901-789] PASSED
RAM              [901-789] PASSED
EPROM            [901-527] PASSED
RAM              [901-527] PASSED
BUTTERFLY UNIT   [901-527] PASSED
ZOOM             [901-393] PASSED
ANALOG SECTION   [901-788] PASSED

*******************************
```

This screen displays the results obtained during the power-up SELFTEST (the code Nos. in brackets indicate the board being tested). If this test is successful another test display will appear:

```
       *** RE201 ***

SOFTWARE REVISIONS       a.a & b.b

OPTION(S)          SOFTWARE REVISION
---------          -----------------

AUDIO GENERATOR          c.c
FILTER OPTION            c.c
WEIGHTING FILTERS        c.c
WOW & FLUTTER            N/A
```

This display presents information of:

* Software revision installed in the Digital Section ('a.a')
* Software revision installed in the Analog Section ('b.b')
* Options installed, as applicable
* Software revisions installed on individual options ('c.c') - for options not holding program information, 'N/A' ("Not Applicable") is displayed.

Battery Backup

In the absence of line power, a battery power supply will be active to retain valid data in the RAM. If the line voltage disappears, a power fail protection circuit isolates the RAM and the battery will take over.

If the RE201 has to be stored for more than two months without power on, it is recommended that the battery be isolated from the RAM by means of the jumper K4 on the 901-788 Static CPU. The Static CPU Board is located in slot 5 in the PCB compartment to the right of the CRT section of the instrument. K4 isolates the battery when placed in position 2-3. The location of K4 is shown in fig. 3.2.5 in section 3.

The contents of the RAM will be lost during such periods of storage without backup.

1.2.2 Installation of Analog Options

The present installation guide describes the installation of the analog options:

* Filter Option 901-525
* Weighting Filters 901-526
* Wow & Flutter 901-456

which are installed in the print magazine of the Analog Section of the RE201. The Analog Section is positioned to the right of the CRT as shown in fig. 1.1.

It is strongly recommended, that the entire installation guide is read through thoroughly before installation is initiated in order to prevent faulty operation and possible damage due to incorrect installation.

Initial Dismantling of the RE201

As the Analog Section, into which the options in question are installed, is not shielded, it is only necessary to remove the top plate of the RE201 and the clamp bar securing the PCB's in the print magazine to gain access to this area.

* Remove the screws securing the top plate using a Pozidrive No. 1 screwdriver (the location of the screws is shown in fig. 4.3.1 of the Dismantling Section in this manual (Section 4)).

* Remove the top plate by sliding it backwards approx. 2 cm until it disengages along the front and the rear edges. The plate may then be lifted and removed.

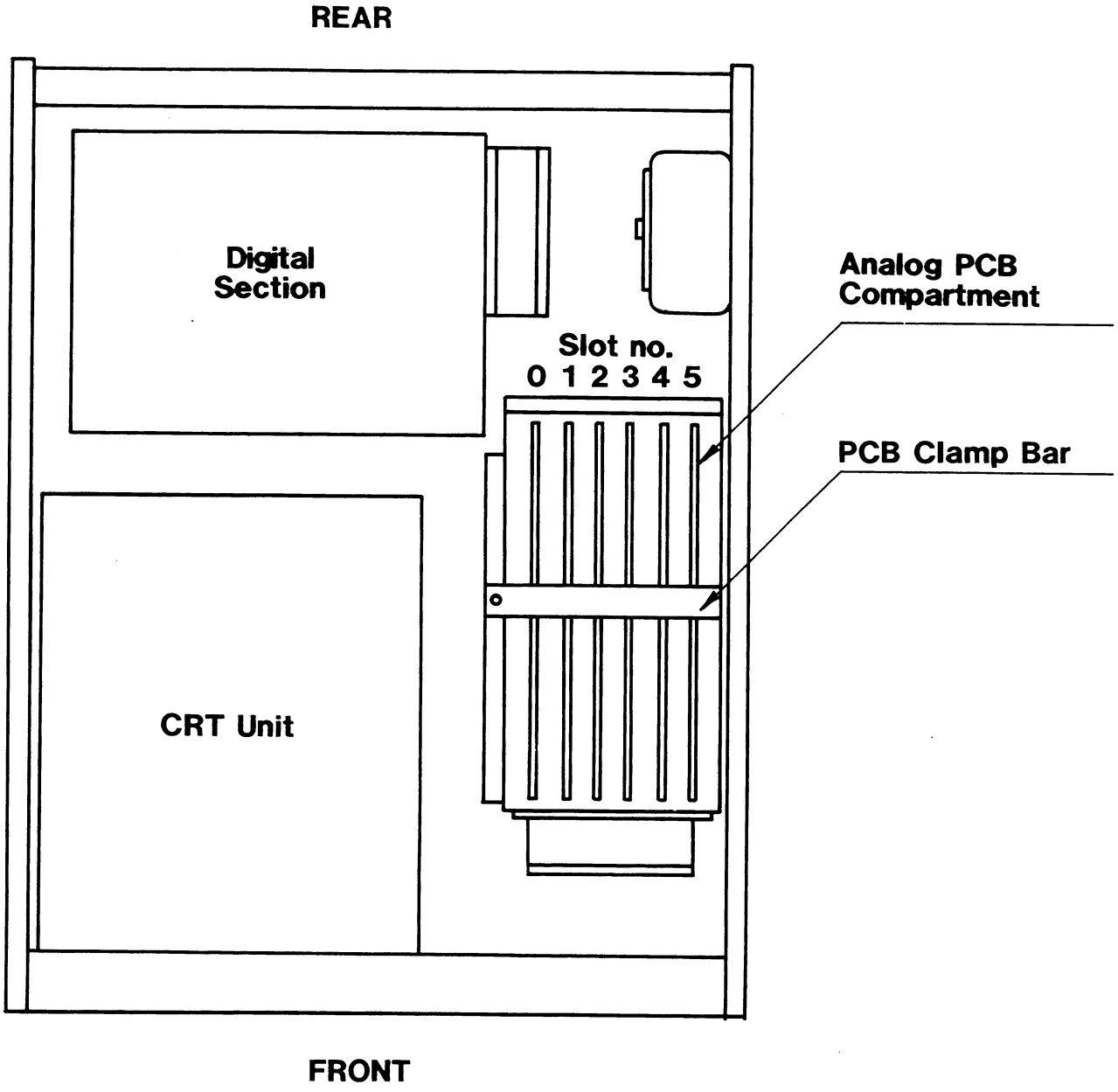


Fig. 1.1 - Interior Top View

* Remove the clamp bar securing the PCB's (refer to fig. 1.1).

The print magazine comprises six slots. No. 0 is the leftmost (viewed from the front of the RE201), and No. 5 is the rightmost. Four slots are available for analog options, as slots No. 0 and No. 5 are used for the Analog Frontend (901-421) and the Static CPU (901-788), respectively. These two boards are connected by a flat cable connecting to J4 on the Analog Frontend and to J2 on the Static CPU. The flat cable has to be disconnected from the Static CPU when options are installed or removed.

Board Positioning

The position of options should be in accordance with the general scheme outlined in table 1.1, the lowest relative position number being closest to the Analog Frontend.

Relative Position	Option
1	Filter Option
2	Weighting Filters
3	Wow & Flutter

Table 1.1 - Relative Positioning

The relative positioning should always be used; if one or more of the options are not installed, all options with a higher relative position number are moved one slot towards the Analog Frontend ("queuing up").

The Audio Generator is not included in the scheme, as it is always mounted with the Analog Board (901-498) in slot No. 3 and the Digital Board (901-499) in slot No. 4 (next to the Static CPU). Thus, if the Audio Generator is installed, only two more analog options can be installed (in slots No. 1 and 2). For information about installation of the Audio Generator, please refer to Technical Manual for this option.

Mounting

Fig. 1.2 depicts the mounting of the four options mentioned above, i.e. excluding the Audio Generator.

For installation of options, the following must be observed:

* Prior to insertion of the options PCB's, disconnect the flat cable connecting the Analog Frontend and the Static CPU board.

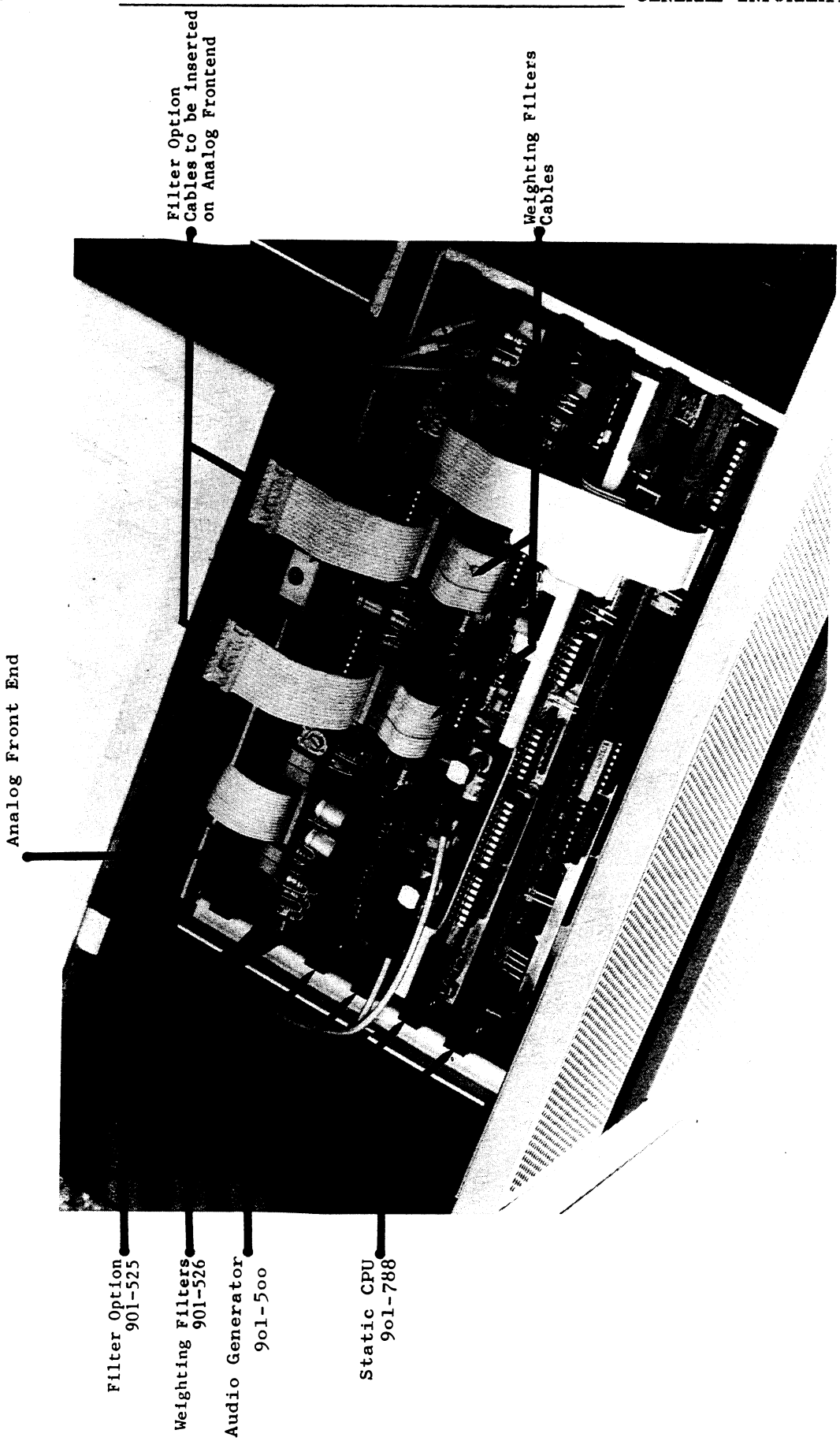


Fig. 1.2 - Mounting Analog Options

* Options are mounted with the component side of the PCB facing towards the right side structure.

* If neither the Filter nor Weighting Filters Option has been previously installed, the blue plug mounted at J2 of the Analog Frontend must be removed, J2 is the central connector at the top edge of the board, just beside the clamp bar. In case the above mentioned options are dismounted later on, the plug must be reinstalled.

* Flat cables for routing of analog signals between the individual options are most easily installed when the receiving PCB is not fully inserted in the print magazine during attachment of the flat cable connector - refer to fig. 1.2, showing the Filter Option in this position, following insertion of the cables from the Weighting Filters Option.

* The individual flat cables, fixed at one end to the respective options, must be connected to the nearest sockets at the upper edge of the PCB positioned one slot closer to the Analog Frontend, ultimately to the sockets on the Analog Frontend.

* Upon completion of the installation, the flat cable connection between the Static CPU and the Analog Frontend must be reestablished at the Static CPU, J2. It may be convenient to extract the Static CPU board a little for insertion of the flat cable.

This procedure should be followed irrespective of the actual subset of options to be installed.

Reassembling

When all options involved are properly installed, reassemble the RE201:

* Mount the PCB clamp bar

* Put the top plate in place by pushing the front and rear edges downwards simultaneously and slide the plate forwards until fully engaged

* Fasten the screws to secure the top plate

Selftest

Turn on the RE201 and watch the display during the initial selftest. If all subassemblies pass the test, the installed software revisions

and options will be displayed. In the options list, all options installed must appear. For option boards holding program information, i.e. Audio Generator, Filter Option and Weighting Filters, the software revision installed is displayed. For the (Wow & Flutter option), a 'N/A' (Not Applicable) is displayed, indicating no software is included on this board.

For selftest extents and performance test procedures, please refer to the Technical Manual for the options in question.

1.3 Equipment and Accessories

This section is subdivided in three:

* Equipment supplied with the RE201
* Options
* Accessories

1.3.1 Equipment Supplied with the RE201

The equipment supplied with the instrument from the factory is listed in table 1.2.

Description	Type	Code No.
Dual Channel Audio Analyzer	RE201	390-979
Line Cord	220 V	615-303
Line Cord	110 V	615-403
Fuse 1 Amp, slow blow (2 pieces)	220 V	450-020
Fuse 2 Amp, slow blow (2 pieces)	110 V	450-123
Fuse 4 Amp, slow blow (2 pieces)	220 V	450-028
Fuse 4 Amp, slow blow (2 pieces)	110 V	450-130
Bayonet Head 5 x 20 mm (2 pieces)	220 V	460-025
Bayonet Head 6.3 x 32 mm (2 pieces)	110 V	460-026
Technical Manual		983-297
Operation Manual		983-298
Installation Instructions		983-270

Table 1.2 - Equipment supplied

1.3.2 Options

Table 1.3 lists the different options available. Please note that operating instructions for all options are included in the RE201 Operation Manual.

Description	Code No.	Technical Manual No.
Wow & Flutter	901-456	983-258
Audio Generator	901-500	983-229
Filter Option	901-525	983-259
Weighting Filters	901-526	983-260
FSK	901-777	983-290

Table 1.3 - Options Code No.

The following subsections provide a brief description of each of the various options.

Audio Generator Option

This digitally based high quality programmable AF generator makes it possible within the RE201 to generate the required test signals and to perform the analysis on the reproduced signal. The unit is based on a principle which allows generation of multitone signals (up to 8 components) as well as single frequencies. Thus, it provides single tones for THD measurement, two-tone signals for intermodulation and difference frequency distortion measurements and multitone signals for fast frequency response measurements. Further, standard TIM (Transient Intermodulation) test signals are included.

Main specifications for the Audio Generator are:

Frequency range	1 Hz to 25 kHz, single tone; 10 Hz to 25 kHz, multitone
Frequency resolution	1 Hz single tone, 10 Hz multitone
Frequency accuracy	+/-20 ppm
Output level range	0.8 mVp to 8.87 Vp, EMF
Output level flatness	+/-0.1 dB
Output level resolution	0.1 dB
Output impedance	600 ohm floating
THD	<-88 dB, typical <-90 dB

Filter Option

As the main signal processing in the RE201 is performed digitally, the dynamic range is limited by the resolution of the A/D converter. The RE201 employs a 12 bit converter which limits the dynamic range to approx. 75 dB. Especially for distortion measurements 75 dB may be a serious limitation so the filter option is designed to overcome this constraint. The filter option which is fully transparent uses a programmable notch filter to filter out the main component so that the full dynamic range of the A/D converter can be used for the harmonics.

Hereby the measurement range of the RE201 can be extended by approx. 30 dB for THD measurements and 10 dB for IM measurements. Furthermore the Filter Option comprises an RMS detector which enables broadband RMS measurements to 75 kHz and SINAD measurements (130 kHz bandwidth) at fundamental frequencies up to 25 kHz.

Weighting Filters Option

When performing signal to noise measurements on audio equipment it is required to measure according to approved standards in order to obtain comparable measurement results. The different standards specify:

1. How the noise signal must be weighted (filtered)

2. How the signal is to be detected

As well the weighting as the type of detection differs from application to application and therefore it has been necessary to include quite many filters:

a. CCITT P53 and C-message filter for measurement of noise in telephone systems. (CCITT P53 and US standards)

b. CCIR 468 and 31.5 Hz to 16 kHz (0.5 dB) bandpass filter for measurement of noise in broadcasting systems. (CCIR468 standard)

c. 300 Hz to 15 kHz (3 dB) bandpass filter with a 19 kHz notch for measurement of noise in FM radios. (DIN45633 and IEC651 standards)

d. Sound level filters A, B and C weighting for measurement of noise. (DIN 45633 and IEC 651 standards)

e. Rumble filters for measurement of weighted and unweighted rumble in disc record playing equipment (DIN 45539 and IEC 98A standards)

f. User recommended filters: the IBA filter for measurement of weighted crosstalk and Dolby Lab's filter (CCIR/ARM) for measurement of noise in professional as well as consumer audio equipment.

For each filter it is possible to select the required type of detection which may be:

a. Quasi-peak detection (as defined in the CCIR468 standard)

b. RMS detection (broadband or selective)

c. Average detection

These filters and detectors will together cover the major part of applications when measuring on consumer and professional audio equipment.

Wow and Flutter Option

With the Wow & Flutter Option installed it is possible to measure W&F in accordance with the commonly used DIN, NAB and JIS standards. The DRIFT measurement is part of the standard facilities in the RE201 Basic Unit. The W&F may be measured unweighted (200 Hz or 500 Hz bandwidth) or weighted according to the recommended weighting curves.

ZOOM Facility

Increased frequency resolution (i.e. better selectivity) is available with the ZOOM facility. Digital mixing and lowpass filtering are used to facilitate e.g. Intermodulation and Difference Frequency Distortion Measurements where distortion products may be separated a few Hz from the main components everywhere in the 20 Hz to 25 kHz frequency band. The option may also be used in applications calling for very selective spectral analysis as it provides a selectivity of better than 4 Hz (80 dB) over the entire frequency range. The option is transparent, i.e. it requires no special operator interaction.

1.3.3 Accessories

Table 1.4 lists the accessories available for the RE201.

Description	Code No.
Multicable for RE Memory Bus	617-761
Cable for DC-input	617-866
BNO Connector for DC-input	805-318
RE905 External Keyboard	906-032
RE201 Rack Mounting Kit	906-033
RE201 Service Kit	906-037

Table 1.4 - RE201 Accessories

Multicable - Special cable for connection of the RE201 and other RE equipment to be controlled by the Memory Bus. NB: The other instruments must be equipped with a Memory Bus Interface, part No. 900-997.

DC Input Cable - Coaxical cable with BNO connector for the DC input on the RE201. 3 banana plugs in the other end of the cable (one GROUND, one DC1 input, one DC2 input).

BNO Connector - Separate, mating connector for the RE201 DC input (BNO). Used for the customer's cables.

RE905 - A duplicate of the keyboard in the Front Panel. Designed for use if the RE201 is placed so far away from the test bench that it is inconvenient to operate the RE201 from the Front Panel (e.g. Memory Bus system applications). Provided with approximately 2 m of flexible cord.

Rack Mounting Kit - 19" rack mounts

***** Note *****

When rack-mounted the RE201 must be supported by a shelf as the rack mount is not designed to carry the full weight of the RE201.

Service Kit - Extender Board and cables necessary for performing adjustments and troubleshooting. The kit is comprised of:

* 1 Extender Board
* 1 14-way flat cable for Arithmetical Unit and ZOOM
* 2 16-way flat cable for Analog Frontend, Static CPU, Filter Option, Weighting Filters Option and Wow & Flutter Option
* 1 26-way flat cable for Audio Generator
* 1 coaxial cable with BNC connector for Audio Generator
* 1 Allen key for dismantling of the Digital Section
* 1 wrench for Audio Generator installation/ dismantling

1.4 Specifications

The following specifications are valid for the RE201 Dual Channel Audio Analyzer, basic instrument (i.e., excluding all options). A description of improvements and extensions obtained by options is found in the technical manuals for the individual options. The specifications outlined in the RE201 Operation Manual are valid for the RE201 including options.

Input

Full scale range	Autoranging from 2.8 mVpeak to 22 Vpeak (-51.8 dBu to 25.7 dBu)
Residual noise, RMS (input short-circuited)	Typical 9 µV (- 99 dBu), 25 kHz bandwidth 4 µV (-106 dBu), A weighted 8 µV (-100 dBu), CCIR unweighted 13 µV (- 97 dBu), 125 kHz bandwidth
Input circuit	2 balanced floating inputs, transformerless, overload protected to 50 Vpeak
Common mode rejection ratio	> 70 dB at 1 kHz
Maximum common mode voltage range	+/- 12V
Channel separation	> 110 dB at 1 kHz, > 95 dB at 15 kHz, 600 ohm generator impedance
Input impedance	330 kohm parallel with 100 pF
Leakage	< 2 µV in a 1 inch (25 mm) two turn loop held 1 inch (25 mm) from the instrument
Connectors	Isolated BNC, others available upon request

Measurements

DC Level Measurement - DC

Range	+/- 16V
Resolution	125 mV
Accuracy	+/- 125 mV
Connector	BNO type and 25 pin Sub-D female

Difference Frequency Distortion - DFIM

Standard	DIN 45403
Frequency range	20 Hz to 25 kHz
Selectivity	4 Hz, -80 dB
Sensitivity	-67 dB (0.02%)
Distortion products included	Selectable 2nd to 9th via spectral analysis
Accuracy	+/- 2.5 dB, DFIM -45 dB +/- 1.5 dB, DFIM > -45 dB
Display modes	%, dB

Frequency - FREQ

Range	4 Hz to 25 kHz
Resolution	1 Hz, 0.1 Hz below 200 Hz
Accuracy	+/- 0.1 Hz, 4 Hz to 60 Hz +/- 0.2 Hz, 60 Hz to 125 Hz +/- 0.8 Hz, 125 Hz to 200 Hz +/- 1.5 Hz, 200 Hz to 25 kHz
Display modes	Hz absolute, Drift (3.00 kHz or 3.15 kHz reference), deviation Hz or % relative to stored reference

Intermodulation - IM

Standards	SMPTE/DIN 45403
Frequency range	20 Hz to 25 kHz
Selectivity	4 Hz, -80 dB
Sensitivity	< -67 dB (0.04%), typical -72 dB any intermodulation product
Intermodulation products included	Selectable 2nd to 9th via spectral analysis
Accuracy	+/- 2.5 dB, IM -40 dB +/- 1.5 dB, IM > -40 dB
Display modes	%, dB

Peak Measurement - PEAK

Frequency range	20 Hz to 75 kHz
Flatness (ref. 1 kHz)	+/- 0.1 dB
Accuracy	+/- 2% + Flatness
Display modes	Positive and negative peak voltages displayed simultaneously in Volts

Phase - PHASE

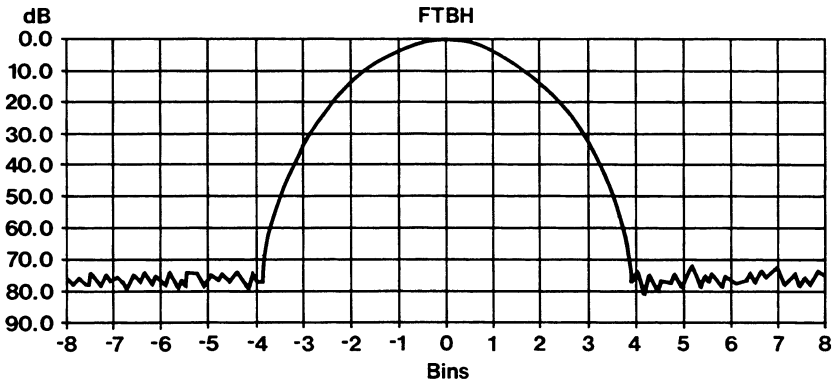
Frequency range	20 Hz to 75 kHz
Range	0 degrees to 360 degrees (0 to 2 π radians)
Accuracy	+/- 1 degree (+/- 0.017 radian) at input level > 20 mV
Display modes	Peak to peak phase variations, mean phase represented as radians or degrees, absolute or relative to stored reference or previously measured value

True RMS - RMS25

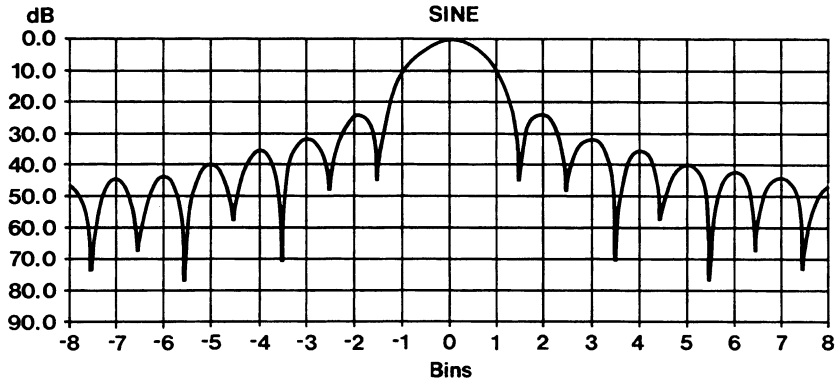
Frequency range	20 Hz to 25 kHz
Cutoff frequencies	25 kHz, -0.1 dB; 41 kHz, -85 dB
Flatness (ref. 1 kHz)	+/- 0.1 dB
Accuracy	+/- 1.5% + Flatness at 1.5V +/-3% + Flatness overall
Display modes	Volt, Watt, dBm, dB relative to the other input, dB or % relative to stored reference or previously measured value

Selective RMS - SEL

Frequency range	20 Hz to 25 kHz
Maximum selectivity	-80 dB at +/- 4 Hz
S/N ratio	Typical -74 dB
Flatness (ref. 1 kHz)	+/- 0.1 dB
Accuracy	+/- 1.5% + Flatness at 1.5V +/- 3% + Flatness overall
Display modes	Volt, Watt, dBm, dB or % relative to stored reference or previously measured value
Filters available	Refer to graphs below



FTBH Window used; 1 bin corresponds to 0.98 Hz



SINE Window used; 1 bin corresponds to 0.98 Hz

Separation - SEP

Description	R/L and L/R separation simultaneously measured selectively
Sensitivity	> 70 dB at equal input levels Crosstalk measurements performed using RMS25

Harmonic Distortion - THD

Frequency range	20 Hz to 25 kHz, harmonics included
Sensitivity at 1 Vrms	-70 dB (0.03%), typical -72 dB
Harmonics included	Selectable 2nd to 9th
Accuracy	+/-2.5 dB, THD -50 dB
	+/-1.5 dB, THD >-50 dB
Maximum distortion	60% (-4.5 dB)
Display modes	%, dB

Transient Intermodulation - TIM

Sensitivity	< -55 dB (0.2%)
Accuracy	+/- 2.5 dB, TIM < -35 dB
	+/- 1.5 dB, TIM > -35 dB
Display modes	%, dB

Interface Capabilities

IEEE std. 488-1978

Capabilities

Function	Subset	Extent of Implementation
Source Handshake	SH1	Complete capability
Acceptor Handshake	AH1	Complete capability
Talker	T6	Talk only omitted
Listener	L4	Listen only omitted
Service Request	SR1	Complete capability
Remote Local	RL1	Complete capability
Parallel Poll	PP1	Remote configuration
Device Clear	DC0	No capability
Device Trigger	DT1	Complete capability
Controller	C0	No capability
Driver Type	E2	Tri-state (except during Parallel Poll)

EIA RS-232C

Capabilities	Screen dump to printer, dump and load of measurement and/or signal definitions
Baudrates	300 to 9600 Baud
Stop bits	1, 1.5 or 2 bits
Parity	Odd, even or none

RE Memory bus

Capabilities	Control of other RE products
Number of setups	100

GPIO

Capabilities	Control of user supplied products
Description	20 bit programmable TTL outputs plus load pulses

Monitor output

Capabilities	Composite video signal to drive external CRT monitors
Impedance	75 Ohms
Level	2.3 Vpeak

Non-volatile Memory Capacity

Measurement definitions	10 per measurement (20 level measurements)
Sequences	20, each consisting of up to 9 measurements
Audio generator signals	100
Multi tone signals	10, each consisting of up to 8 components
Setups	100, containing paired measurements and signals, Memory bus setting and GPIO output

Physical Characteristics

Height	221.5 mm (8.72 inches)
Width	440 mm (17.32 inches)
Depth	570 mm (22.44 inches)
Net weight	24 kg (52.91 lbs.)
Shipping weight	31 kg (68.34 lbs.)

Power Requirements

Consumption	90 VA
Line frequency	47.5 Hz to 63 Hz
Line voltage	90 V to 130 V AC 190 V to 260 V AC

Environment

Operation	5° C to 40° C (41° F to 104° F)
Storage	-40° C to 70° C (-40° F to 160° F)
Humidity	20% to 80%, non-condensing

2 PRINCIPLES OF OPERATION

The RE201 Dual Channel Audio Analyzer is a modular, combined analog and digital instrument, designed for measuring the performance of sound reproduction equipment. In order to obtain a high degree of versatility, a wide range of options provided as plug-in PC-boards are available, enhancing the interface and measurement capabilities of the instrument in accordance to the needs of the actual application.

For a short description of each of the options, refer to section 1.3.2.

2.1 Measurement Principles

In general, two different measurement principles are being employed: Spectral analysis, based on the Fast Fourier Transform (FFT), and analog detectors. By using digital and analog techniques throughout the design of the instrument, it has been the goal to "pick the best from two different worlds".

The FFT is used for all distortion measurements (except the SINAD measurement provided by the Filter option), for the frequency measurement and for the selective level measurement.

Analog detectors are mainly used for the various level measurements:

* Peak
* RMS in 75 kHz bandwidth (Filter Option)
* Quasi-peak (Weighting Filters Option)

The phase measurement, the wow and flutter measurement (option) and the SINAD measurement (Filter Option), however, also utilize analog detectors. The latter is actually carried out as two RMS measurements.

Dedicated digital hardware is used to calculate the true RMS value (25 kHz bandwidth), whereas the 'AVERAGE' level is calculated directly from data samples read from the A/D converter. The DC measurement is based on a successive approximation method, using D/A converters.

Following the analog detection, measurement results are digitized by means of the same Analog-to-Digital converter (A/D) which is used for spectral analysis (FFT). Most of the outputs from the analog detectors are smoothed by digital filtering implemented in software.

The general signal handling during measurements is depicted in the simplified Block Diagram, fig. 2.1. The basic principles are described in the following.

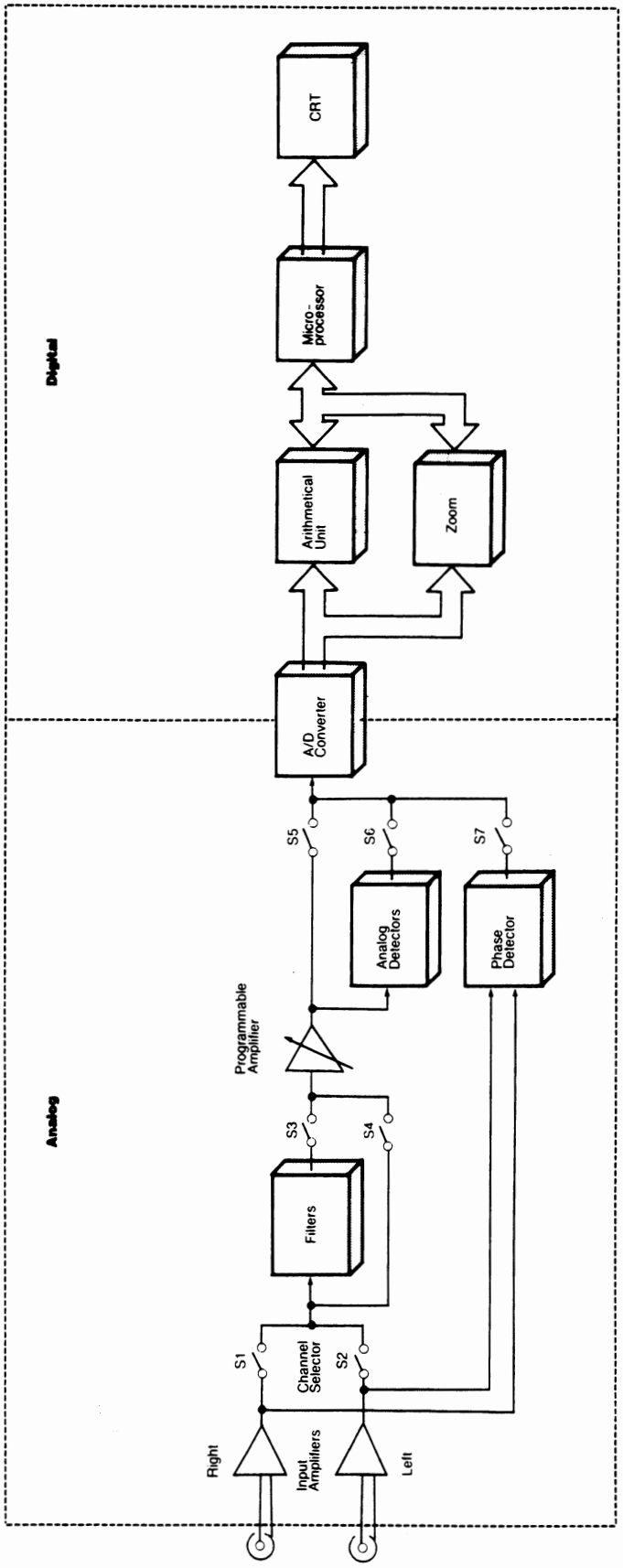


Fig. 2.1 - RE201 Simplified Block Diagram

In order to reduce the amount of hardware, only the input attenuators are dedicated to each channel. Thus, measurements in both channels are performed sequentially. The actual input channel is determined by a channel selector (S1, S2) following the input attenuators. The detector used for phase measurements utilizes the output from both input attenuators, since during this measurement it is necessary to have signals from the two channels available simultaneously at the measuring circuitry.

Following the channel selector, the input signal is supplied to various filters - lowpass filters, notch filters, weighting filters etc. By means of software controlled switches, the output from the filter applicable to the actual measurement type may be selected, or the filters may be bypassed (S4 closed).

By means of an amplifier, programmable in 2 dB steps, the signal may be adjusted to a well-defined level for further processing. This processing may involve one of the analog detectors, or the AC signal may be directly presented to the Analog-to-Digital (A/D) converter (S5 closed). Again, the actual signal path is selected by software controlled switches.

Following the sampling and digitizing, the 12 bits of data from the A/D converter is subject to digital signal processing, either the Fast Fourier Transform or software filtering. A so-called Arithmetical Unit handles the digital signal processing under microprocessor control. For increased frequency resolution, the ZOOM may be employed. The results are displayed on the CRT, which is controlled by the microprocessor.

2.2 The Fast Fourier Transform

The Fast Fourier Transform is an algorithm used to speed up the computations involved in Fourier analysis (Discrete Fourier Transformation). Since certain complex multiplication products appear over and over during the computations, the FFT organizes these and calculates the required products only once. Thus, it should be noted that the FFT is merely an efficient algorithm to calculate a Discrete Fourier Transform - not a different kind of transform in itself. The FFT algorithm was first published by Cooley and Tukey: "An Algorithm for the Machine Calculation of Complex Fourier Series" in the Mathematics of Computation (1965).

The FFT algorithm transforms N equally spaced samples of a time function to N equally spaced samples of the associated frequency spectrum. In the RE201, the spectrum used for spectral analysis is computed by a microprocessor (the Main CPU). 512 data samples are collected and stored, then the spectrum is calculated by means of a 256 point complex FFT (equivalent to a 512 point real FFT), and the spectral components of interest are extracted. Thus, the analysis is not real time, but repeated over and over continuously.

The spectrum generated from the samples of the input signal does not, however, resemble the output of a conventional analog spectrum analyzer. This is a consequence of inherent properties of the digital signal processing.

The amount of information which can be extracted from the digital spectrum is mainly restricted by three parameters:

* The number of bits used in the analog to digital conversion
* The sampling period (T)
* The number of samples collected (N)

The first two parameters are mainly limited by the A/D converter used. The number of bits determine the degree to which the amplitude of the signal may be resolved, and hence this is limiting the dynamic range. In order to benefit from all 12 bits of the A/D converter, the entire input voltage swing for the converter must be utilized, meaning that the peak voltage of the signal being applied to the converter must be as close as possible to +/- 2.5 Volts. This task is handled by the autoranging feature of the RE201.

The sampling rate is a limiting parameter, because sampling of a time signal causes the spectrum of the time function to be repeated with frequency distance 1/T. This repetition generates 'aliasing' in the frequency domain. Aliasing means that following the digital processing, parts of the spectrum have been "contaminated" with spectral components originating from other parts of the real spectrum.

In order to avoid the aliasing, which may cause incorrect measurement results, the frequency contents of the signal must be controlled by means of a lowpass filter (antialiasing filter). Furthermore, the analog signal must be sampled at a sampling rate at least twice the highest frequency in the signal (the Nyquist rate). In order to obtain a bandwidth of 25 kHz, a sampling rate of 64 kHz has been chosen for the RE201. Frequency components above half the sampling frequency (32 kHz) are removed before the analog input signal is applied to the Analog-to-Digital converter.

The third parameter, the number of samples, together with the sampling rate, determines the time truncation of the signal, i.e. the final extent of the observation period (sampling period). As the sampling period does not necessarily match a natural period of the input signal, discontinuities are introduced at the beginning and end of each observation period. These discontinuities are responsible for spectral contributions, "leakage", over the entire frequency range, meaning that sinusoids in the digital spectrum do not appear as single lines, but as a broad spectrum.

The leakage may also be regarded as a 'time domain aliasing', due to sampling in the frequency domain, equivalent to the above mentioned frequency domain aliasing, which is due to sampling in the frequency domain.

In order to reduce the effect of the time truncation, a windowing function is multiplied on the sampled data, thus reducing the order of the discontinuities by smoothly bringing the data values to zero at the boundaries of each observation period. Alternatively, the windowing function may be considered as a transformation of the input signal into a signal with a natural period equalizing the observation period.

The actual amount of the leakage depends on the window function used. In fact, in the digital spectrum a single frequency appears as the sampled Fourier Transform of the window function used. The term 'window' is used, as the time signal is 'viewed' through this function.

As may be figured from the above, the sampling rate, the number of samples involved in the FFT and the window function used determine altogether the minimum separation between frequency components to be resolved. The FFT produces frequency samples with a spacing of 1/NT (64 kHz/512 = 125 Hz for an RE201 not using the ZOOM facility). A very useful interpretation of the results from an FFT is to think of the output from an N-point FFT as one set of samples of the outputs from a filter bank consisting of N identical filters, all having frequency response equal to the Fourier Transform of the windowing function. The center frequencies for the filters are 0, 1/NT, 2/NT and so forth.

The RE201 may utilize two different window functions:

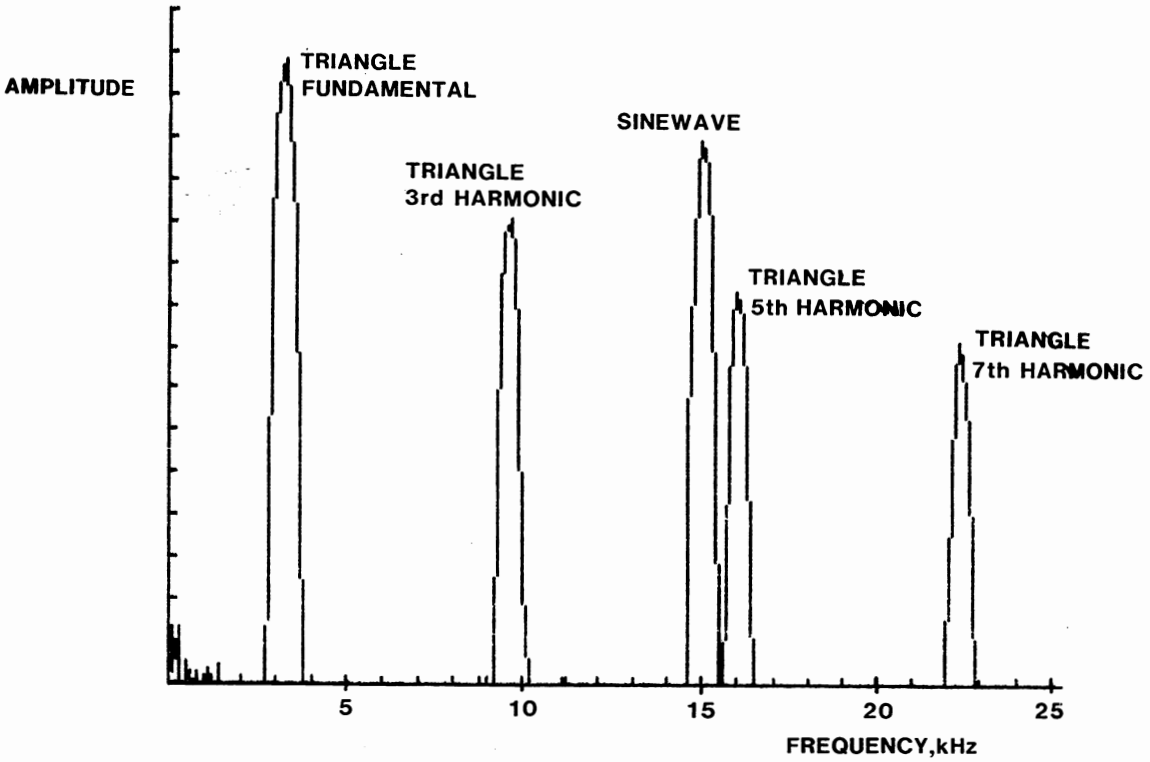
* Four Term Blackmann-Harris (FTBH)

* Sine

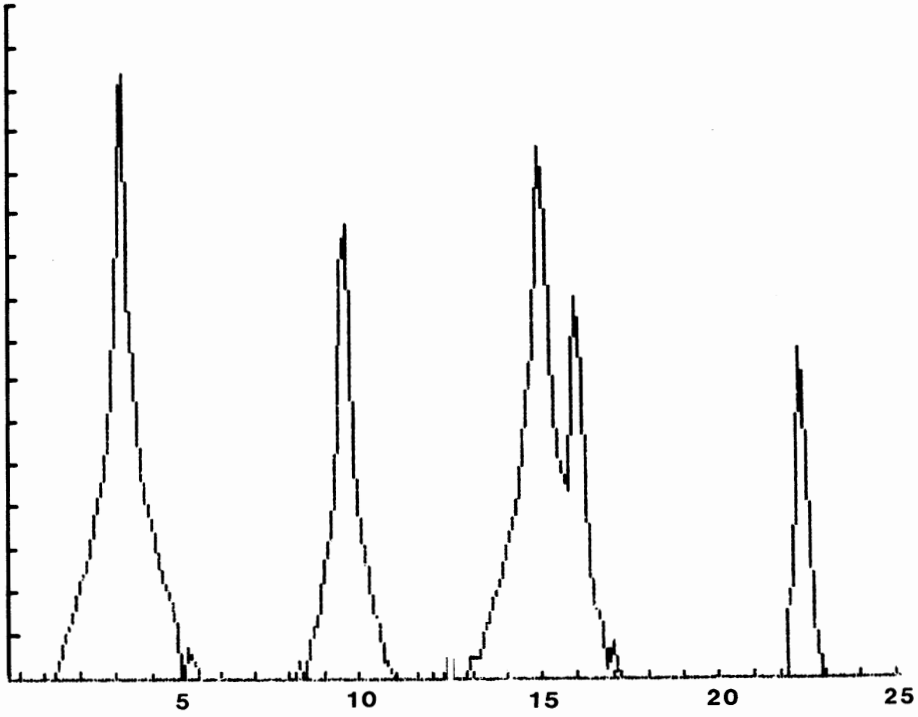
The Fourier Transform of the FTBH window, i.e. the equivalent filter, has a relatively broad main lobe, whereas sidelobes are practically not present. This window is used most of the time in order to ensure high isolation from other signals in the input spectrum.

Spectra, actually recorded from the RE201, are shown in fig. 2.2 for both window functions. As an example has been chosen a 3.2 kHz triangle wave superimposed with a 15 kHz sine wave (TIM test signal).

If the sampling rate is reduced, the width of the windows in the frequency domain is narrowed and consequently the frequency resolution is improved. It must be ensured, however, that high-frequency components which may cause aliasing, are removed.



(a) FTBH window used



(b) SINE window used

Fig. 2.2 - Spectra for Different Windows

In the RE201, increased frequency resolution may be achieved by means of the ZOOM facility.

By means of digital mixing of the digitized input signal with a programmable, digitally synthesized frequency, the frequency band of interest is 'moved' to DC, and then digitally lowpass filtered and resampled with a lower sampling frequency. This method may be used to obtain increased frequency resolution over the entire frequency range.

Using the ZOOM facility, frequency components may be obtained with a frequency resolution down to 0.98 Hz. Fig. 2.3 depicts a part of the same spectrum as fig. 2.2, enlarged after ZOOM processing.

For further information, refer to the ZOOM facility in the Technical Manual.

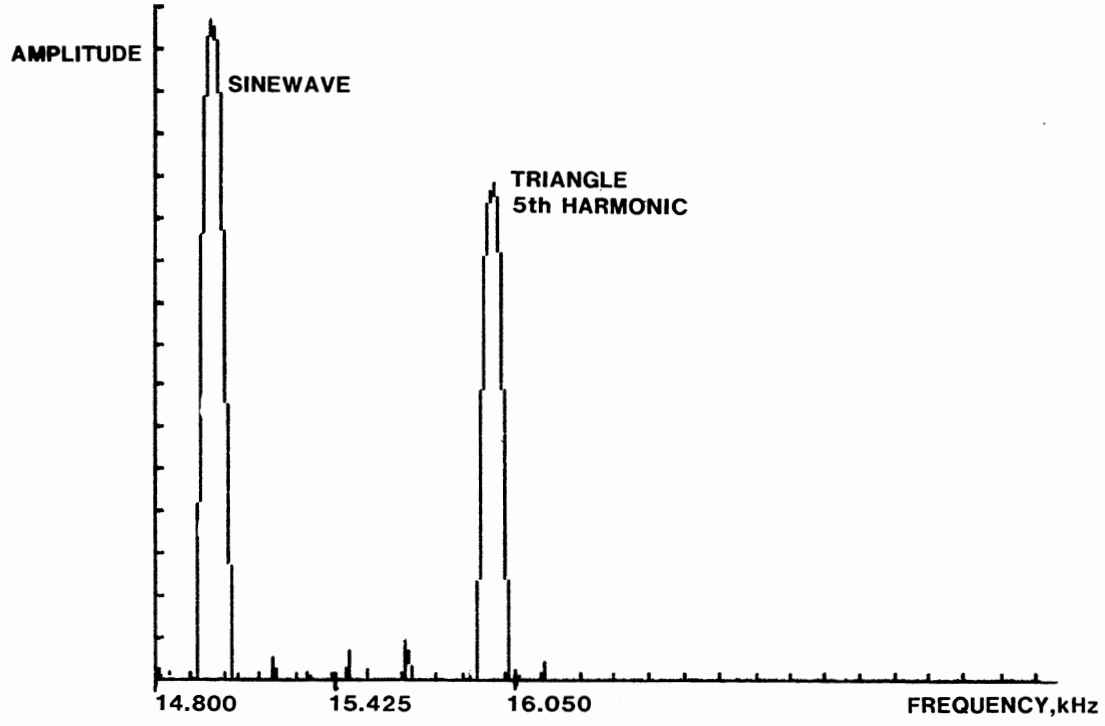


Fig. 2.3 - ZOOM Spectrum

2.3 Microprocessors

The RE201 is controlled by two 16 bit microprocessors, one providing the interface to the operator and to the analog circuitry - the Static

CPU - while the second - the Main CPU - handles the actual measurements including calculation of the FFT.

The major tasks for each of the CPU's may be summarized as follows:

Static CPU:
* Execution of LEARN MODE
* Monitoring of keyboard(s)
* Setup of analog signal paths etc.
* Autoranging of input
* Control of Memory Bus
* Control of GPIO
* Execution of DC measurements
* Control of Audio Generator Option

Main CPU:
* Execution of measurements incl. FFT
* CRT display control
* IEEE488 Bus Interface
* RS232C Interface

As a microprocessor produces broadband noise making measurements on sensitive receivers almost impossible, two different techniques have been employed in order to overcome this problem.

One technique - the more conventional one - is shielding; this is used for noise reduction of the Main CPU performing the measurements. The processor and related digital circuitry performing the digital signal processing are enclosed in a separate, shielded box to minimize Electromagnetic Interference. All signals in/out of the box must be filtered. Thus, the number of such interconnections has been kept at a minimum.

The other technique is used for the frontend processor. During all measurements and periods where the keyboard is not activated, the computer is inactive, as the clock oscillator is stopped. As almost all Electromagnetic Interference is related to this high-frequency oscillator, this effectively removes EMI during periods of measurement. As soon as e.g. a Front Panel key is activated by the operator, the clock oscillator is enabled, and the computer is restarted in order to pick up the input from the keyboard. Other events restarting the CPU are overload in the analog signal path or a

message (command) from the Main CPU. From this mode of operation, the CPU is named the Static CPU.

Inputs from the operator and commands concerning analog circuit setup must be communicated between the two CPU's. Therefore, they have been loosely coupled using a medium speed serial bus structure, which only needs two interconnection lines.

The instrument may thus be divided into three different sections:

* Analog Section - non-shielded, as CPU is static
* Digital Section - carefully shielded, as CPU is active
* Display section (CRT) - shielded to avoid EMI from the CRT.

Drawing No. 985-217 at the rear of this manual depicts the detailed Block Diagram, with all interconnections between the different sections shown. From this may be observed that all signals in/out of the shielded sections - the Digital Section and the CRT section - are either transmitted in coaxial cables or carefully filtered by means of pi-filters.

2.4 Start of Measurements, Sequences and Setups

This section describes the various tasks being performed by the RE201 upon activation of the different facilities.

Start of Measurement

When a measurement is started, the following steps are executed:

a. The user selects the measurement using the keyboard, this is detected by the Static CPU, monitoring the keyboard.

b. The Static CPU fetches the measurement definition from CMOS RAM. If channel selection is 'TBD' (To Be Defined), a prompt for actual channel is issued.

c. The Static CPU dumps the appropriate screen picture for result display to the CRT controller via the Main CPU.

d. The measurement parameters are transmitted to the Main CPU; the Main CPU performs the parameter check and issues an acknowledge message to the Static CPU. Upon receipt of this message, the Static CPU enters the static mode (the clock oscillator is stopped by the CPU itself).

e. The Main CPU now starts the measurement: The proper setup for the signal path in the Analog Frontend (and analog options, if applicable) is composed and transmitted as a

command to the Static CPU (controlling the Analog Section), followed by an autorange command. Upon receipt of the commands, the Static CPU is restarted.

f. The Static CPU sets up the signal path and performs autoranging, utilizing the peak detectors and the A/D converter of the Analog Frontend.

g. The gain which is set as a result of 'f' above, is communicated to the Main CPU. Then, the Static CPU is stopped again.

h. Having received the gain information, which is used for result calculation, the Main CPU waits for the Frontend to settle. The settling time depends on various factors, such as measurement type, actual gain etc.

i. When the settling time has elapsed, the actual measurement procedure is initiated.

j. After completion of a measurement run, the "input low" condition is checked - this is done in different ways and with different acceptance levels according to the actual measurement. Overload detection is done by hardware in the Analog Frontend.

For measurements involving spectral analysis, the Fast Fourier Transform is employed as follows:

a. 512 data samples are collected by the Arithmetical Unit and stored in RAM.

b. Upon completion of this, the Arithmetical Unit notifies the Main CPU.

c. The Main CPU then calculates the spectrum (employing the FFT), utilizing dedicated hardware of the Arithmetical Unit. From the digital spectrum the information of interest is extracted, and the result is displayed on the CRT (transferred to the IEEE488 bus, if the RE201 is in the REMOTE state).

For measurements involving the ZOOM facility, preprocessing of the time samples (mixing and lowpass filtering) is carried out before the FFT is employed (refer to the Technical Manual for the ZOOM facility for further information).

All measurements based on analog detectors are in principle performed in an equal manner:

a. The Analog Frontend is set up as above, routing the output from the active detector to the A/D converter.

b. The Main CPU reads the A/D converter; as the output of the detectors usually is fluctuating, lowpass filtering, implemented in software, is employed on the data samples from most of the detectors.

Since the analog detectors produce DC output, which is not processed by the FFT, the frequency limitation of 25 kHz due to the aliasing problem does not apply. As an example, if the signal is routed to the peak detectors, the 25 kHz lowpass filter is bypassed.

Start of a Sequence

When a sequence of measurements is activated, the procedure is very similar to that of a single measurement activation. The Static CPU fetches the information about which measurements constitute the sequence, then it composes the result display and sends it to the Main CPU, followed by each measurement definition. If a measurement with channel selection 'TBD' is encountered, the user is prompted for the channel, as for single measurements.

Before the sequence is started by the Main CPU, the measurements are ordered so that all measurements in the left channel are carried out before measurements in the right channel. This minimizes the need to alternate between the two channels, thus reducing measurement time. Autoranging is only performed once in each channel; the gain set up for each channel is stored and reestablished after succeeding channel changes.

It should, however, be noted, that separate gains are established for each of the following conditions:

* 25 kHz bandwidth measurements (anti-aliasing filter employed)

* Peak measurements (anti-aliasing filter bypassed)

* SINAD measurements (when measuring the noise and distortion)

Start of a Setup

The different activities of a setup are initiated in the following order:

a. The setup number is output to the Memory Bus and the REMOTE signal is activated - this causes all connected instruments to go to the remote state and to recall the actual setup.

b. The GPIO is set up and LOAD pulses issued.

c. The Audio Generator Option is activated (if applicable).

d. The measurement/sequence comprised in the setup is activated.

e. The Memory Bus Uncalibrated input signal is checked; if active, a message is sent to the Main CPU. The latter checks whether the instrument is remote controlled; if so, a Service Request is issued via the IEEE488 Bus (refer to RE201 Operation Manual, IEEE488 Commands Description).

Upon EXIT from a setup, the Memory Bus REMOTE signal is released, thus restoring the local state of the instruments connected to the bus.

2.5 Actual Measurement Setups

Table 2.1 gives a survey of the principles applied to the various measurements.

Special cases are the RMS25 measurement, the Average measurement and the DC measurement. The RMS25 measurement is implemented in digital hardware, performing directly the squaring and summation of data samples. After completion of the measurement period, the result is fetched from a 48 bit register by the Main CPU, which calculates the square root of the sum and calibrates the result according to the actual gain of the Analog Frontend. The Average measurement is done by direct computation from data samples collected from the A/D converter by the Main CPU. The DC measurement is - as the only measurement - performed by the Static CPU. The algorithm is a successive approximation utilizing dedicated D/A converters, located on the I/O & Memory Bus Interface board.

In the following, the actual setup of switches in the Analog Frontend is described for each type of measurement. The description is based on an RE201 equipped with the Filter Option, Weighting Filters Option and , Wow & Flutter Option, as this configuration is the most complicated one. Setups for other option configurations may be extracted from the information given. The Audio Generator Option is not included, as it is not interfering with the signal path for the input signal. Details concerning individual blocks are found in section 3, Circuit Descriptions, of this manual, and in the separate Technical Manuals for the options.

Fig. 2.4 shows a Block Diagram of the Analog Frontend and the above mentioned options. All the switches shown are implemented by means of FET-transistors, which are switched ON/OFF by the microprocessor in the Analog Section (the Static CPU). For reference purposes, the actual correspondence between switches and transistor designations for the FET's are given.

Figs. 2.5 to 2.11 show the setups employed for various measurements. It should, however, be noted that during actual measurements, the setup may temporarily be changed, e.g. during autoranging or when check of input level or the like is being performed. In the figures

Measurement	Principle
Average	Direct software calculation from time samples
DC	Successive approximation performed by the Static CPU
DFIM	FFT analysis; ZOOM used when difference frequency < 475 Hz
Frequency	FFT analysis; ZOOM used when frequency < 200 Hz
IM	FFT analysis; ZOOM used when lower frequency < 475 Hz
Peak	Analog detectors (Analog Frontend)
Phase	Analog detector (Analog Motherboard)
Quasi-peak	Analog detector (Weighting Filters Option)
RMS 25 kHz BW	Digital detector (Arithmetical Unit)
RMS 75 kHz BW	Analog detector (Filter Option)
RMS relative	Two successive RMS25 measurements (one for each channel)
RMS selective	FFT analysis; ZOOM used when bandwidth < 600 Hz
SINAD	Two successive RMS75 measurements, with and without the fundamental frequency removed by means of the notch filter of the Filter Option; frequency determined via FFT
Separation	FFT analysis; ZOOM used when lowest frequency < 250 Hz or frequency difference < 475 Hz
TIM	FFT analysis
THD	FFT analysis; ZOOM used when highest harmonic to be included < 9812 Hz
Wow & Flutter	Analog detector (Wow & Flutter Option)
Measurements exclusive for the IEEE488 Bus Interface	
DATACO	Data collection from A/D converter.
RMSFIL	FFT analysis; ZOOM user selectable
SPECTR	FFT output; ZOOM user selectable
TRIMFQ	FFT analysis (partial FFT)
TWOLEV	FFT analysis; ZOOM used when frequency < 250 Hz or frequency difference < 475 Hz

Table 2.1 - Measurement Principles

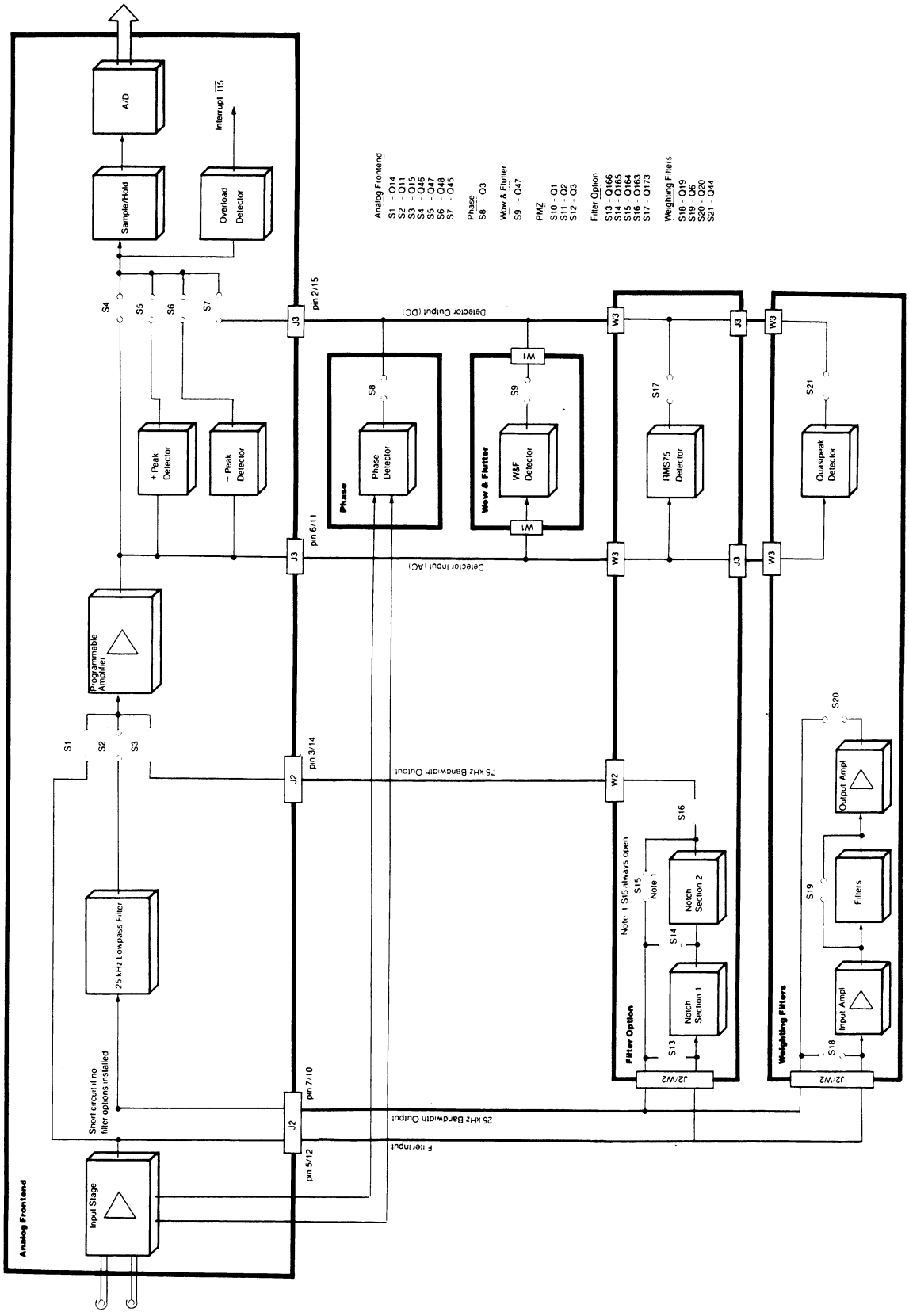


Fig. 2.4 - Measurement Setup Block Diagram

the signal path is highlighted; only switches which must be either closed or opened are shown. This means that the position of switches not specifically shown is arbitrary.

NORMAL Setup (Fig. 2.5)

The setup designated NORMAL is used for measurements in 25 kHz bandwidth, i.e. RMS25, Frequency, Average and all types of distortion measurements except SINAD.

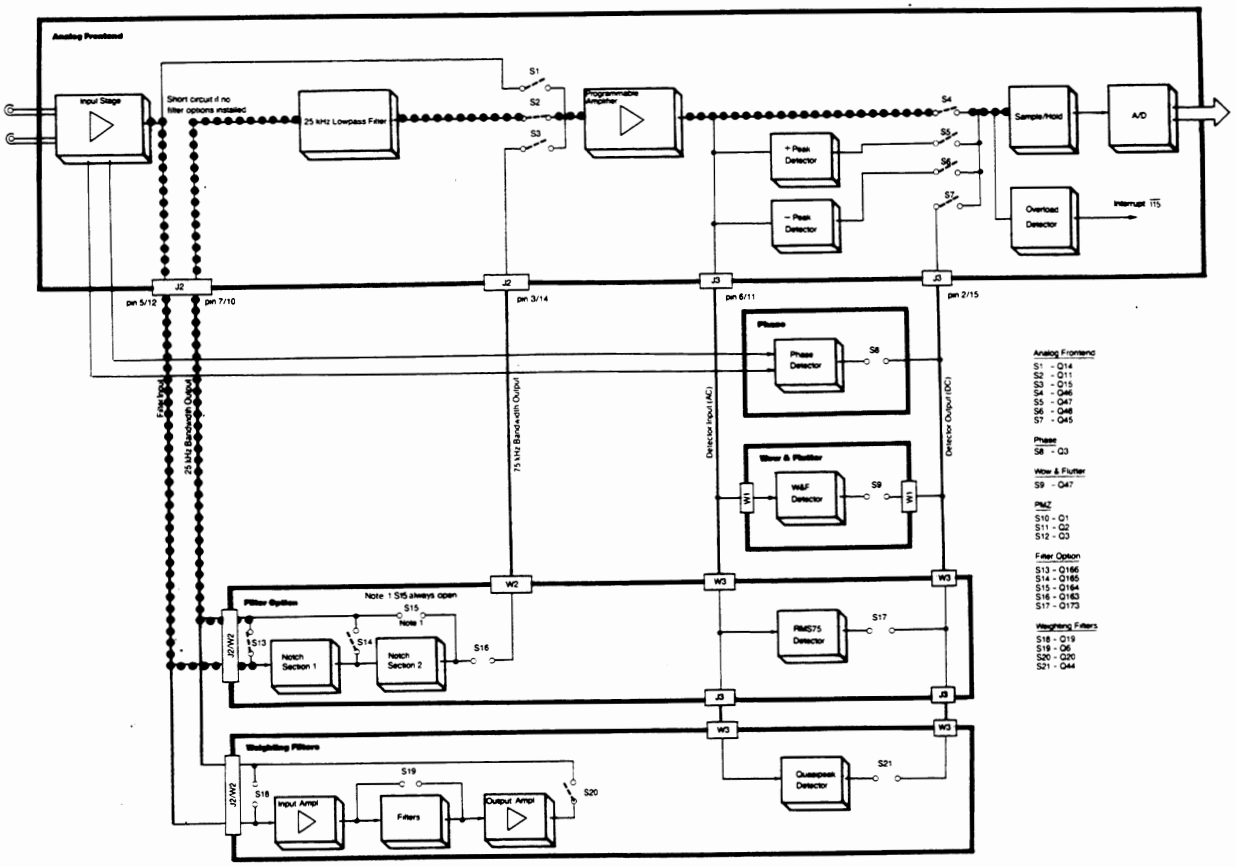


Fig. 2.5 - NORMAL Setup

The following should be noted:

* If the Filter Option is not installed, S18 on the Weighting Filters Option is used to connect the Filter Input (pins 5/12) to the 25 kHz Bandwidth Output (pins 7/10).

Peak Measurements (Fig. 2.6)

When peak measurements are executed, toggling between S5 and S6 is done to accomplish sequentially measurements of positive as well as negative peak voltages. When measuring peak voltages, the 25 kHz antialiasing filter is bypassed to enable measurements in a bandwidth of approx. 75 kHz.

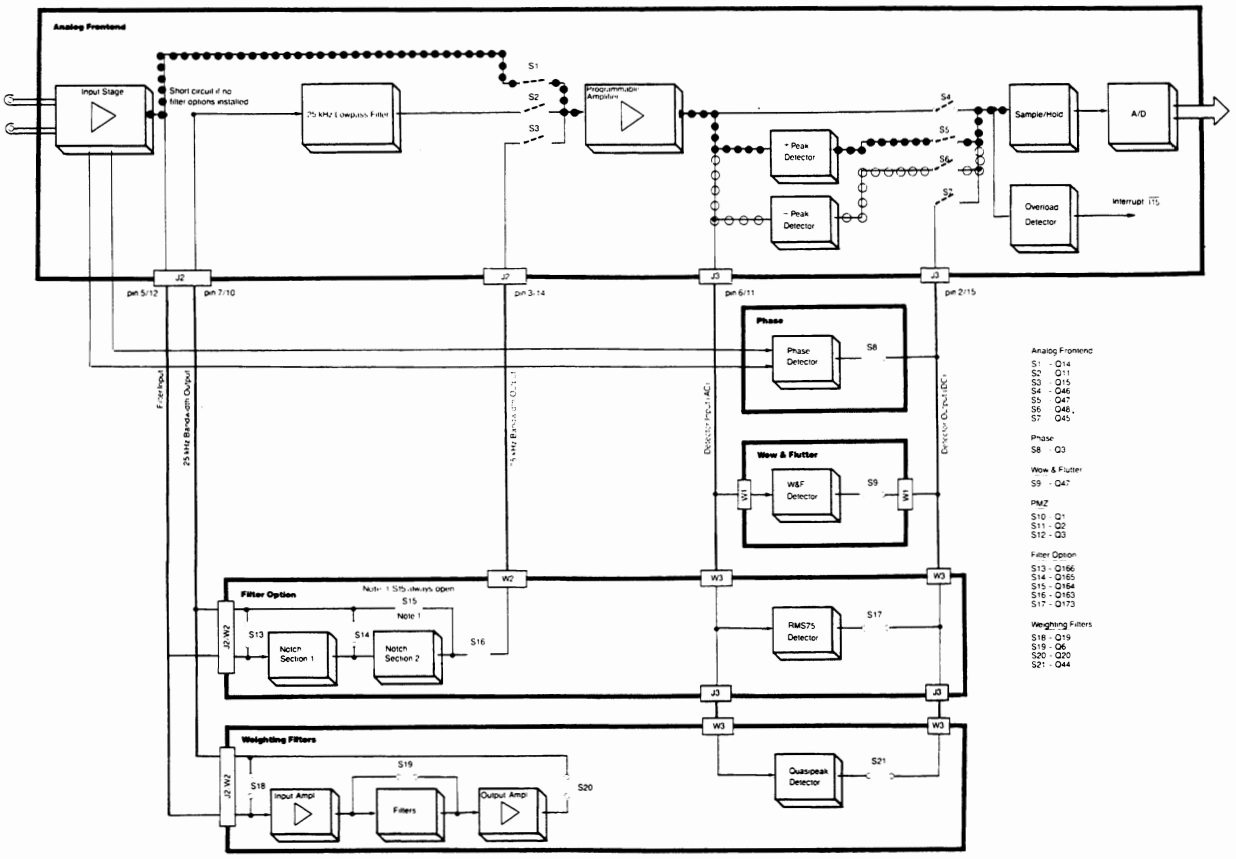


Fig. 2.6 - Peak Measurements

Phase Measurements (Fig. 2.7)

The input to the phase detector is taken directly from the input stage in order to obtain simultaneous information about the input signals in both channels. These signals are routed via the Analog Frontend board edge connector to the Analog Motherboard where the Phase detector is located; the output is routed likewise from the Phase detector to the Analog Frontend. This is in contrast to other analog signals, which are routed in flat cables connecting to the top edge of the analog boards.

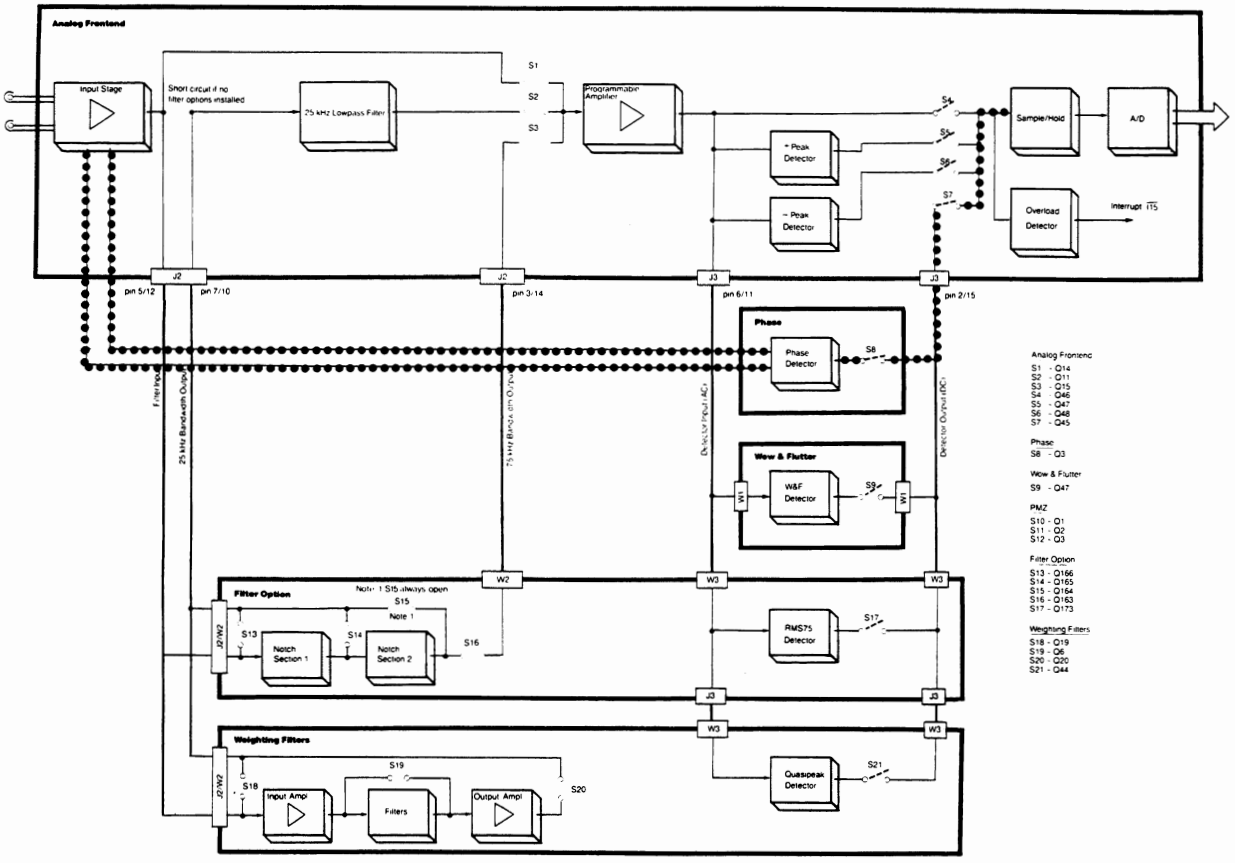


Fig. 2.7 - Phase Measurements

As may be observed, the output switches from other analog detectors connecting to the detector bus are all opened during phase measurements.

RMS75 Measurements (Fig. 2.8)

The RMS detector used for 75 kHz bandwidth measurements is located on the Filter Option board. The 25 kHz antialiasing filter is bypassed for this measurement. As for the phase measurement, the output switches for other analog detectors are opened.

THD or IM Using Filter Option (Fig. 2.9)

If all harmonics are below -64 dB, and the Filter Option is installed, the notch filter of this option is switched in to reject the fundamental frequency component when measuring the level of the harmonic components (for further information, refer to the Technical manual for the Filter Option). As 40 dB amplification of the harmonics, relative to the fundamental, is sufficient for full range THD measurements, only one of the Notch Filter Sections is used. If the Filter Option is not available, or the level of one of the harmonics is above -64 dB, the THD result is extracted from a single spectrum, obtained with the switch setting shown as NORMAL (fig. 2.5).

The setup is identical for IM measurements employing the Filter Option.

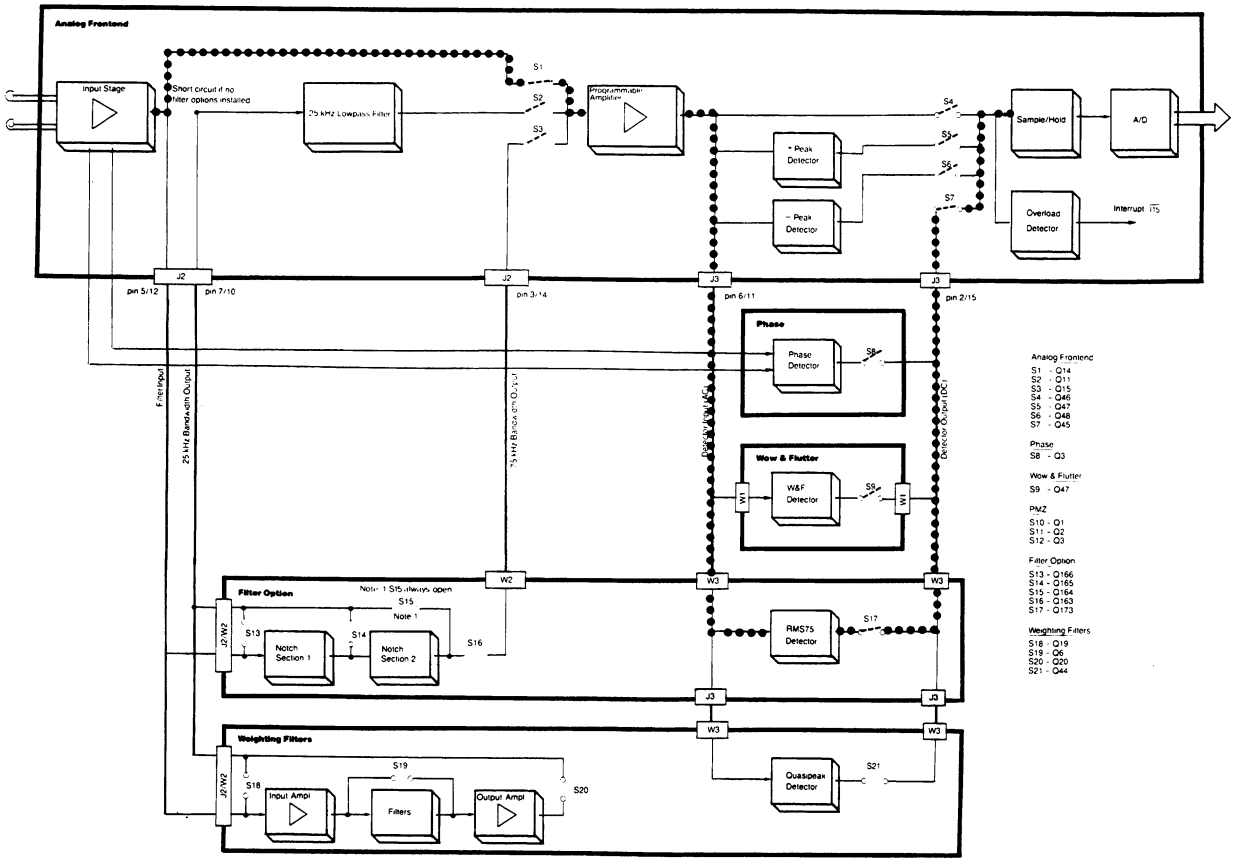


Fig. 2.8 - RMS75 Measurements

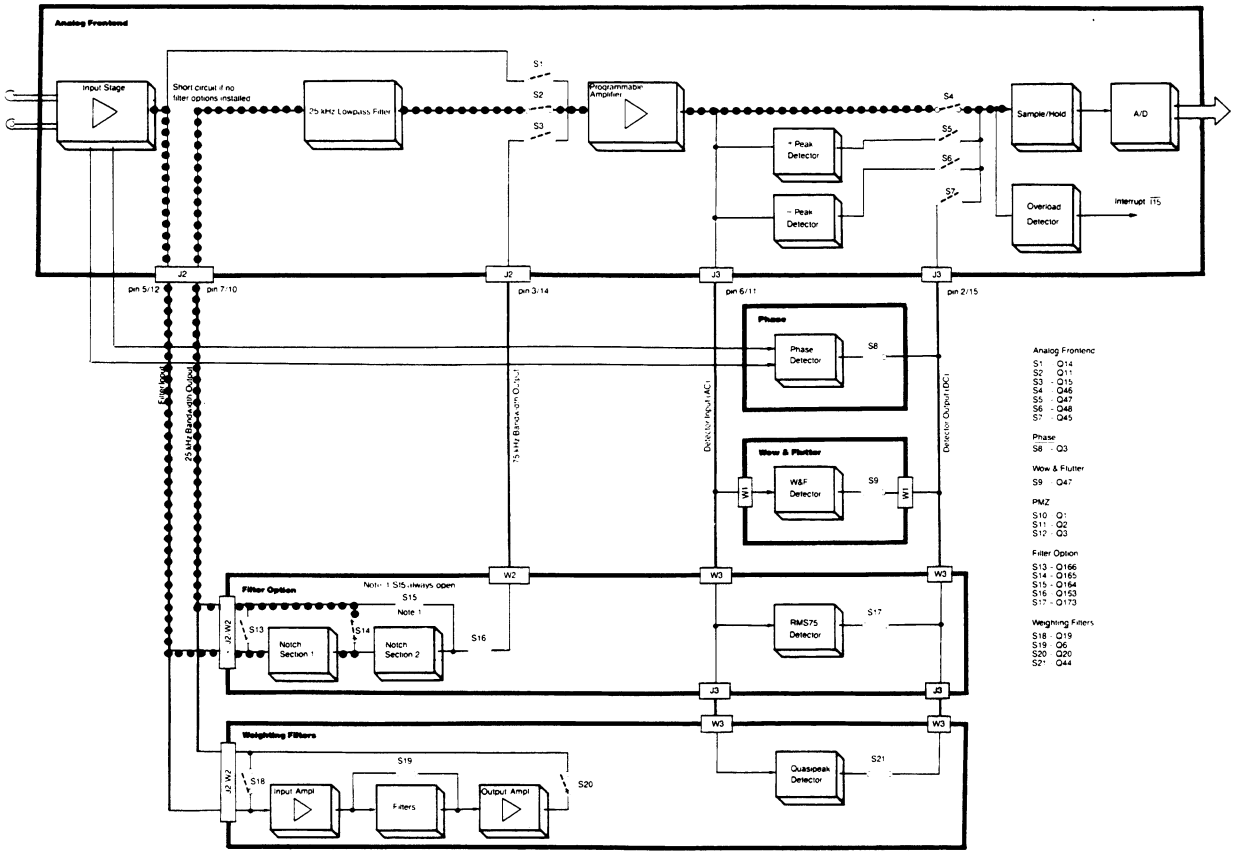


Fig. 2.9 - THD or IM Using Filter Option

SINAD Measurements (Fig. 2.10)

A SINAD measurement is executed as two RMS75 measurements, one on the entire signal and one on the noise and distortion. The first is performed as a standard RMS75 measurement (refer to the pertinent section above), the second is done with the setup shown in fig. 2.10. The notch filter (both sections) is inserted in the signal path, removing the fundamental component of the signal. The remaining signal - the noise and distortion - is amplified, using both the amplifiers included in the Filter Option and the programmable amplifier of the Analog Frontend and measured by means of the RMS75 detector.

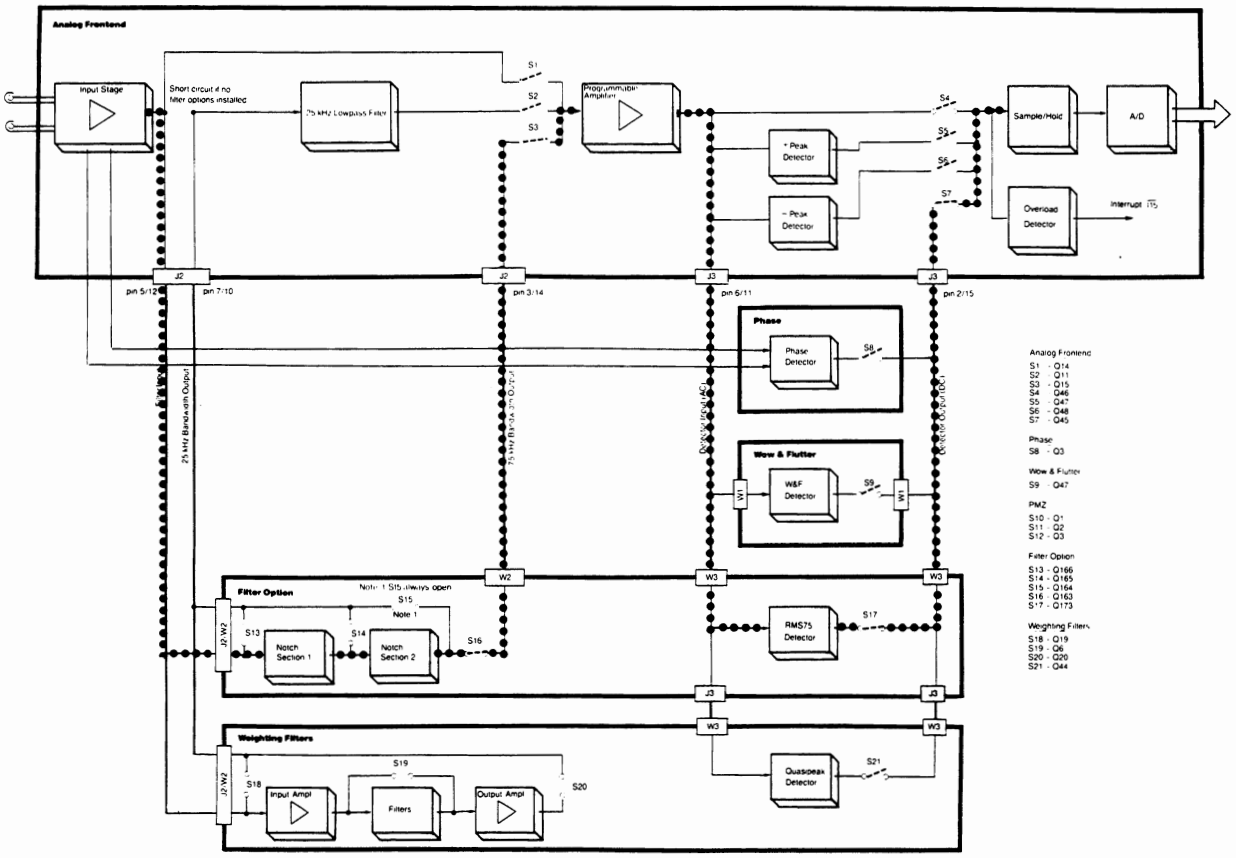


Fig. 2.10 - SINAD Measurements

Wow & Flutter Measurements (Fig. 2.11)

For the Wow & Flutter measurement (fig. 2.11), the input signal is routed to the antialiasing filter to remove interfering noise, and then via the programmable amplifier to the Wow & Flutter detector.

During Wow & Flutter measurements, check of the input level is performed with regular intervals. This check is accomplished by switching between S5/S6/S7.

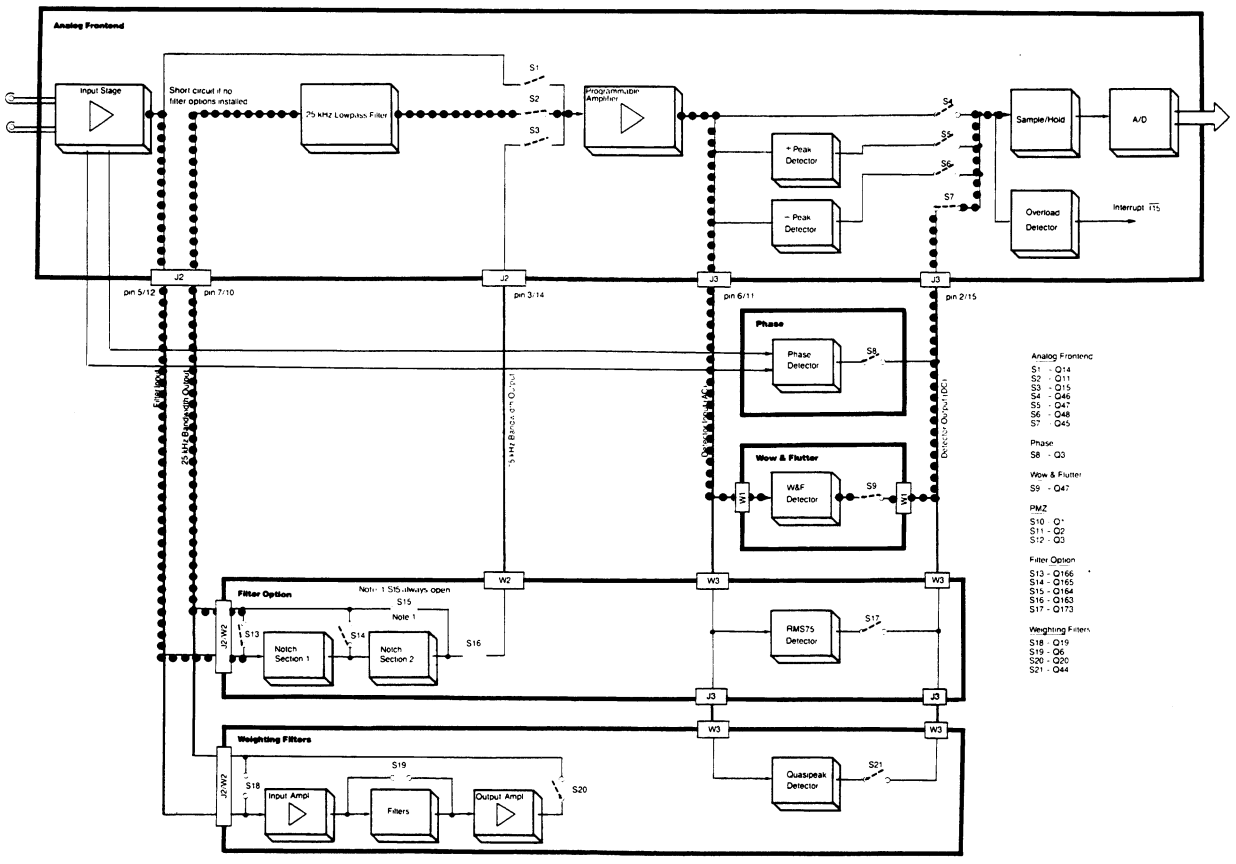


Fig. 2.11 - Wow & Flutter Measurements

3 CIRCUIT DESCRIPTIONS

3.1 Interconnections

The RE201 is divided into three main sections:

* Analog Section, comprising all analog preprocessing of the input signals (non-shielded, as no EMI is created)

* Digital Section, comprising all digital processing hardware, including the interface to the IEEE488 Bus (shielded, as EMI is generated by the digital circuitry)

* CRT Section (shielded to avoid interference from the line frequency of the CRT display).

The main element in the mechanical construction of the RE201 is an aluminium Base Plate, onto which all three separate sections are fixed. Directly into this Base Plate all pi-filters employed for filtering of connections in/out of the shielded sections (Digital Section and CRT Section) are mounted to obtain the best filtering. Furthermore, the shield of the coaxial wires is connected to this structure via the connectors.

One of the design goals for the RE201 has been to minimize the wiring in order to reduce complexity and increase reliability. Flat cables are used when possible, motherboards are used for both the Analog and the Digital Sections etc. The number of separate wires interconnecting various assemblies is thus kept at a minimum.

The Top Level Interconnections and Block Diagram at the rear of this manual (drawing No. 985-217) depicts all interconnections in the RE201. Fig. 3.1.1 shows a bottom view of the RE201, from which the locations of individual pi-filters and coaxial cables may be identified.

Grounding

The main principle applied to the RE201 grounding is the star point structure. The star point joining the separate analog and digital ground systems is located at the A/D Converter on the Analog Frontend Board of the Analog Section. Throughout the Analog Section, no connections are made elsewhere between the two ground systems. This ensures an increased noise immunity for the analog circuitries.

The Digital Section is grounded to the Base Plate, which then establishes the ground connection between the Analog and the Digital Section. In order to achieve the best transmission path for the Start Conversion clock signal, generated in the Digital Section (on the

Arithmetical Unit), to the A/D Converter in the Analog Section, the ground connection for the entire Digital Section is established from the Digital Motherboard as close to the driving buffer for this signal as possible.

The ground for the CRT Section is identical to the Digital Section ground.

The Memory Bus Interface, the GPIO and the DC inputs are all referenced to the same ground system as the measuring circuitry, i.e. the structure of the instrument, which in turn is connected to safety ground via the mains input receptacle. A break of this ground connection jeopardizes nearly all measurements due to ground loops and increased hum.

The input voltage to the Switch Mode Power Supply, coming from a rectifier located at the Linear Power Supply, has a separate return wire, as the ground for the input voltage is not identical to the system ground. The two supply wires are twisted to minimize electromagnetical emission.

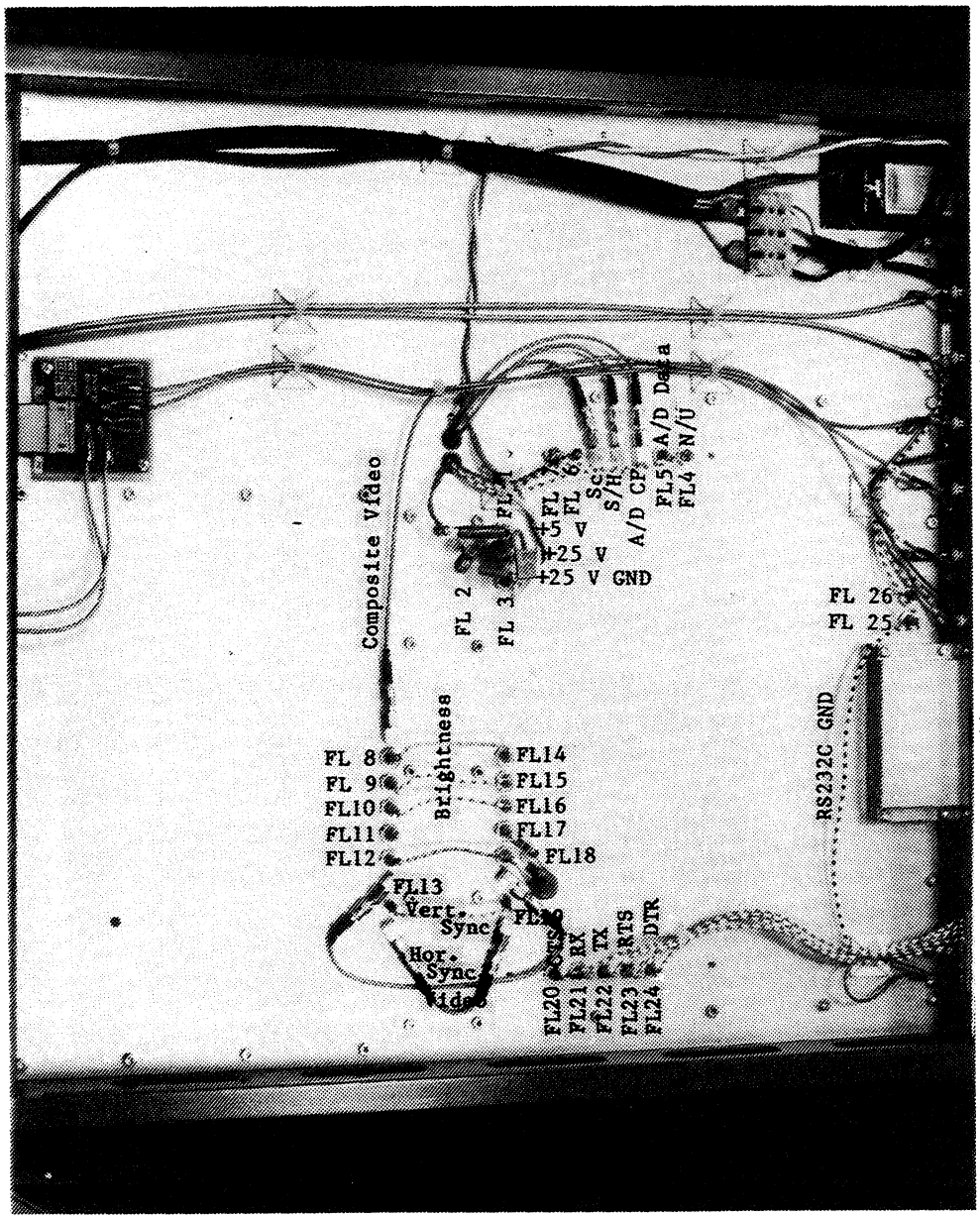


Fig. 3.1.1 - Interior Bottom View

3.2 Analog Section

The Analog Section of the RE201 is located to the right of the instrument (when viewed from the front). Contrary to the Digital Section, no shielding is employed, as the digital circuits included in this section are kept 'static', i.e. no clock is running, during periods of measurements. Hereby, the noise floor is effectively reduced to allow sensitive measurements, such as THD with a dynamic range better than 100 dB.

The main functions of the Analog Section are:

* to condition the analog input signals before the analog-to-digital conversion (autoranging, filtering etc.)
* to employ analog detectors where applicable
* to generate audio test signals (if Audio Generator is installed)
* to handle user inputs from the keyboard
* to operate the Memory Bus and the GPIO
* to perform DC measurements
* to provide the instrument with +/-15 V power supplies for the analog circuitry and with a rectified DC supply voltage for the Switch Mode Power Supply in the Digital Section.

In addition to this, the microprocessor in the Analog Section (the Static CPU) handles execution of LEARN MODE and stores all user definitions.

3.2.1 Analog Section Configuration

Most of the printed circuit boards of the Analog Section are positioned in a print magazine, into which the PCB's are inserted by means of PCB guides. The print magazine and the Analog Motherboard are fixed together in order to ease dismantling of this assembly.

The Analog Motherboard provides interconnections between the boards in the Analog Section. However, in order to obtain optimal separation between the digital and the analog signals, the analog signals are routed in flat cables on top of the PCB's.

The following PCB's are placed in the analog print magazine:

* Analog Frontend
* Static CPU
* Audio Generator, 2 PCB's (Option)
* Filter Option
* Weighting Filters (Option)
* Wow and Flutter (Option)

It should, however, be noted, that due to the limited number of slots, it is not possible at the same time to have all the above mentioned options installed, as only four slots are dedicated to options.

In addition to the boards in the print magazine, four PCB's are mounted separately:

* Interconnection Board
* Keyboard
* Linear Power Supply
* I/O & Memory Bus Interface

The Interconnection Board, part No. 901-403, is mounted beneath the Base Plate. The purpose of the board is to connect the front and the rear inputs. A flat cable feeds the input signals from the Interconnection Board to the Analog Frontend.

The Keyboard PCB, part No. 901-410, into which the pushbuttons of the Front Panel keypad are directly inserted, is mounted on the Front Panel Structure. The connections to the Static CPU, which monitors the keyboard, are provided by a flat cable connecting the keyboard to the Analog Motherboard; the connector on the Analog Motherboard is located beneath the fan.

The I/O & Memory Bus Interface, part No. 901-407, and the Linear Power Supply, part No. 901-406, are mounted on top of each other at the rear end of the RE201 below the Mains Transformer. The Linear Power Supply at the bottom connects directly to the Analog Motherboard. The I/O & Memory Bus Interface, which is mounted on stands on the Linear Power Supply, has a flat cable connection to the Analog Motherboard.

The location of the various PCB's (except the Interconnection Board) is shown in fig. 3.2.1.

In the following sections detailed descriptions of each of the PCB's are given. The options are described in the separate technical manuals.

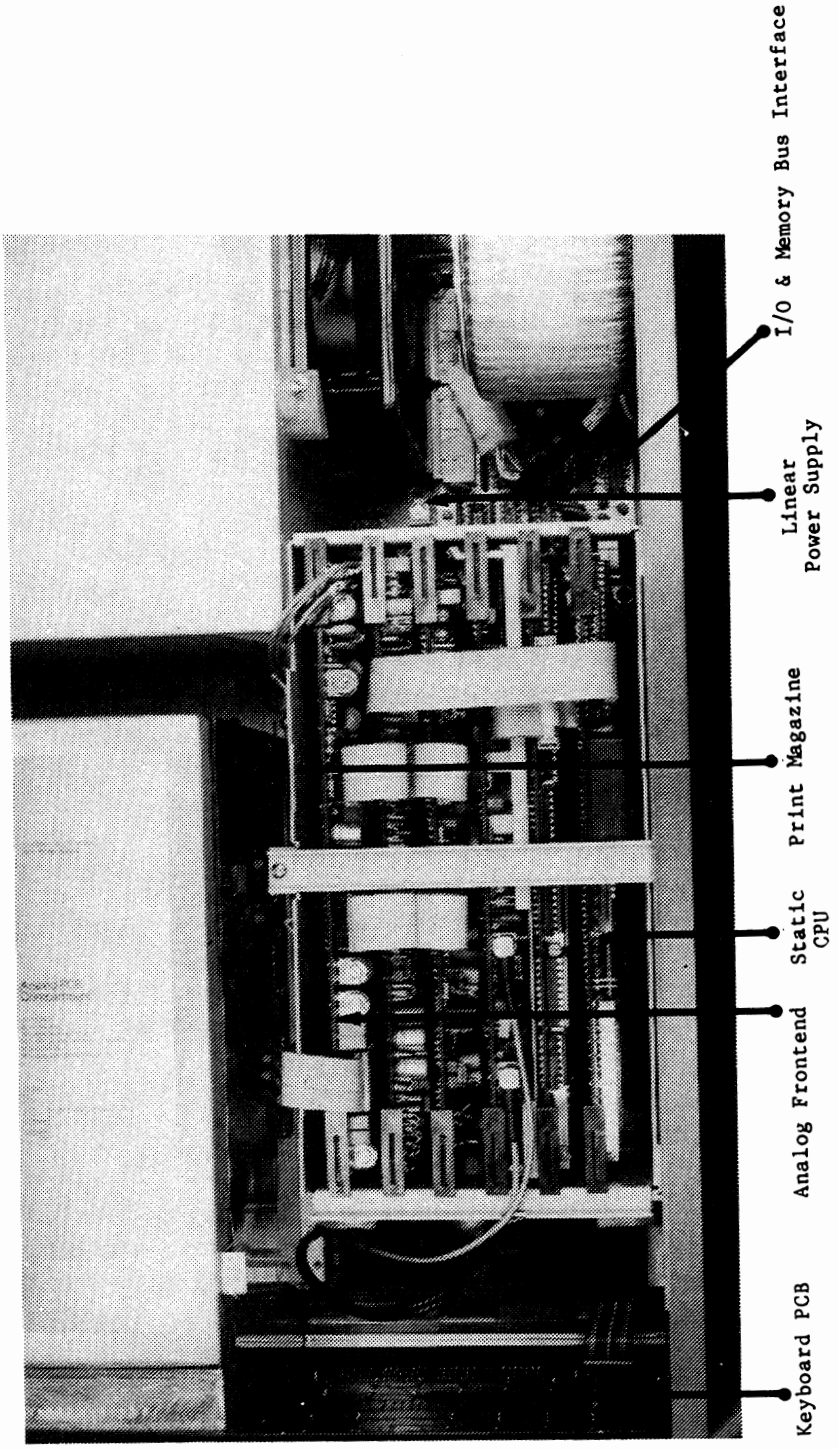


Fig. 3.2.1 - Analog Section Board Positioning

3.2.2 Static CPU 901-788

The tasks of the RE201 Static CPU are mainly three:

* Servicing of the keyboard(s)
* Setup of Analog Boards
* Execution of LEARN MODE

In addition to this, the Static CPU controls the GPIO and Memory Bus Interfaces and the DC measurements.

As the Static CPU is located in the unshielded part of the RE201, a special technique has been employed in order to avoid EMI (Electromagnetic Interference): Whenever the CPU is not performing any of the above mentioned tasks, the CPU clock oscillator is stopped, thus making the circuitry "static". All measurements are performed by the Main Computer located in the shielded compartment, while the Static CPU is held in Static Mode. If service is needed, e.g. because the keyboard is activated, the clock is restarted and the CPU activated.

The CPU is a 16 bit microprocessor with 8 bit external data bus, the TMS 9995 from Texas Instruments. Pin description is given in table 3.2.1 for reference.

Referring to the block diagram, fig. 3.2.2, and the schematic diagram 985-251 at the rear of this manual, the main parts of the Static CPU are:

* Computing Unit, QD1, with associated clock and timing circuitry

* Memory

* Input/output interface

Clock and Reset Circuitry

The clock signal for the CPU is generated by an external crystal oscillator, which can be turned on/off. The clock frequency is 12 MHz, which - divided by four by the CPU - gives a processor clock cycle time of 333 ns. The processor clock is available as output CLKOUT from the CPU chip.

On power-up, a RESET pulse is generated by R14, C4 and QD17 (Schmitt trigger device). This causes the CPU to perform a master reset and reinitialize all devices.

When the CPU has finished all pending tasks, it enters the Static Mode by pulsing the CLKOFF signal (QD6, pin 13), thus disabling the clock oscillator immediately and activating the RESET for the CPU.

Signal	Pin	In/Out	Description
			Power Supplies & Clock
Vcc	10		Supply voltage (+5V)
Vss	31		Ground
XTAL2/CLKIN	2	IN	Input pin for external oscillator (12 MHz)
XTAL1	1	IN	Crystal input pin for internal oscillator (not used)
CLKOUT	3	OUT	CLOCK OUTPUT SIGNAL: The frequency of CLKOUT is one fourth the oscillator input frequency (3 MHz).
			Address Bus
A0	24	OUT	A0 is the most significant bit of the 16 bit Memory Address Bus and the
A1	25	OUT	15 bit CRU Address Bus. A14 is the 2nd least significant bit of the 16
A2	26	OUT	bit Memory Address Bus and the LSB of the 15 bit CRU Address Bus.
A3	27	OUT	
A4	28	OUT	
A5	29	OUT	
A6	30	OUT	
A7	32	OUT	
A8	33	OUT	
A9	34	OUT	
A10	35	OUT	
A11	36	OUT	
A12	37	OUT	
A13	38	OUT	
A14	39	OUT	
A15/CRUOUT	40	OUT	Address bit 15/CRU output data
			Data Bus
D0	12	I/O	During memory cycles, D0-D7 are used to transfer data to/from memory.
D1	11	I/O	During non-memory cycles, D0, D1 and D2 are used to distinguish between
D2	9	I/O	CRU operation and external instructions (all low for CRU operations).
D3	8	I/O	
D4	7	I/O	
D5	6	I/O	
D6	5	I/O	
D7	4	I/O	
			Bus Control
$\overline{\text{MEMEN}}$	20	OUT	MEMORY ENABLE: When active, $\overline{\text{MEMEN}}$ indicates that $\overline{\text{WE}}$/$\overline{\text{CRUCLK}}$, $\overline{\text{DBIN}}$ and the Address and Data Buses are being used for a memory cycle. When inactive, $\overline{\text{MEMEN}}$ indicates that $\overline{\text{WE}}$/$\overline{\text{CRUCLK}}$, $\overline{\text{DBIN}}$ and the Address and data Buses are being used for a CRU cycle or an external instruction.
$\overline{\text{DBIN}}$	17	OUT	DATA BUS IN: During memory read cycles, $\overline{\text{DBIN}}$ is active to indicate to other devices, that data may be put on the bus. During CRU input cycles, $\overline{\text{DBIN}}$ is also active to indicate that the CRU cycle is an input cycle.
$\overline{\text{WE}}$/$\overline{\text{CRUCLK}}$	19	OUT	WRITE ENABLE/CRUCLK: When active, $\overline{\text{WE}}$/$\overline{\text{CRUCLK}}$ indicates that memory data is available on the Data Bus or that CRU data is available on A15/CRUOUT or that an external interface should decode external instructions.
CRUIN	13	IN	CRU INPUT DATA: During CRU cycles, CRUIN is the input data line for CRU input data.
READY	23	IN	READY: When active, READY indicates that the present memory, CRU or external instruction cycle is ready to be completed; otherwise Wait States are inserted until READY goes high.
			External Control
$\overline{\text{HOLD}}$	18	IN	HOLD: Not used
IAQ/HOLDA	16	OUT	INSTRUCTION ACQUISITION/HOLD ACKNOWLEDGE: If IAQ is active when $\overline{\text{MEMEN}}$ is active, the memory read cycle in progress is that of reading an instruction opcode. Not used for Hold Acknowledge.
$\overline{\text{RESET}}$	22	IN	RESET: When active, $\overline{\text{RESET}}$ causes TMS 9995 to enter a RESET state and inhibit $\overline{\text{MEMEN}}$, $\overline{\text{DBIN}}$ and $\overline{\text{WE}}$/$\overline{\text{CRUCLK}}$.
$\overline{\text{NMI}}$	21	IN	NON-MASKABLE INTERRUPT: Not used.
$\overline{\text{INT1}}$	15	IN	INTERRUPT 1: Not used.
$\overline{\text{INT4}}$/$\overline{\text{EC}}$	14	IN	INTERRUPT 4/EVENT COUNTER: Not used.

Table 3.2.1 - TMS 9995 Pin Assignments and Functions

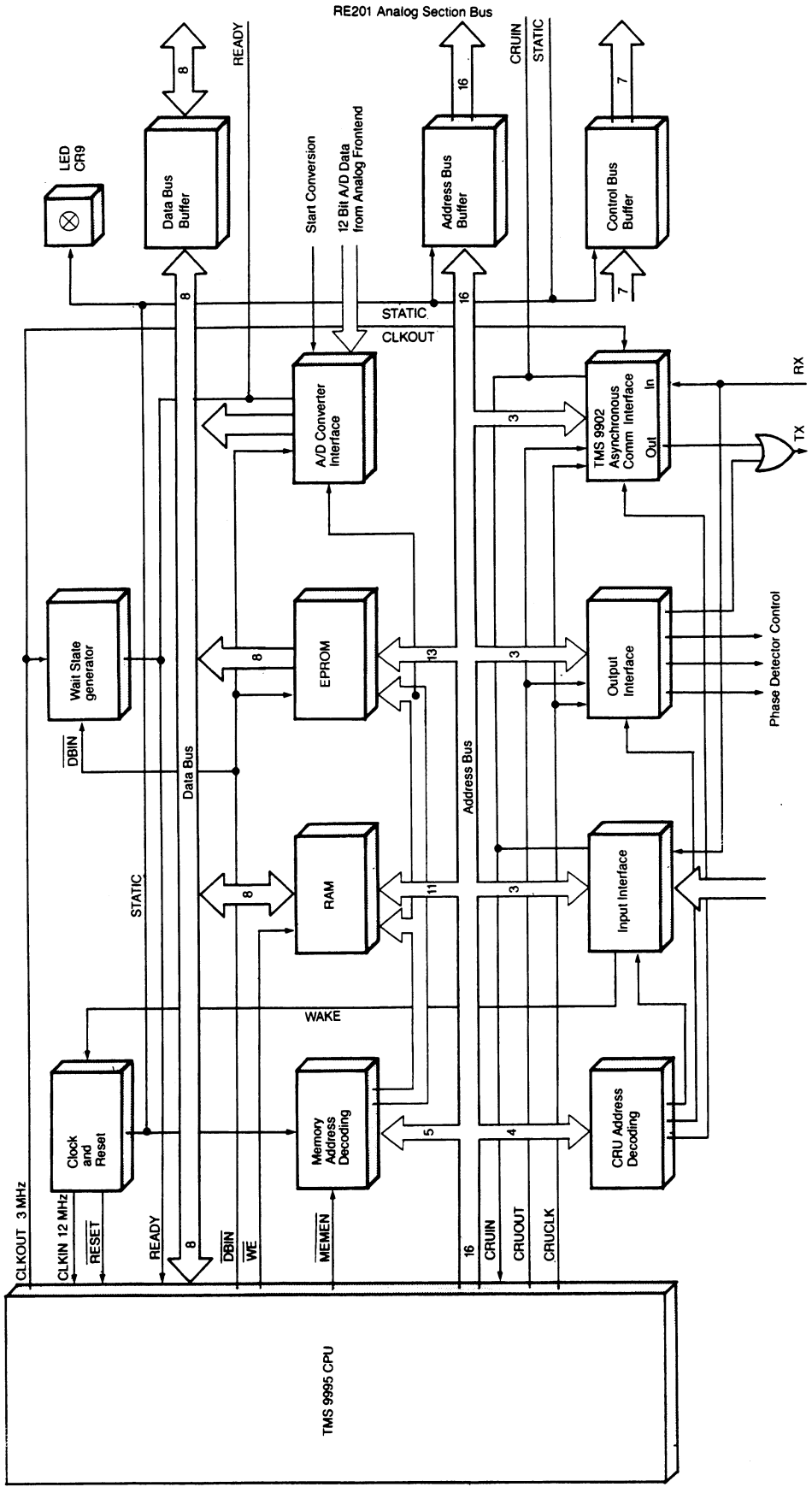


Fig. 3.2.2 - Static CPU Block Diagram

As this stops all activity in the digital circuitry, a major contributant to electromagnetic interference is eliminated. When a WAKE condition occurs (QD32, pin 13 high), the flip-flop QD10 is preset. The clock oscillator starts immediately, but release of RESET is delayed by R12 and C3. This ensures the proper start condition for the CPU, as the CPU is clocked for a period before RESET goes high.

The procedure for start after a power-on reset and from Static Mode are essentially identical, however, the power-up latch QD10 enables the CPU to detect which condition has occurred.

If the TMS 9995 were to run at full speed, it would require memory with an access time of 100 ns. To operate the EPROM memory circuits actually used, one Wait State is inserted, extending the bus cycle by one CLKOUT cycle (333 ns). As access to certain memory parts may be done without any waitstate inserted, the Automatic First Wait State generation feature of the TMS9995 is disabled by holding the signal at low level during release of the RESET-signal.

Wait states are thus controlled from the wait state generator circuitry.

Memory

Internally, the TMS 9995 operates with 16 bits. However, for external operation these 16 bits are divided into bytes (8 bits), meaning that the Data Bus is only 8 bit wide; 16 bit data words are accessed by two consecutive bus transfer operations. The Address Bus is 16 bits wide, thus allowing addressing of 64 kbytes of memory.

To perform a memory read operation, the TMS 9995 first outputs the appropriate address on AØ-A15 and asserts MEMEN. Then the CPU puts its data bus drivers in the high impedance state, asserts DBIN whereupon the data byte is read. Timing relationships of the memory read sequence with one Wait State inserted are shown in fig. 3.2.3. Most memory accesses involve a transfer of a word, i.e. two byte transfer cycles. As words are always stored on consecutive byte locations in memory, A15 (LSB) distinguishes between transfer of the two bytes of a data word: when A15 is low (even addresses), Most Significant Byte is transferred, when A15 is high (odd addresses), Least Significant Byte. The MEMEN signal remains active (low) between consecutive memory operations, whereas DBIN is asserted twice for word transfers.

Memory write operations are performed in a similar way: the TMS 9995 first outputs the appropriate address on A0-A15 and asserts MEMEN. Then the data byte being written to memory is presented on pins DØ-D7, and the CPU asserts WE. Timing relationships of the memory write cycle are also shown in fig. 3.2.3.

The READY signal, which allows extended memory cycles, is also shown on fig. 3.2.3. If READY is low at the falling edge of CLKOVT during a memory cycle, the CPU extends the memory cycle by one clock cycle (CLKOUT). This is repeated until READY is high at the falling edge of CLKOUT, indicating the end of the memory operation.

The memory for the Static CPU is composed of 64 kbytes of EPROM two 32Kx8 27C256 (QD34-QD35), and 16 kbytes of RAM two 8Kx8 TC5565 (QD36-QD37). The EPROMS are used for the program (software)

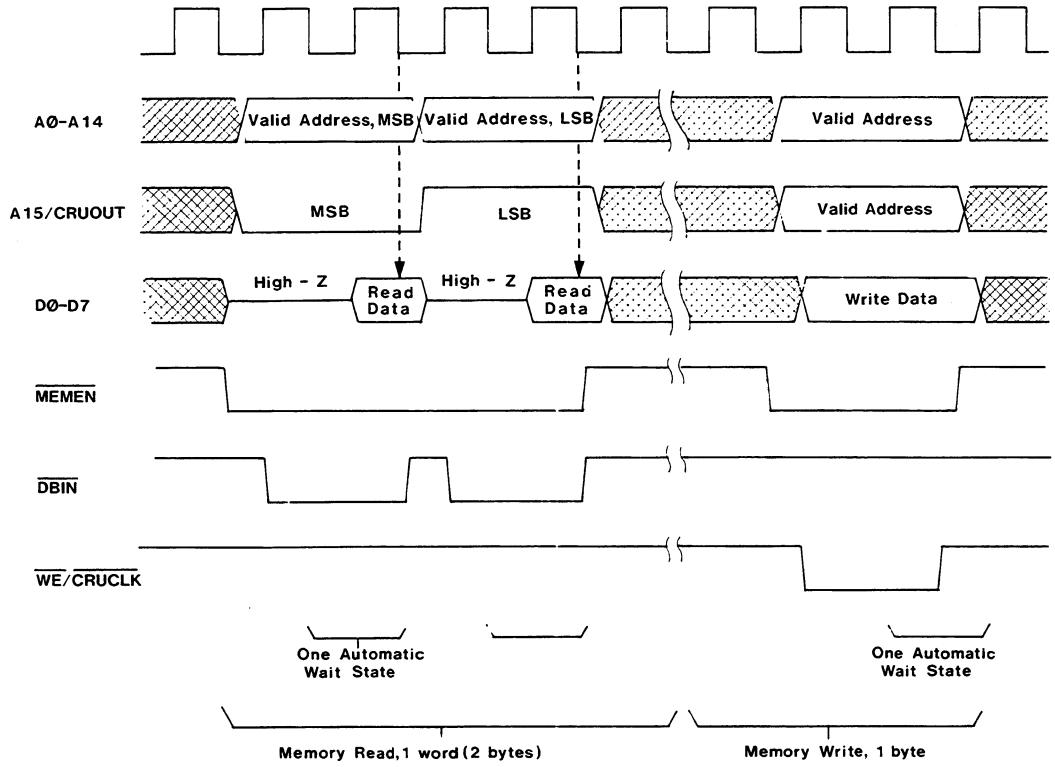


Fig. 3.2.3 - TMS 9995 Memory Timing

and the RAM's are used partly for housekeeping purposes, partly for the different definitions made by the user.

The circuitry configured around Q1 and Q2 enables battery power for the RAM's during periods of power-down. In this way, data are retained when the +5 V supply is missing. By means of the jumper K4, battery power may be removed during long term storage in order to avoid complete discharge of the battery.

The address decoding for the memory is performed by a PAL (QD18).

A/D Converter Interface

The CPU is able to obtain readings from the A/D Converter via the buffers QD26-QD27. The connector J2 at the top of the board is used to

input the 12 bit data from the Analog Frontend. The interface to the A/D Converter is memory mapped, i.e. the CPU reads the data buffers just as any memory location. The LSB address bit A15 is used to enable the transfer of the 12 bit data words from the A/D Converter to the 8 bit bus of the CPU: When A15 is low, the eight most significant bits are transferred, and when A15 is high, the four remaining bits are transferred as the four most significant bits of this byte, while the remaining four bits are held low. Thus, the CPU reads the 12 bits into a 16 bit data word, with the four least significant bits always zeroed.

To avoid reading of the A/D Converter during the conversion cycle the reading is synchronized to the Start Conversion signal used by the converter by insertion of an appropriate number of wait states. This is accomplished by a circuitry configured around two flip-flop's (1/2 QD11, 1/2 QD12). One flip-flop (QD11) is used to synchronize Start Conversion ($\overline{SC}$) to the processor clock, CLKOUT, in order to fulfill the setup-time requirements for the READY input to the CPU. When the CPU tries to read MSB of the A/D data from the buffer QD27, READY is pulled low by QD19, pin 3 - the inputs to this NAND-gate are both high, pin 1, because QD27 is being addressed, pin 2, because the flip-flop QD11 has been cleared at the end of a previous read operation, when LSB of the A/D data is read from QD26. READY is released when $\overline{SC}$ goes low, i.e. just before a new conversion is instigated. As the CPU then reads within 1 micro sec., the A/D Converter value will not change during the read cycle.

CRU Operations

The TMS 9995 may accomplish bit-wise input/output through the use of the Communications Register Unit (CRU), which is used for all control purposes, e.g. setup of analog circuits. Acting as a serial bus, the CRU can in a single operation transfer from one up to 16 bits of data between the CPU and a specified device, selected by means of the Address Bus. Except from the Address Bus the CRU operates three signals:

* CRUIN, used for bit input
* CRUOUT, used for bit output
* CRUCLK, used as synchronization clock for bit outputs.

The same output pin of the TMS 9995 is used for $\overline{WE}$ and $\overline{CRUCLK}$, since $\overline{WE}$ only is used during memory cycles, and $\overline{CRUCLK}$ only during CRU cycles. Furthermore, as only 15 address bits are valid during CRU operations, A15 and CRUOUT share the same output pin.

To input a data bit from an external device, the TMS 9995 first outputs the appropriate address on A$\emptyset$-A14, then leaves $\overline{MEMEN}$ high - indicating a CRU cycle -, strobes $\overline{DBIN}$ and reads in the data bit on CRUIN. Completion of a CRU input cycle or generation of Wait States is determined by the READY input. QD11 prolongs bus cycles for

CRU operations by one Wait State. Timing relationships of the CRU input cycle are shown in fig. 3.2.4.

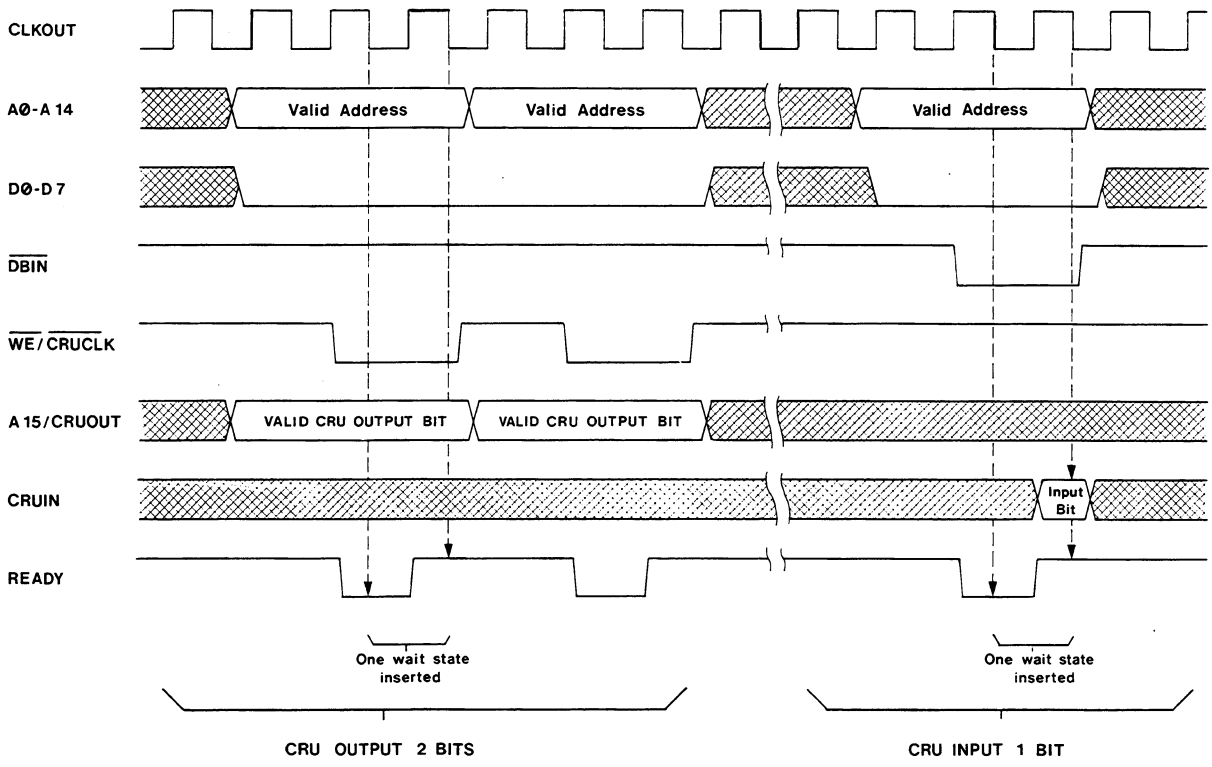


Fig. 3.2.4 - TMS 9995 CRU Interface Timing

To output a data bit to an external device, the TMS 9995 first outputs the appropriate address on AØ-A14, then leaves MEMEN high, outputs the data bit on CRUOUT, and strobes CRUCLK. As for CRU input cycles, one Wait State is generated by QD11. Timing relationships of the CRU output cycle are also shown in fig. 3.2.4.

For multiple bit transfers, these input cycles (output cycles, respectively), are repeated until transfer of the entire field of data bits has been accomplished.

Main Computer Interface

Communication with the Main Computer is provided by means of a tree-wire link, one receive line, one transmit and one handshake line. This interprocessor link is a serial asynchronous interface similar to the EIA RS232C standard, except that the levels are TTL. Acknowledge messages are exchanged under software control.

Every transmission from the Main CPU is commenced by the Main CPU pulling the handshake line from high to low level; this transition is latched by QD12 and used to wake up the Static CPU.

The interface is implemented by means of a TMS 9902 Asynchronous Communications Controller from Texas Instruments (QD14). Communication between the CPU and the TMS 9902 is accomplished by the CRU interface.

Input Interface

Eight input lines may be scanned by the CPU by means of QD30. They are used as follows (active low):

Pin 1: Power-up
Pin 2: Main Computer Interrupt
Pin 3: Not used
Pin 4: Internal Keyboard Activated
Pin 5: External Keyboard Activated
Pin 6: Wow and Flutter Option Present
Pin 7: Option detect (used by Audio Generator, Filter Option and Weighting Filters)
Pin 9: Overload occurred in Analog Frontend

The occurrence of a condition for restarting the CPU from Static Mode, supplemented by the power-up reset, is monitored by QD32. A WAKE signal, terminating the Static Mode, is generated by any of these four devices:

* Internal Keyboard
* External Keyboard
* Main Computer
* Analog Frontend Overload Detector

Output Interface

The CPU controls eight output lines (QD28), out of which one is used for the interprocessor communication to keep the transmit line inactive (high) during the static periods, and three are used for control of the phase measuring circuitry (refer to section 3.2.4 for details).

Eight LED's (CR1 - CR8) are controlled by the CPU. They are used for error code display during selftest and otherwise for status display. For interpretation of the codes, please refer to section 5.2.1. One additional LED, CR9, is lit whenever the CPU is active (Non-Static).

Bus Interfaces

As the Static CPU is the controller of the Analog Section, it must communicate with several other circuits. The communication takes place via the Analog Motherboard. To avoid fan-out problems, the CPU

busses - address, control and data - are buffered towards the Analog Motherboard (QD2-QD5).

Interface to memory circuits located on other boards is included in order to communicate with options boards holding programme information, and to access the RAM circuits of the Audio Generator (refer to the Technical Manual for this option).

CRU is used for all other interfaces, including the control of the GPIO and the Memory Bus. To hold the information concerning setup of analog circuits, an HEF4724 8 bit addressable latch located close to the circuit to be controlled (e.g. on Analog Frontend or Audio Generator option) is used in most cases.

Jumpers

The locations of jumpers and test points are shown in fig. 3.2.5. A list of their use is given below:

K1: Not used (open)
K2: Not used (short circuit)
K3: Simulated power-up reset if short-circuited
K4: 1-2 Battery backup enabled
2-3 Save battery during long-term storage
K5: MSB of address TD QD34. Prestrapped to +5V for use with 27C256.

Test Points

The Test Points listed below are mainly incorporated for use at the factory.

TP1: +5V
VBAT
+20V
-20V

TP2: $\overline{CE1}$ (QD34)
$\overline{CE2}$ (QD35)
CE3 (QD36)
CE4 (QD37)

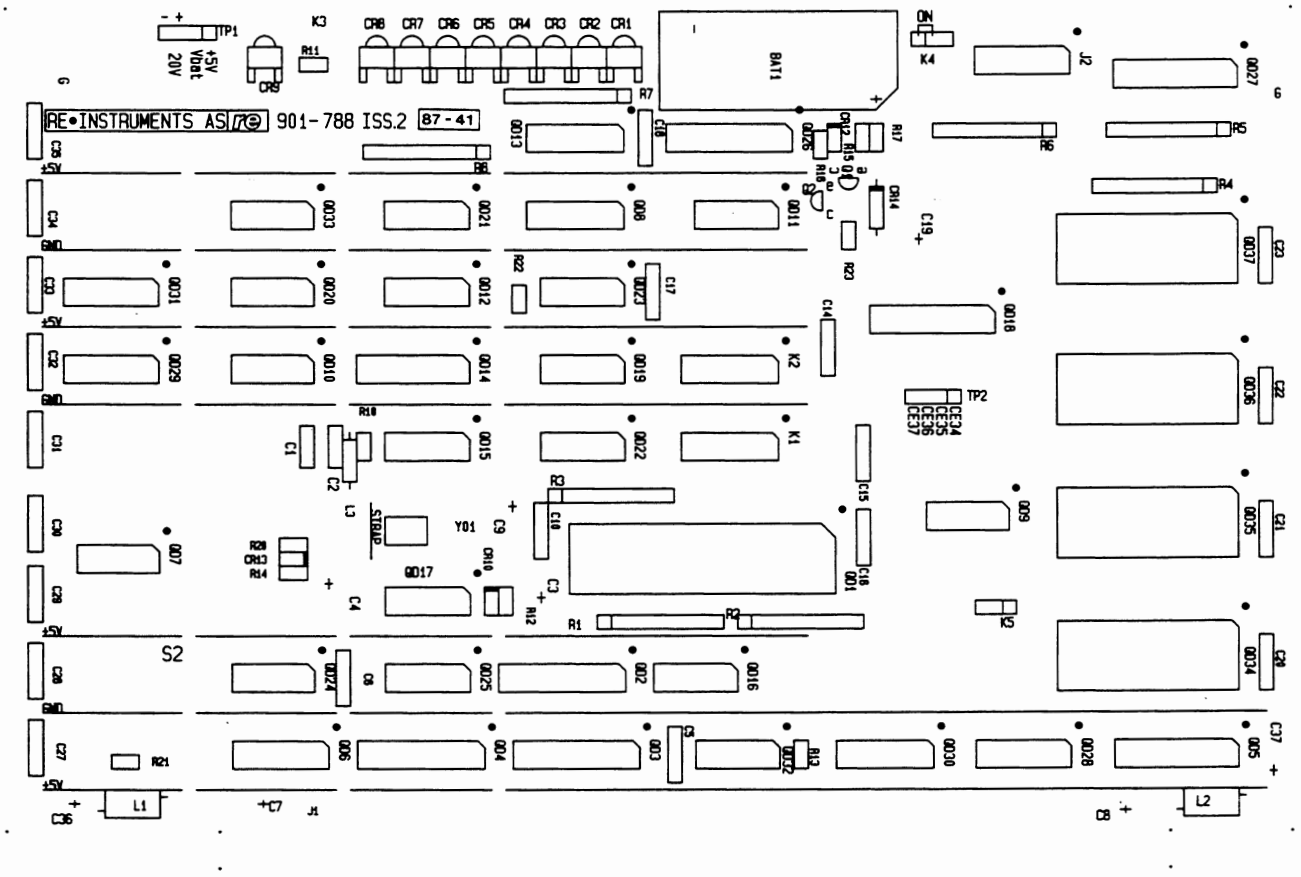


Fig. 3.2.5 - Static CPU Component Layout

3.2.3 Analog Frontend 901-421

The main purpose of the Analog Frontend is to condition the analog input signal before it is digitized. This conditioning involves amplification/attenuation and frequency limiting. As the dynamic range of a digital instrument is dependent on the number of bits used in the Analog-to-Digital conversion, it is essential that the full input range of the A/D Converter (+/-2.5 Vpeak) is utilized. Therefore, one of the major tasks of the Analog Frontend is to ensure, that the signal at the input of the A/D Converter always has a peak voltage close to the maximum value. On the other hand it is important to ensure that the maximum voltage is not exceeded, as this will cause distortion and measurement errors.

The frequency conditioning (lowpass filtering) is necessary to ensure that the sampling theoreme is obeyed, i.e. the sampling frequency must be at least two times the highest frequency component in the sampled signal. If the sampled signal does not fulfill this fundamental requirement, so-called aliased frequency components will appear within the baseband spectrum. These frequency components cannot be removed after sampling and will cause measurement errors.

In the RE201 the base band is the audio frequency range 0 Hz-25 kHz. Thus the frequency conditioning filter must be flat up to above 25 kHz and reject all frequency components above 39 kHz (64 kHz-25 kHz).

Furthermore, the Analog Frontend includes Peak detectors, which are used for peak measurements and during the autoranging procedure.

The block diagram of the Analog Frontend board is shown fig. 3.2.6 while the schematic diagram is shown in drawing No. 985-099.

Input Stage

The input stage consists of two identical instrumentation amplifiers - one for each channel - (QA1-QA6), which provides high impedance differential inputs. A relay-driven 20 dB attenuator in front of these amplifiers provides handling of input signals with peak amplitudes reaching 25V. Input protection for peak amplitudes up to 50 V is provided by diodes CR7-CR14. The input amplifiers are followed by a channel selector (Q1-Q2). For phase measurements, the outputs from both instrumentation amplifiers are used.

Anti-aliasing Filter

The anti-aliasing filter is a 9th order elliptical LP-filter having a 0.1 dB upper frequency at 25 kHz, reaching -85 dB at 41 kHz, in order to attenuate aliasing components.

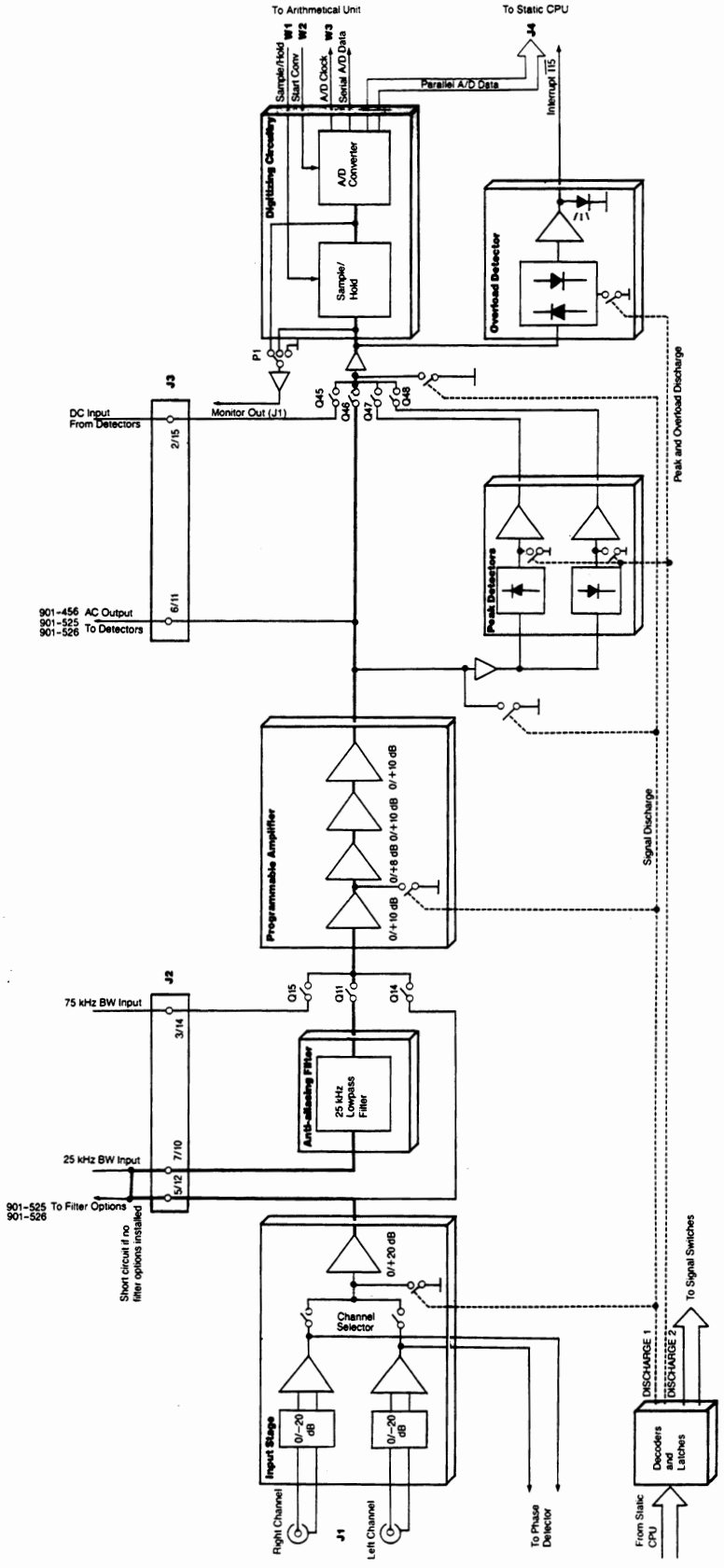


Fig. 3.2.6 - Analog Frontend Block Diagram

The filter has been implemented using FDNR's (Frequency Dependent Negative Resistance) in order to eliminate problems related to conventional inductors, such as large size, low Q, non-linearity, etc.

In order to perform measurements in 75 kHz bandwidth using analog detectors, it is possible to bypass the filter by setting FET-switch Q14 'ON' instead of Q11. Q15 selects input from filters located on option boards.

Gain Section

Five computer controlled amplifiers (QA7, QA17-QA20) enable setting of any gain from 0 to +58 dB in steps of 2 dB. Gain values in the range -20 to 0 dB are achieved by activating the relay of the input stage, giving -20 dB attenuation. To improve noise behavior, the gain section has been divided in two, as a 20 dB amplifier is placed in front of the anti-aliasing filter. The filter comprises a large number of operational amplifiers, which would reduce the overall noise performance if not preceded by a low noise amplifier The gain is selected by means of FET-switches Q3, Q4 and Q20-Q27, controlled by the computer interface. This interface is configured of addressable latches which can be loaded by the Static CPU.

Peak Detectors

The Peak Detectors used for peak measurements and for autoranging (QA23, QA25) are built using LM311 voltage comparators to obtain high performance detectors. Both peak detectors are buffered using TL084 BIFET op-amps (QA21). The outputs from the peak detectors are routed to the S/H amplifier using FET switches (Q47, Q48) when peak measurements are being performed.

Overload Detector

In order to ensure that the input signal does not overload the A/D converter, a full wave rectifier (QA22) is used for overload detection. When the voltage applied to the Sample/Hold amplifier is in excess of 2.4 V peak, the overload LED CR21 is activated and $\overline{I15}$ goes low, informing the Static CPU of the overload condition.

Digitizing Circuitry: Sample/Hold and A/D Converter

The purpose of the Sample/Hold amplifier QA26 is to keep the value of the input signal constant while A/D conversion is in progress. The output from the S/H amplifier represents a value of the signal at a precisely known time. During the "sample" period, an internal switch of the amplifier is closed, and the input signal is fed to the hold capacitor. In "hold" mode, the switch is opened, and the voltage over the capacitor is held during the A/D conversion. In this way signals having large dV/dt's may be digitized without loss of accuracy. The Sample/Hold control signal is generated by the

Arithmetical Unit in the Digital Section and transmitted in a coax cable (W1).

The A/D converter is a 12 bit successive approximation converter with a conversion time of 10 micro sec. The 12 bits are routed in parallel format to the Static CPU via a flat cable, connecting to J4, and in serial format to the Arithmetical Unit in the Digital Section. A synchronization clock, generated by the A/D Converter, is transmitted in a coaxial cable (W3). The Start Conversion signal is delivered from the Arithmetical Unit via the coaxial cable W2.

Discharge

Whenever abrupt signal changes occur in analog circuitry, e.g. due to signal switching, capacitors will be charged/discharged and glitches may be generated. Before such transients have decayed, sensitive measurements cannot take place; further, unintended overload interrupts might be generated, disturbing the execution of measurements. In order to minimize the probability of occurrence of glitches and to shorten the settling time for the signal after switching, all AC coupling capacitors are discharged during signal switching. The discharging is accomplished by means of FET-switches, clamping one end of the capacitor to ground. Prior to any signal switching or change of gain, the Static CPU first closes these switches, hereby clamping the signal to ground while switching takes place. Discharging switches are included for every AC-coupling capacitor. One control signal, DISCHARGE 1, which may be activated by the Static CPU, enables all signal discharge switches.

In addition to this, a means for "reset" of the peak detectors and the overload detector is provided, controlled by the signal DISCHARGE 2.

Monitoring Buffer

To enable monitoring of the signals reaching the Sample/Hold amplifier and the A/D converter, a buffer amplifier is included which may be connected to the signal before or after the Sample/Hold amplifier (selectable by means of the jumper P1). The output from the amplifier is via the flat cable connecting to J1 routed to the Interconnection Board at the bottom of the instrument.

Interface to Other Boards

Reference is made to the Top Level Interconnection and Block Diagram at the rear of this manual (drawing No. 985-217), as well as to the Analog Frontend Block Diagram, fig. 3.2.6.

The analog input signals coming from the Interconnection Board, located beneath the Base Plate, enter the Analog Frontend by means of a flat cable, connecting to J1, located at the top of the board to the left. The location of J1 is shown in fig. 3.2.7.

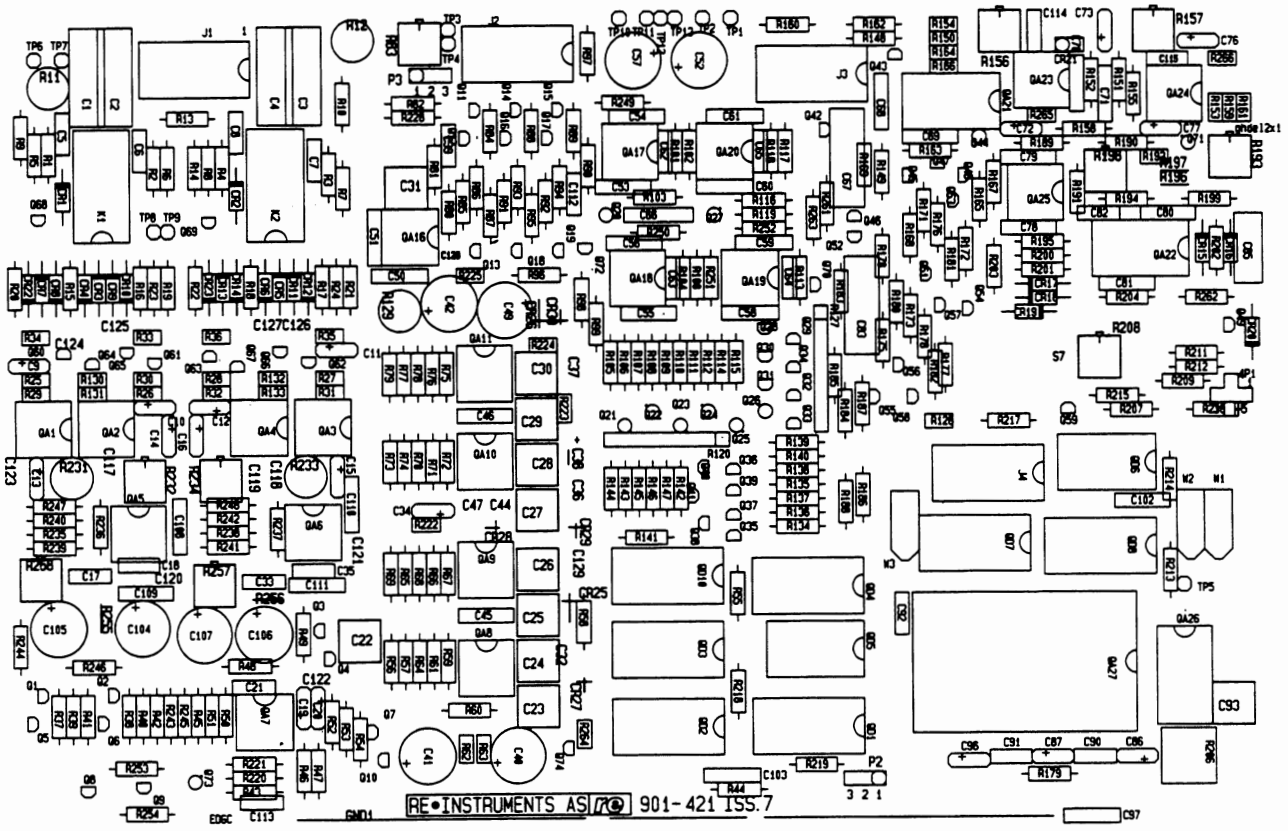


Fig. 3.2.7 - Analog Frontend Component Layout

All analog interfaces to option boards are routed in flat cables connecting to the top of the Analog Frontend (J2 and J3). Input from option boards is selected by means of FET switches under software control (Q15 and Q45).

J2 carries the input/output signals related to the different filters which may be inserted - the notch filters of the Filter Option, and the Weighting Filters. Two filter inputs are provided, because the signal coming from the filtering options may or may not be routed through the 25 kHz lowpass filter (anti-aliasing filter) of the Analog Frontend.

J3 is used for input/output to the different analog detectors located on option boards - the RMS detector on the Filter Option, the

Quasi-peak detector on the Weighting Filters, and the Wow and Flutter detector. The output of the phase detector located on the Analog Motherboard enters the Analog Frontend by the PCB edge connector.

The parallel A/D data to the Static CPU are routed in a flat cable connecting to J4.

Jumpers

The location of jumpers and test points is shown in fig. 3.2.7.

P1: selects input to the monitoring buffer amplifier
- 1-2 Input signal to the Sample/Hold amplifier
- 2-3 Output signal from the Sample/Hold amplifier *
- 2-4 Monitoring buffer input grounded

P2: Not mounted: Sample/Hold always active *
- 1-2 Sample/Hold only active for AC input
- Other positions not used

P3: selects source for Sample/Hold control signal
- 1-2 Sample/Hold from W1 *
- 2-3 Sample/Hold from J4

From the factory, jumpers are positioned as marked with an asterisk (*).

Test Points

TP5: Start Conversion (from Arithmetical Unit)

3.2.4 Analog Motherboard 901-405

The Analog Motherboard carries the connections between the boards in the Analog Section, i.e. Data Bus, Address Bus, control signals and power lines. There are six 86 poled connectors on the Bus, one dedicated to the Analog Frontend and five general-purpose for the Static CPU and option boards. Furthermore the Analog Motherboard contains a phase detector used for phase measurements, and it provides connections for Keyboard (J11) and I/O & Memory Bus Interface (J9). The signals for the Keyboard - which are also routed to the external keyboard, RE905 - are buffered by QD3-QD4.

A block diagram showing the main blocks of the Phase Detector is found in fig. 3.2.8 while the schematic diagram and a table of the assignment of the individual bus lines are shown in drawing No. 985-100.

The Analog Section is supplied from two power supplies: The +5 V for digital circuits is supplied from the Switch Mode Power Supply in the Digital Section through connector J7, while the +/-15 V and +/-20V for analog circuits are supplied from the Linear Power Supply connected to the Analog Motherboard by J10.

Phase Detector

From the Analog Frontend input amplifiers the Right and Left Channel signals are fed through amplifiers QA1 (inverting or non-inverting amplifier selectable) to two zero-crossing detectors (QA2, QA3). The TTL output signals from these detectors clock two flip-flops which constitute the Phase Detector (QD1).

The duty-cycle of the output signal from the Phase Detector is proportional to the phase difference between the two input signals. The Phase Detector signal is integrated (QA4) and the DC voltage obtained is fed back to the Analog Frontend DC input.

The Phase Detector is controlled by three control lines from the Static Computer, P0-P2, (refer to the bus connection table in drawing No. 985-100). Non-inverting amplifiers are selected (Q5, Q11 on, respectively) by holding P0, P1, respectively, on logic one. The Phase Detector output is enabled by holding P2 on logic zero (Q3 on).

To obtain high accuracy input levels to the integrator, QD2 is supplied from a +5V reference supply (QA4).

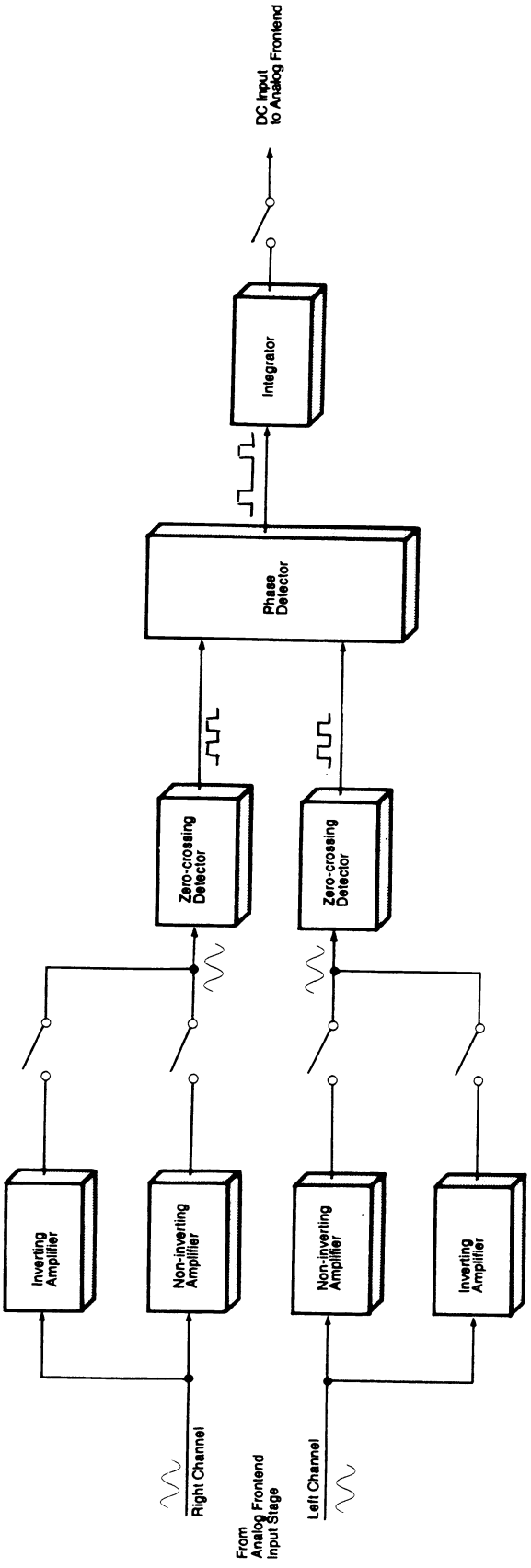


Fig. 3.2.8 - Phase Detector Block Diagram

Test Points

For test and adjustments a list of test points is given below. The location of the test points is shown in fig. 3.2.9.

TP1 : Ground for +5 V ref.
TP2 : +5 V ref.
TP3 : Ground for +5 V ref.
TP4 : Ground for outputs from input amplifiers
TP5 : Non-inverting output for Right Channel
TP6 : Inverting output for Right Channel
TP7 : Inverting output for Left Channel
TP9 : Non-inverting output for Left Channel
TP10: Ground for input signals
TP11: Right Channel Input
TP12: Left Channel Input

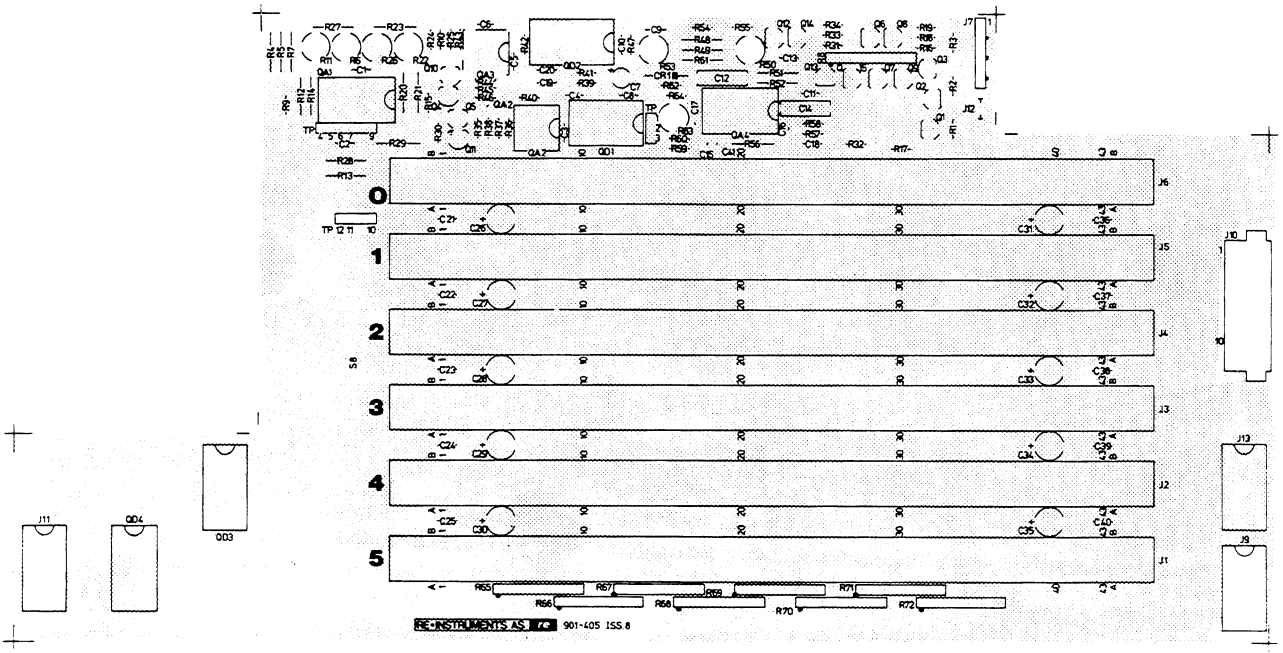


Fig. 3.2.9 - Analog Motherboard Component Layout

3.2.5 Linear Power Supply 901-406

The schematic diagram of the Linear Power Supply is shown in drawing No. 985-101.

The Linear Power Supply, which is supplied from the Mains Transformer through J1, comprises four regulated linear power supplies generating +15 V, -15 V, +20 V and -20 V to be used by the analog circuitry. The +/-20 V supplies are not used in a standard RE201 but are incorporated for further enhancements. Furthermore a +25 V unregulated DC for the Switch Mode Power Supply is included (CR2, C3 and C4).

The +/-15 V supplies are built around two LM301 (QA3, QA4), each controlling a Darlington transistor (Q2, Q7). By means of R11, R29 and Q3, Q6, the maximum current is limited to 1.5 amps. The output voltage may be adjusted by means of R2.

The +/-20 V are obtained by zener diodes (CR3, CR4) controlling transistors (Q1, Q8).

The +25 V unregulated DC for the Switch Mode Power Supply is provided via the rectifier CR4, which is mounted directly on the base plate in order to activate adequate cooling.

Test Points

The location of the test points is shown in fig. 3.2.10.

TP1: Ground
TP3: -15 V
TP4: +15 V

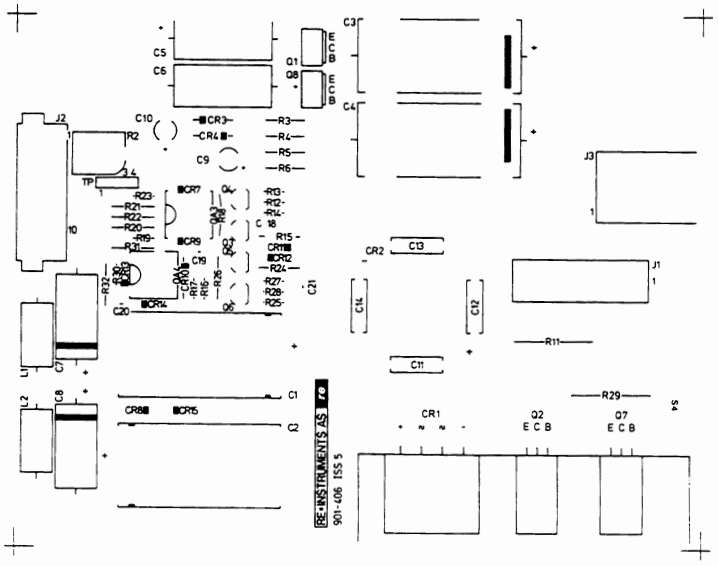


Fig. 3.2.10 - Linear Power Supply Component Layout

3.2.6 I/O & Memory Bus Interface 901-407

The I/O & Memory Bus Interface board consists of three main circuit blocks. The Memory Bus Interface, the outputs for the General Purpose Interface (GPIO) and two identical DC measurement circuits (DC1 and DC2).

A block diagram of the I/O & Memory Bus Interface is shown in fig. 3.2.11 while the schematic diagram is shown in drawing No. 985-102.

The I/O & Memory Bus Interface is mounted on top of the Linear Power Supply in the rear right corner of the RE201 below the Mains Transformer. The board is kept in place by special plastic stands on the Linear Power Supply for easy dismantling. A ribbon cable on J1 provides the connections to the Analog Motherboard. The I/O & Memory Bus Interface is controlled by the Static CPU in the Analog Section by means of the Communications Register Unit (CRU). (Refer to section 3.2.2).

The Memory Bus Interface

The Memory Bus Interface consists of two addressable latches QD7 and QD8 controlled by the Communications Register Unit on the Static CPU. To provide sufficient output drive, the interface is buffered by QD11 and QD12. A 25 way flat cable provides the connections between the Memory Bus Interface and the 25 poled D-connector on the rear panel of the RE201. The pin-out of the connector is given below:

Setup number outputs:	Pins 1 (LSB) - 7
READY output:	Pin 8
REMOTE output:	Pin 10
'Out of range' input:	Pin 11
Vernier:	Pins 17 - 19
Ground:	Pins 15 and 16

The Memory Bus Interface is used for storing and recalling of instrument settings in generators and coders in the RE1xx and RE5xx series. Only instruments supplied with the Memory Interface Option and connected to the RE201 with a special memory bus cable can be controlled. This Memory Interface Option contains a programmable memory (1024 x 4 bits) by means of which an entire function setup of an instrument can be stored and recalled. The RE201 is able to output 100 setup numbers (0-99).

The Memory Bus Interface in the RE201 is either controlled manually from the Keyboard of the RE201 using the RE201 setup facility or by means of the RE201 IEEE488 Bus Interface.

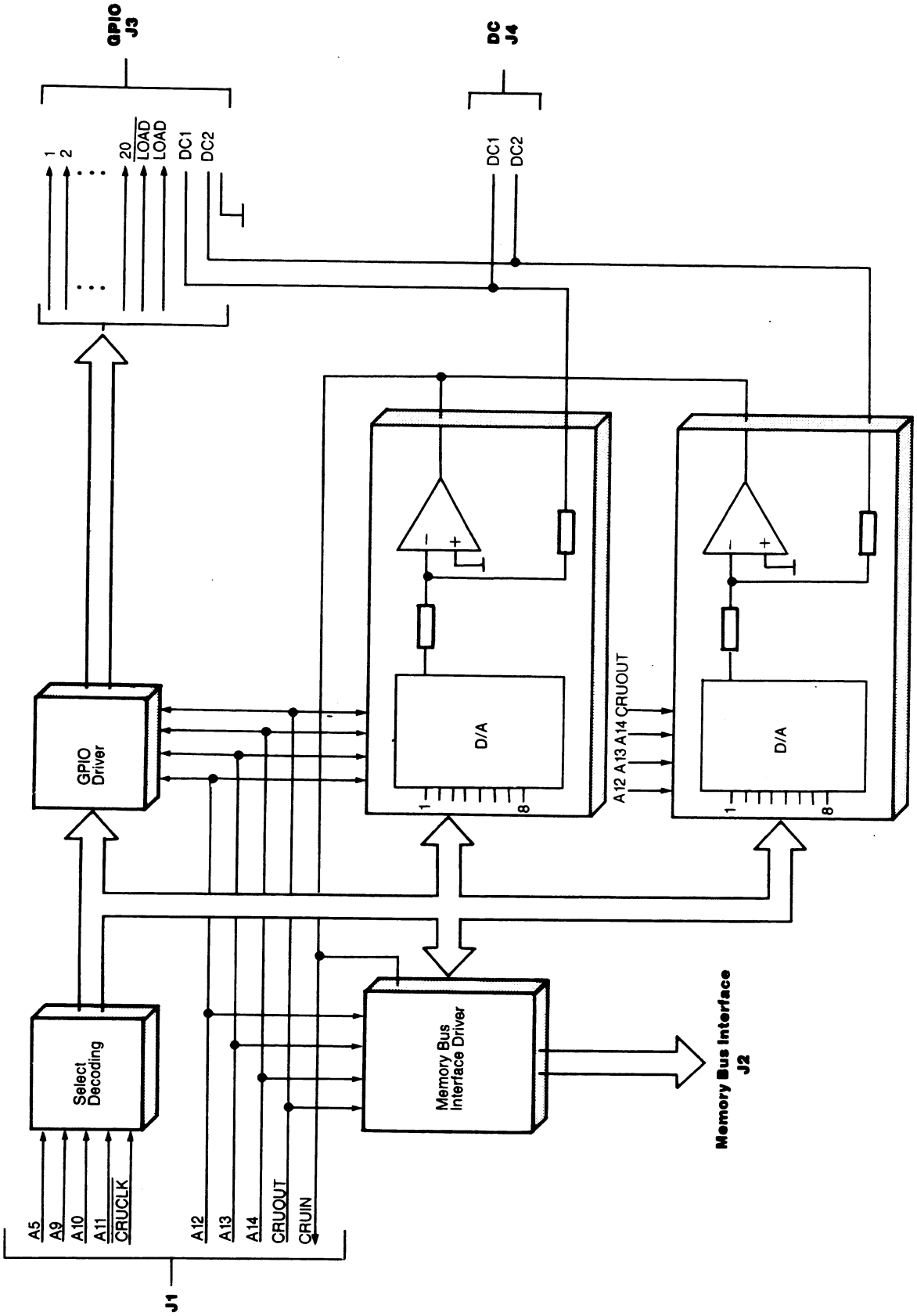
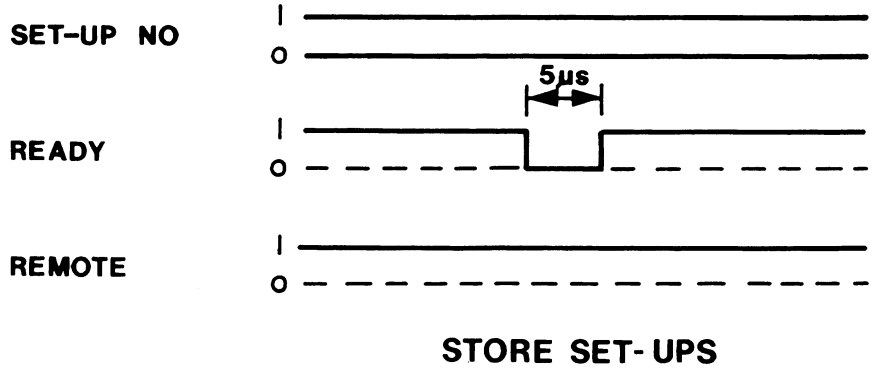


Fig 3.2.11 - I/O & Memory Bus Interface Block Diagram

Storing Setups

Instrument setups are stored in the generators connected to the RE201 during learn mode. When a setup is entered in the RE201 the interface outputs the equivalent 7 bit binary setup number. When storing the setup the RE201 generates a programming pulse of approximately 5 microseconds duration on interface output pin 8 (READY). (Refer to fig. 3.2.12).



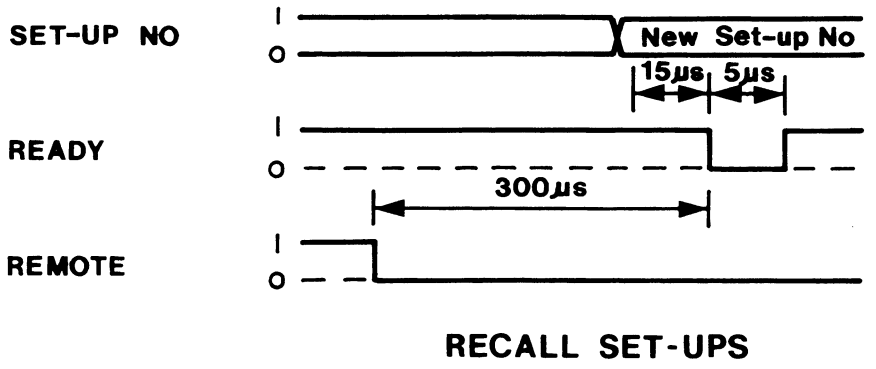


Fig. 3.2.12 - Memory Bus Interface Timing

Recalling Setups

When executing setups in the RE201 the Memory Bus Interface recalls setups in the instruments on the bus as shown in the timing diagram fig. 3.2.12. The difference between storing and recalling of setups is the state of the REMOTE output line - high for storing, low for recalling.

Vernier

R5 and R6 which are connected to pins 17-19 on the Memory Bus connector provide a vernier function on the RE104 Synthesized Signal Generator. When the vernier key is activated on the RE104, the output level is decreased by 0.5 dB.

Out of Range

The Out of Range input (QD13) (pin 11 on the Memory Bus Interface connector) is used to indicate to the RE201 when one of the instruments on the Memory Bus is out of range. The Out of Range input can only be recognized by means of the RE201 IEEE488 Interface.

The General Purpose Interface Outputs (GPIO)

The GPIO consists of three addressable latches QD2, QD3 and QD4 controlled by the Communications Register Unit of the Static CPU. A 25-way flat cable provides the connections from the GPIO to the 25 poled D-connector on the rear panel of the RE201. The pin-out of the connector is shown below:

20 output lines:	Pins 1 (LSB) - 20
LOAD output:	Pin 21
$\overline{\text{LOAD}}$ output:	Pin 22
DC1 input:	Pin 23
DC2 input:	Pin 24
Ground:	Pin 25

The GPIO is designed to control user defined circuits such as analog switches, relays and programmable power supplies. The GPIO includes 20 TTL output lines and two lines providing load pulses.

The state of each output is defined in LEARN MODE when an RE201 setup is defined. The pin No. for each of the output lines 1-20 corresponds to the designation used in LEARN MODE. The timing for the output signals is shown in fig. 3.2.13.

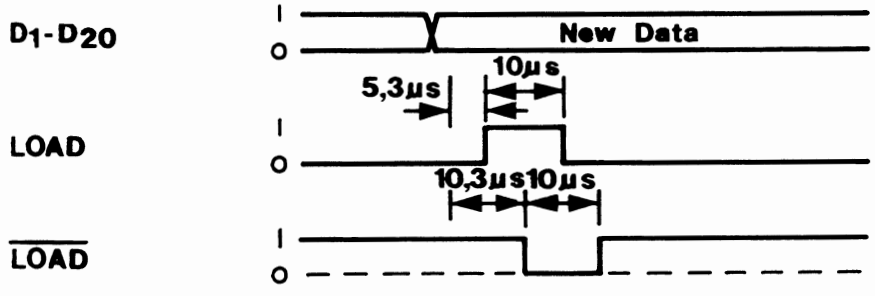


Fig. 3.2.13 - GPIO Timing

DC Inputs

The DC Inputs are connected to a special three terminal connector (BNO) on the rear panel of the RE201. The DC inputs are also connected to the GPIO connector pin 23 (DC1) and pin 24 (DC2) with ground located on pin 25. The BNO connector is shown in fig. 3.2.14.

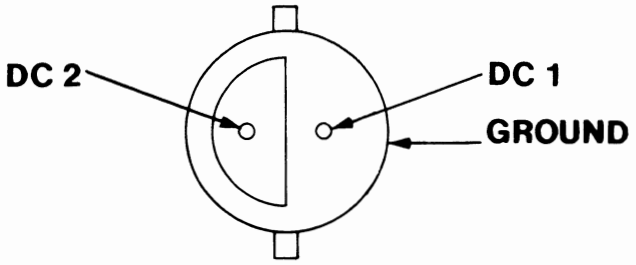


Fig. 3.2.14 - BNO DC Connector

As the two DC measurement circuits are identical, only one of the circuits will be discussed in the following (DC1).

The DC measurement circuit is operated by the Static CPU and consists of an 8 bit Digital-to-Analog converter, QD9, controlled by a Communications Register Unit Interface QD5, a comparator QA2 and an input amplifier QA1.

The output from the D/A converter (QD9) is inverted and by resistors R15 and R10 added to the DC input voltage. The sum signal is fed to a comparator (QA2). The measurement routine performed by the Static CPU is initiated by programming QD9 to 0 V and checking the comparator status by reading the CRUIN line. Then the output voltage from the D/A converter is changed (successive approximation) until variation of the LSB makes the comparator change state. As the D/A converter is an eight bit type, the resolution is 1/256 of the voltage range, i.e. 2*16 V/256 = 125 mV. The DC inputs are overvoltage protected by means of four diodes CR2-CR5.

Facilities for adjustment of the DC measurement circuits are available. The procedure is described in section 4.4.5.

Test Points

For test and adjustments a list of test points is shown below. The location of the Test Points is shown in fig. 3.2.15.

TP1: DC1 D/A converter output
TP2: DC1 comparator output
TP3: DC2 D/A converter output
TP4: DC2 comparator output

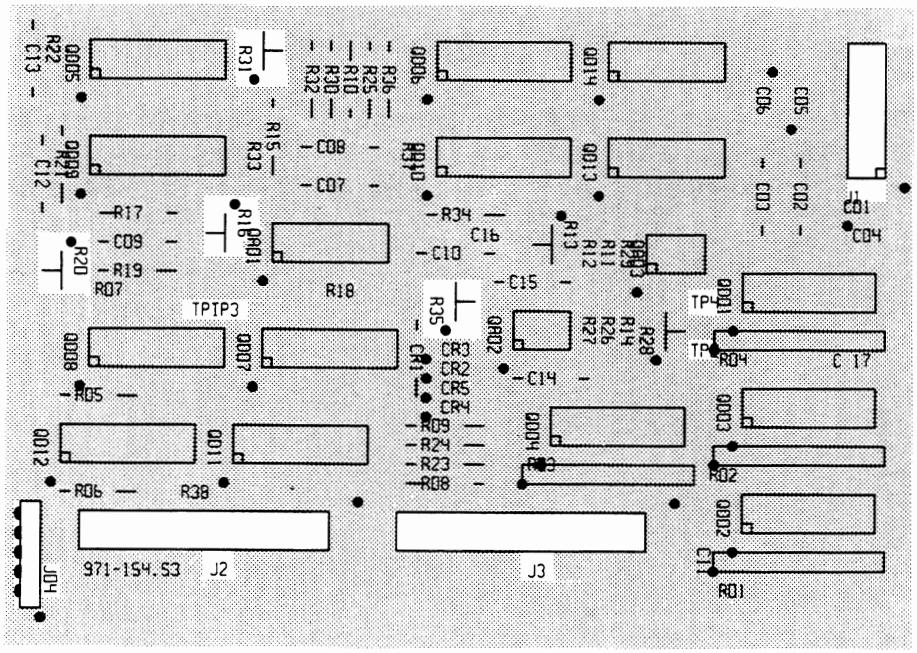


Fig. 3.2.15 - I/O & Memory Bus Interface Component Layout

3.2.7 Keyboard 901-410

The keyboard provides the operator interface when the RE201 is operated manually.

A block diagram of the keyboard is shown in fig. 3.2.16 and the schematic diagram is found on drawing No. 985-103.

When the operator depresses one of the 36 push-buttons, the interrupt line $\overline{I11}$ will go to logic zero. In this situation it is necessary to distinguish between two different cases:

Static Computer Inactive:

In this situation the level on line No. 15 of J1, STATIC, is a logical 1. This forces all outputs on QD3 and QD4 to "1". Thus when a push-button is activated one of the inputs to QD5 will be "1", which in turn will force pin 2 on QD6 ($\overline{I11}$) to "Ø".

Static Computer Active:

The level on line 15, STATIC, will be "Ø". As the computer is active the address lines A12, A13 and A14 will run through all states. This will via QD1 in time provide "$\overline{1}$"'s on all outputs on QD3 and QD4, and the interrupt line $\overline{I11}$ will go low.

When the Static Computer observes the interrupt it writes a "Ø" to QD8 pin 6. In case the RE905 External Keyboard is connected then the level on QD8 pin 6 on the PCB in the RE905 will also be "Ø" as the two keyboards share address space.

This "Ø" will allow the internal keyboard to transmit information on the CRU line CRUIN while the external keyboard will be disabled - due to an additional inverter in the RE905.

The Static Computer will now by means of QD1 and QD2 carry out a keyboard scan, and when the depressed push-button is found, the interrupt line is reset by the CPU by toggling pin 7 on QD8.

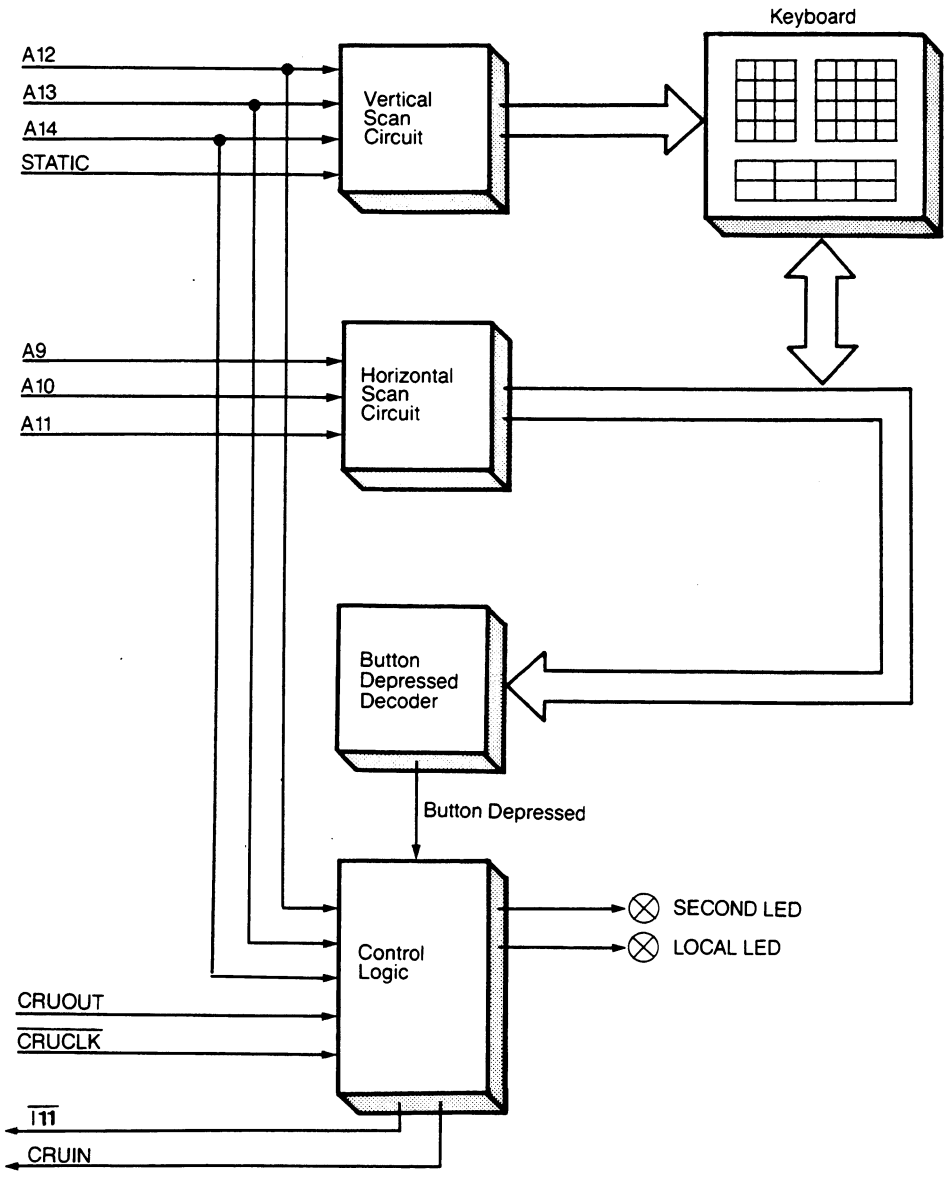


Fig. 3.2.16 - Keyboard Block Diagram

3.3 Digital Section

The Digital Section comprises:

* Motherboard
* Switch Mode Power Supply
* Main CPU Board with CRT Controller
* Arithmetical Unit
* A Shielding Box

The Motherboard has four slots for Printed Circuit Boards with an 86-pole edge connector. One slot (No. 0) is reserved for the Switch Mode Power Supply, while the remaining three slots are free for general use. However, in order to optimize the airflow for cooling the recommended positioning of the boards is as shown in fig. 3.3.1.

Two zoom option boards fit into the Digital Section providing the instrument with an increased frequency resolution over the Audio Band.

The Digital Section is shielded in order to minimize electromagnetic radiation from the instrument. The shielding is obtained by a metal box which is bolted to the base plate of the instrument with 18 bolts. The metal box is placed on top of a metal gasket which runs along the edge of the box.

The main functions of the Digital Section are:

* to control the execution of measurements
* to perform sampling with and without multiplication with a window function
* to perform the calculations involved in the complex FFT
* to interpret the obtained spectra in order to extract and calculate the information needed for a specific measurement.
* to control the displays on the CRT
* to provide the instrument with the necessary regulated power for digital circuitry and for the CRT Section

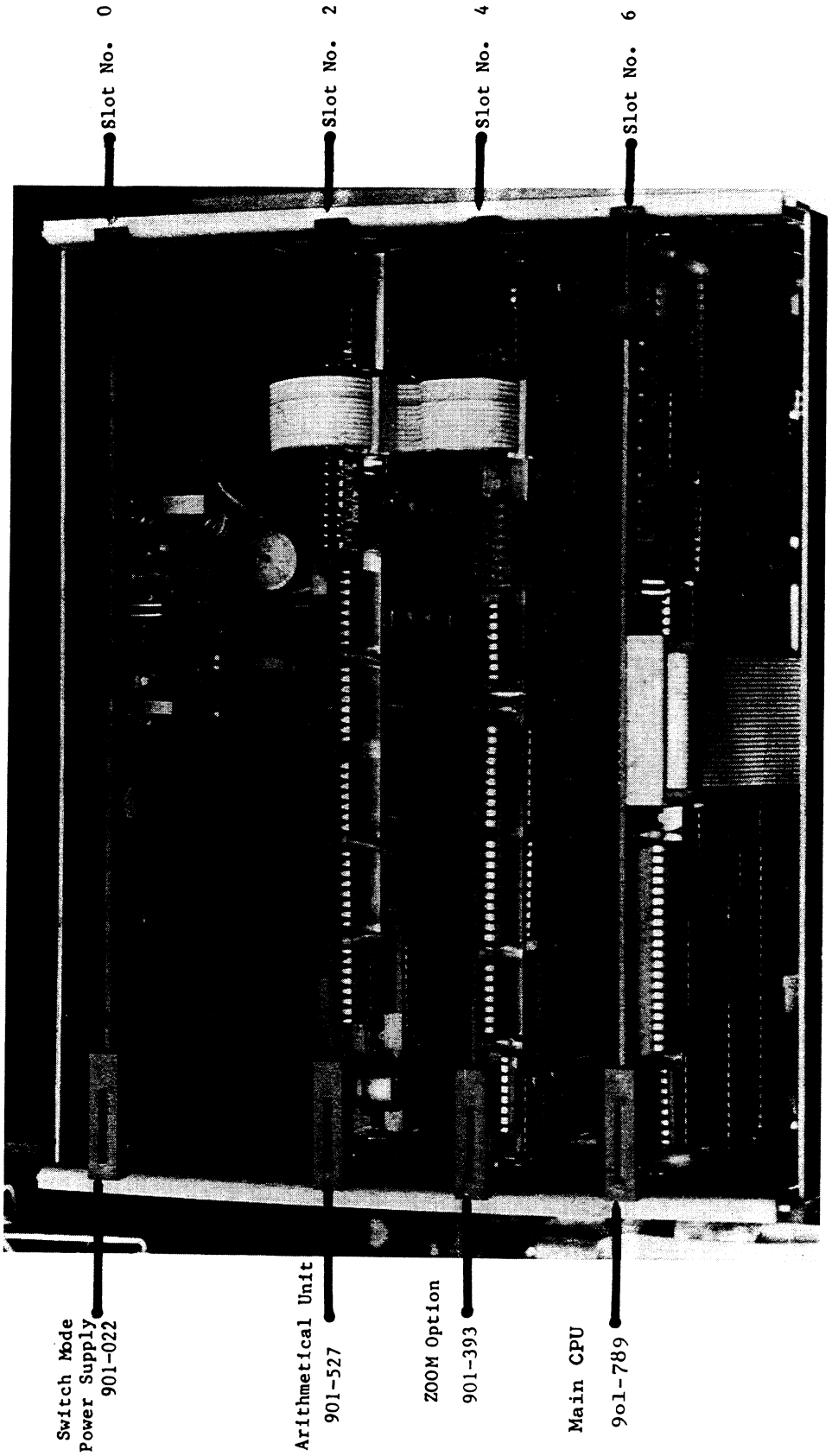


Fig. 3.3.1 - Digital Section Board Positioning

The actual setup of the analog signal path and the in- and outcoupling of different detectors is done in cooperation with the Static CPU - located in the Analog Section. The two CPU's communicate with one another over a 9600 Baud serial communication line.

3.3.1 Main CPU 901-789

The CPU board consists of a 16-bit CPU, 64 kbyte EPROM, 32 kbyte RAM, and a video controller with buffers and associated circuits for character generation and generation of video attributes.

A block diagram showing the essential parts of the CPU board is shown in fig. 3.3.2, while the schematic diagram is shown in drawing No. 985-252.

Memory

The memory is organized in bytes. The instruction set of the TMS 9995 allows both byte and word operands. When reading a word, the CPU performs two byte readings. The memory space is 64 kbytes or 32 kwords.

The RE201 memory map is shown in table 3.3.2.

The memory timing is described in section 3.2.2, static CPU.

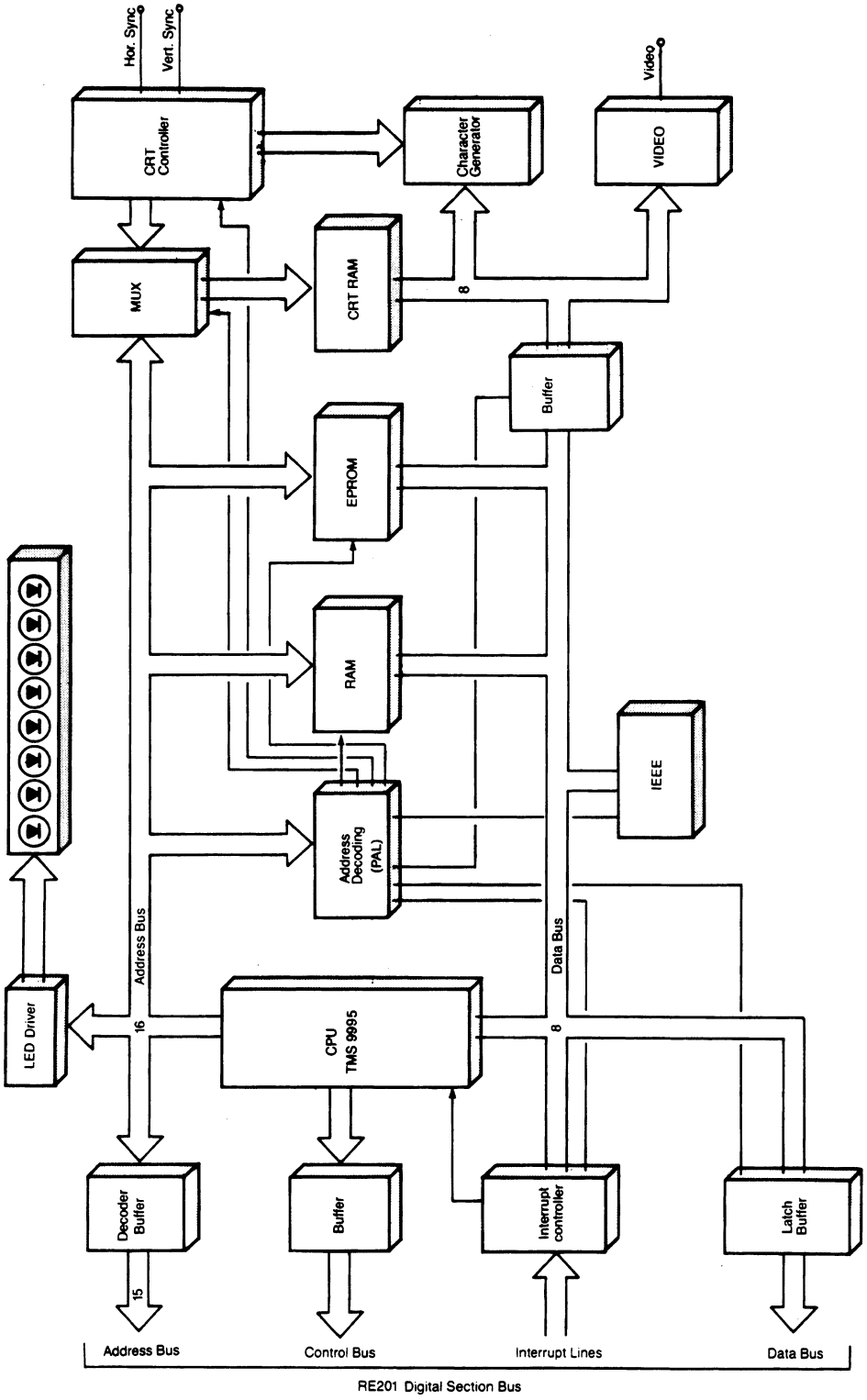


Fig. 3.3.2 - Main CPU Block Diagram

Address	Memory Content	Type	Location	Ext.Address
0000-2FFF	Programme instructions	EPROM	CPU	
3000-3FFF	Window & Tables	EPROM	ARI	4000-4FFF
4000-7FFF	Programme instructions	EPROM(IEEE)	CPU	
8000-97FF	- variables	RAM(IEEE)	CPU	
A000-8FFF	- Banks	EPROM	CPU	
C000-EFFF	- variables	RAM	CPU	
F000-F0FF	- -	RAM(internal)	CPU	
F100-F1FF	Memory mapped I/O	Devices	ARI,ZOOM	6000-60FF
F200-F2FF	CRT RAM Data	RAM	CPU	
F300-F3FF	CRT RAM Address	LATCH	CPU	
F400-F43F	CRT Controller	DEVICE	CPU	
F440-F47F	IEEE -	DEVICE	CPU	
F480-F4BF	Interrupt controller (CONTROL)	DEVICE	CPU	
F4C0-F4FF	Interrupt controller (INTA)	DEVICE	CPU	
F800-FFFF	Samples & Spectrum	RAM	ARI	5000-57FF

Table 3.3.2 - Memory Map

Bus Buffers

The Address, Data and Control Buses in the Digital Motherboard are used, when the CPU communicates with other boards in the Digital Section. The Address Bus on the CPU board is fully buffered at the interface to the Motherboard (buffers QD25-QD26).

The data bus 8 bits wide on board but 16 bits wide offboard. When the CPU communicates with the external bus, one of the bytes is latched. The buffers to the external bus are transceivers with two internal registers (Q27-Q28). When reading a word, the CPU first reads the most significant byte with one extra Wait State inserted, and the other byte is latched. The CPU then reads the latched byte without any Wait State. When writing a word, the CPU first writes the most significant byte to the latch without any Wait State; the least significant byte is then written to the bus together with the latched most significant byte with one Wait State inserted. The byte handling and the Wait State generation is controlled by a PAL (QD11).

The following control signals are buffered at the interface to the Motherboard:

* $\overline{\text{DBIN}}$
* $\overline{\text{IAQ}}$
* CLKOUT
* CRUOUT

* $\overline{\text{CRUCLK}}$

while the input line CRUIN, being an open collector line, is unbuffered.

The $\overline{\text{WE}}$ and READY signals are buffered by special circuitries to ensure correct timing.

Interrupt controller

The interrupt controller used is the Intel 8259. According to the interrupt masking and prioritizing, an interrupt is generated for the

CPU ($\overline{\text{INTA}}$). The CPU answers by an $\overline{\text{INTA}}$ pulse, wherever the interrupt controller sends out the interrupt address.

CRT Controller

The CRT controller (QD14), a 68A45 from Motorola, provides all synchronization signals for the CRT unit. The CRT RAM (QD12) contains all the variable data needed for the CRT screen. The address for the CRT RAM locations is latched from the data bus (2bytes) in order not to "waste" memory space seen from the CPU. These address latches occupy one word location of the CPU memory mapped area, the CRT RAM (transferring variables) another one.

It takes 3 memory accesses to perform one CRT RAM access. The first 2 memory accesses are used to set up the CRT RAM address, the last memory access to perform the actual CRT RAM access.

A conflict occurs, when the CRT controller and the CPU try to access the CRT RAM simultaneously. To ensure a quick screen update, the CPU always has the highest priority. When the CPU accesses the CRT RAM, the data to the video circuit will be erroneous. To avoid flickering on the screen, the video signal is turned off, until the CPU has completed the access to the CRT RAM.

Character Mode

In character mode, the CRT screen is formatted in 16 lines by 32 characters. As the CRT RAM (QD12) is 8kx8bit, it is possible to store 16 pages in the CRT RAM. A character area is 9x12 dots out of which the character only occupies 7x9 dots. This is illustrated in fig. 3.3.3.

When refreshing the CRT screen, the CRT controller outputs the CRT RAM address of the character to be written. The addresses cell contains the ASCII code for the character. These 8 bits together with 4 bits from the video line counter in the CRT controller constitutes the address to the character PROM (QD13).

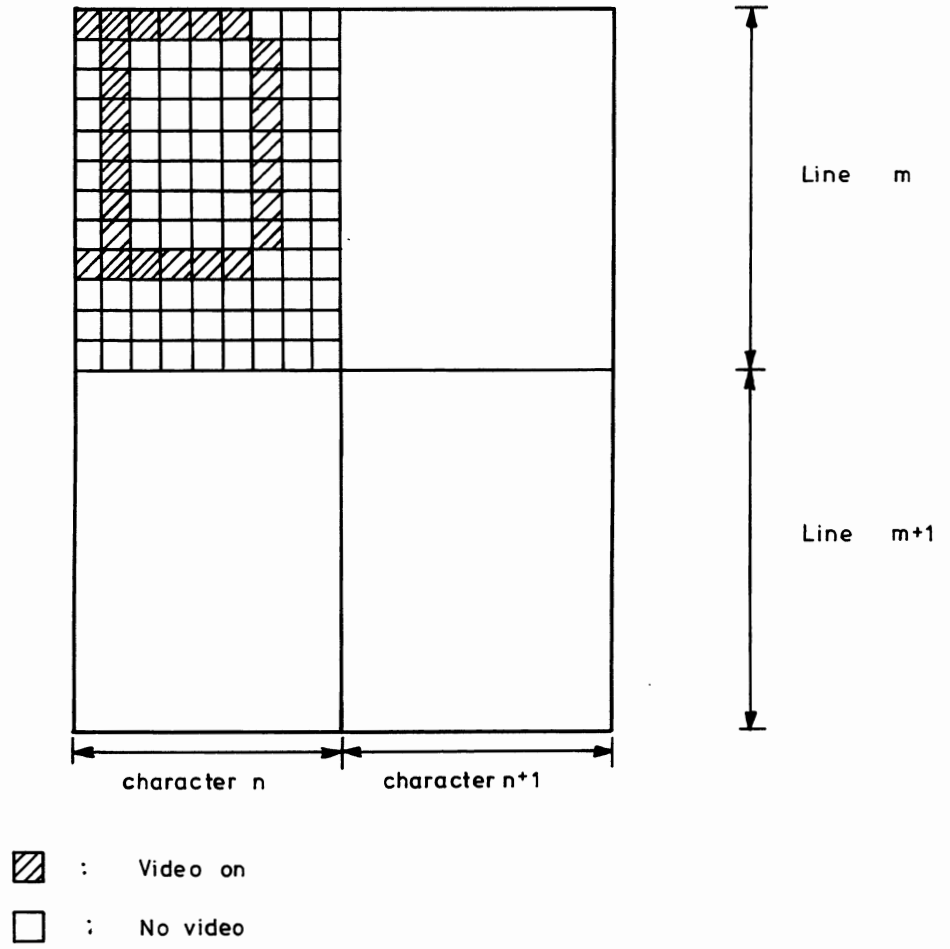


Fig. 3.3.3 - Dot Character Font

This PROM outputs 16 bits/character/video line. One of the first 8 bits is latched; together with the next 8 bits these 9 bits control the required 9 dots per character, which are output serially on the video line.

This sequence is performed for every character (32) in one scan line, repeated for every scan line (12) in the character area. These 384 accesses to the CRT RAM are performed for every character line.

The output from the CRT RAM is 8 bits wide, but only 6 bits are necessary to select a character. One of the remaining bits is used to access another part of the character PROM used for display of inverse video characters. The remaining bit is used for a limited set of graphic characters, as shown in fig. 3.3.4.

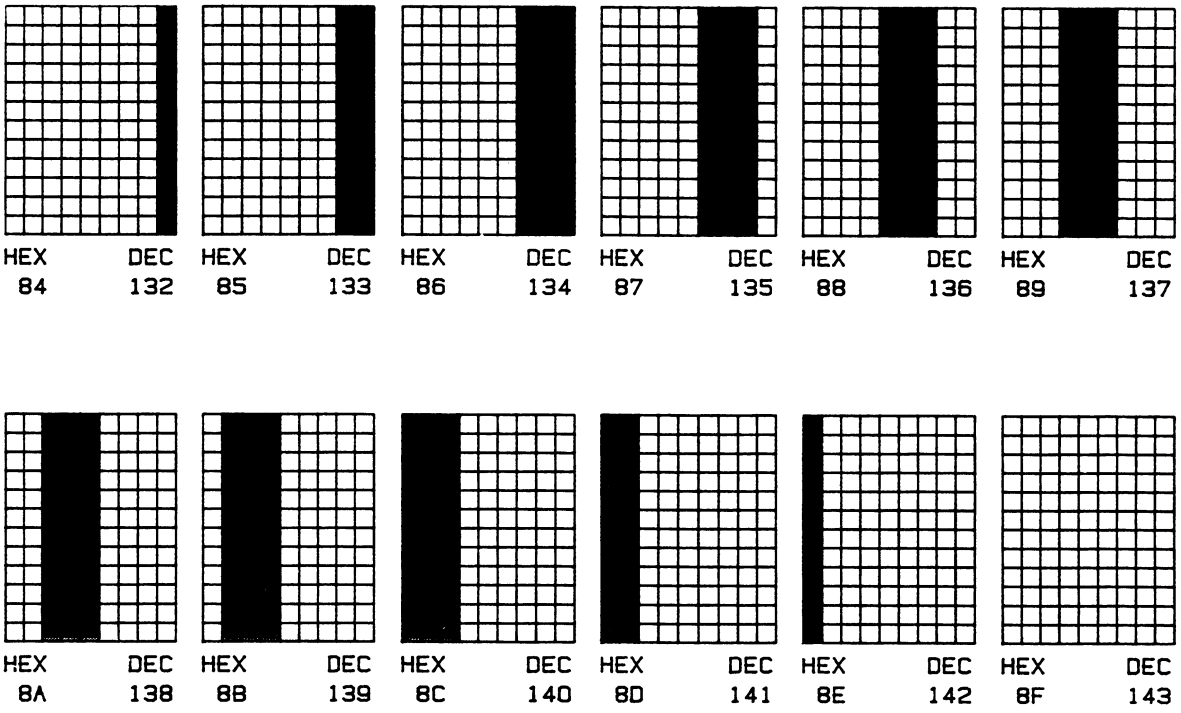


Fig. 3.3.4 - Graphics Character

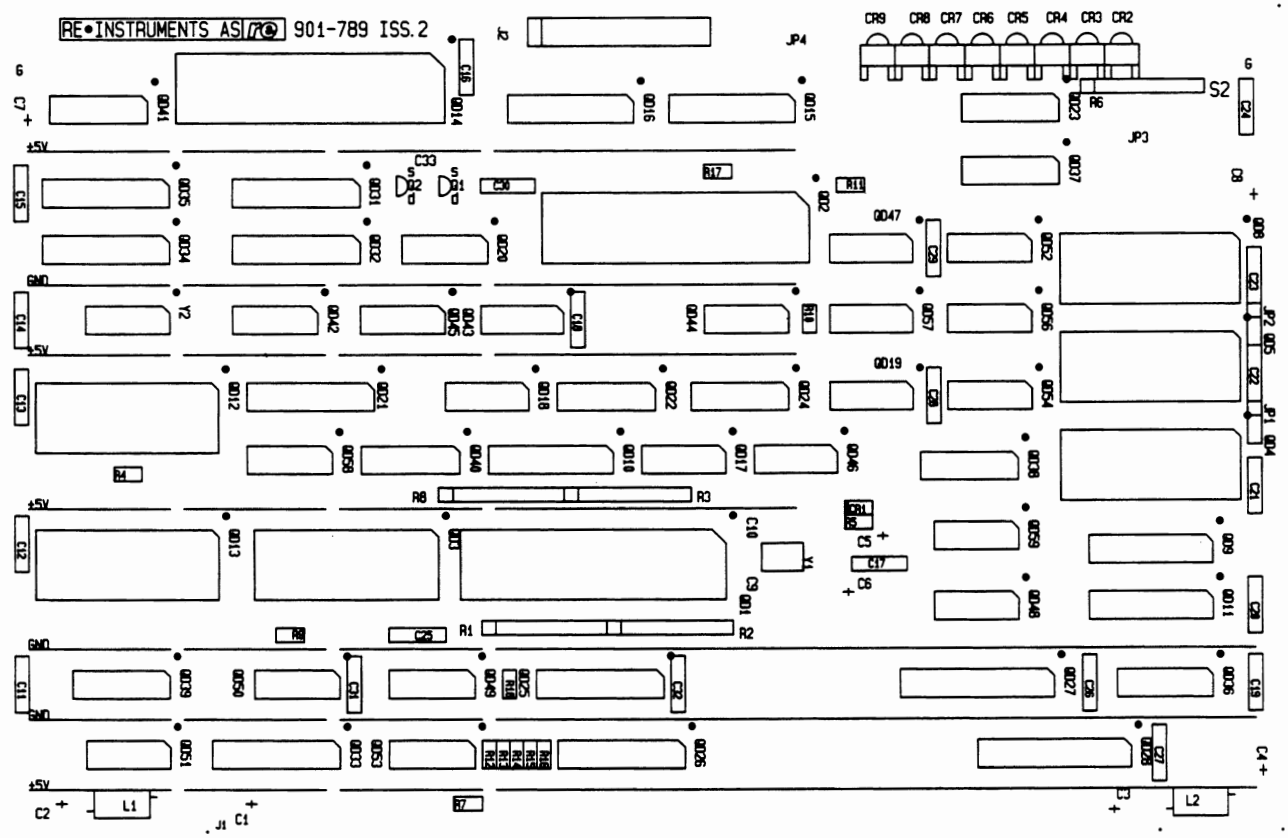


Fig. 3.3.5 - Main CPU Component Layout

The link between the CPU and the IEEE488 Bus is provided by the TMS9914, which is a programmable, general purpose interface adapter, allowing the instrument to act as Talker, Listener or Controller as required. The TMS9914 serves the purpose of ensuring that the state of the IEEE488 Bus Interface and the RE201 instrument is always in accordance with the requirements of the IEEE488 Standard Protocol.

The direct interface to the IEEE488 Bus lines is QD15 and QD16 , which are buffers specifically designed to meet the requirements in the interface standard (termination and drive capability). These buffers - depending on application - are programmed to be either open collector outputs or three state outputs for increased communications speed on the IEEE488 Bus lines.

To hold the software and data area necessary to run the IEEE488 Bus drive, 8 kbyte static RAM and 16 kbyte EPROM of the CPU memory area is dedicated to the IEEE488 Bus handling.

Most of the RAM area is used to hold the set-up information, as the set-up facility is only available via the IEEE488 Bus.

General Purpose Interface Adaptor TMS9914

The TMS9914 is designed to be used when an intelligent instrument is required to communicate with an IEEE488 General Purpose Interface Bus. It performs the interface function between the microprocessor and bus and relieves the processor of the task of maintaining the IEEE488 protocol. By utilizing the interrupt capabilities of the device the bus does not have to be continually polled, and fast responses to changes in the interface configuration can be achieved.

The GPIB input/output pins are connected to the IEEE488 Bus via bus transceivers. The direction of data flow is controlled by the TE and CONTROLLER outputs generated on the TMS9914. The SN75160 and 75161 are designed specifically for use with a GPIB interface. The TE and CONTROLLER signals are routed within the devices so that the buffers on particular lines are controlled as required by the TMS9914.

Communication between the microprocessor and TMS9914 is carried out via memory mapped registers. There are 13 registers within the TMS9914, 6 of which are read and 7 write. They are used both to pass control data to, and to get status information from the device.

The 3 of least significant address lines from the CPU are connected to the register select lines RS0, RS1 and RS2 and determine the particular register selected. The high order address lines are decoded by external logic to cause the $\overline{CE}$ input to the TMS9914 to be pulled low when any one of 8 consecutive addresses are selected. Reading or writing to these locations transfers information between the TMS9914 and the microprocessor. Reading and writing to the same location will not access the same register within the TMS9914 since they are either read-only or write-only registers. For example, a read operation with RS0-RS2 = 011 gives the current status of the GPIB interface control lines, whereas a write to this location loads the so-called auxiliary command register.

The IEEE488 standard prescribes each device on the bus interface to be given a 5-bit address, enabling it to be addressed as a Talker or Listener. This address is defined as a part of the RE201 system definitions and written into the address register whenever SYSTEM parameters are stored, and as part of the initialization procedure. When this address is detected on the GPIB data lines, the TMS9914 responds by causing an MA (My Address) interrupt and entering the required addressed state.

The TMS9914 is provided with facilities for meeting the complete IEEE488 protocol in the RE201, however, only the subset listed in section 1.4 is implemented.

Table 3.3.3 exhibits a list defining the functions of the individual pins on the TMS9914.

In case of a Parallel Poll Request the second OR gate will cause the outputs of the bus driver, QD15, to change from tri-state to open collector. Usually, the tri-state configuration is used to increase the bus speed, but when a Parallel Poll is executed it is necessary for all bus drivers connected to the IEEE488 Bus Interface Option to have open collector outputs.

Signature	Pin	I/O (Type)	Description
			Power Supplies & Clock
$\overline{\emptyset}$	18	I	CLOCK input: up to 5 MHz maximum.
Vss	20		Ground reference voltage.
Vcc	40		Supply voltage (+5 V nominal).
			IEEE488 Data I/O
DIO8 (MSB)	31	I/O (p/p)	DIO8 through DIO1 are the data input/output lines on the IEEE488 Bus side.
DIO7	32	I/O (p/p)	These pins connect to the IEEE488 Bus via non-invertings tranceivers.
DIO6	33	I/O (p/p)	
DIO5	34	I/O (p/p)	
DIO4	35	I/O (p/p)	
DIO3	36	I/O (p/p)	
DIO2	37	I/O (p/p)	
DIO1 (LSB)	38	I/O (p/p)	
			IEEE488 Control
DAV	26	I/O (p/p)	DATA VALID: handshake line controlled by source to show acceptors when valid data is present on the bus.
NDAC	24	I/O (p/p)	NOT DATA ACCEPTED: handshake line. Acceptor sets this false (high) when it has latched the data from the I/O lines.
NRFD	25	I/O (p/p)	NOT READY FOR DATA: handshake line. Sent by acceptor to indicate readiness for the next byte.
ATN	28	I/O (p/p)	ATTENTION: sent by controller. When true (low) interface commands are being sent over the DIO lines. When false (high) these lines carry data.
REN	22	I/O (o/d)	REMOTE ENABLE: sent by system controller to select control either from the front panel or from the IEEE488 Bus.
IFC	23	I/O (o/d)	INTERFACE CLEAR: sent by the system controller to set the interface system into a known quiescent state.
SRQ	29	I/O (p/p)	SERVICE REQUEST: set true (low) by a device to indicate a need for service.
EOI	27	I/O (p/p)	END OR IDENTIFY: if ATN is false (high) this indicates the end of the message block. If ATN is true (low) the controller is requesting a parallel poll.
$\overline{\text{CONTROLLER}}$	30	O (p/p)	Controls the direction of transfer of the bus transceivers for the bus management lines (ATN,SRQ). When false the device is the controller in charge (not used in the 901-686).
TE	21	O (p/p)	TALK ENABLE: controls the direction of transfer of the line transceivers.
			Data Bus
DØ (MSB)	17	I/O (p/p)	Data transfer lines on CPU side of the device.
D1	16	I/O (p/p)	
D2	15	I/O (p/p)	
D3	14	I/O (p/p)	
D4	13	I/O (p/p)	
D5	12	I/O (p/p)	
D6	11	I/O (p/p)	
D7 (LSB)	10	I/O (p/p)	
			CPU Control
RSØ (MSB)	6	I	REGISTER SELECT LINES: determine which register is addressed by the CPU
RS1	7	I	during a read or write operation.
RS2 (LSB)	8	I	
$\overline{\text{CE}}$	3	I	CHIP ENABLE: TMS 9914 active when the $\overline{\text{CE}}$ pin is pulled low.
$\overline{\text{WE}}$	4	I	WRITE ENABLE: when active (low) indicates to the TMS 9914 that data is being written to one of its registers.
DBIN	5	I	DATA BUS IN: an active (high) state indicates to the TMS 9914 that a read is about to be carried out by the CPU.
$\overline{\text{INT}}$	9	O (o/d)	INTERRUPT: sent to the CPU to cause a branch to a service routine.
$\overline{\text{ACCRQ}}$	1	O (p/p)	ACCESS REQUEST: this pin becomes active (low) to request a direct memory access. Not used in the 901-686.
$\overline{\text{ACCGR}}$	2	I	ACCESS GRANTED: Not used in the 901-686.
$\overline{\text{RESET}}$	19	I	RESET: initializes the TMS9914 at power up.
TR	39	O (p/p)	TRIGGER: activated when the GET command is received over the interface. Not used in the 901-686.

(p/p) = push/pull output
(o/d) = open drain output with internal pull up.

Table 3.3.3 - TMS9914 Pin Assignment and Functions

3.3.2 Arithmetical Unit 901-527

The Arithmetical Unit provides the instrument with the basic Data Collection and FFT capabilities together with an Integration Unit used for RMS measurements. The Arithmetical Unit is able to perform autonomous operations, i.e. operate without interactions from the CPU, by means of a sequencer, implemented by a Schottky PROM.

Main Features of the Arithmetical Unit are:

* Data Collection with Windowing via DMA
* Window multiplication with three different Windows
* Computation of Dual Node pairs in FFT
* Squaring and Summation in 48 bits for RMS-calculation

A block diagram showing the essential parts of the Arithmetical Unit is shown in fig. 3.3.6, while the schematic diagram is shown on drawing No. 985-109.

Operation Mode Word

The Main CPU programs the Arithmetical Unit for the desired mode of operation by setting the appropriate bits in the operation mode latch QD21 through the CRU interface QD20.

One of the bits, MR, provides a Master Reset of vital functions, such as various counters and the sequencer. Two parameters, DMA and RMS, determine the operation of the Multiplier/Adder-Section.

The Board can be configured for three different operations of the Shift Registers and Multiplier/Adder-Section:

* DMA - operation: multiplication of time-samples with Window samples in order to provide the windowing in the time-domain, and storing of results in "scrambled" order to prepare for the FFT.
* RMS - operation: squaring and summation of time-samples using a combination of three 16 bits Shift Registers to provide one 48 bit summation-register.
* BUTTERFLY - operation: complex multiplication and summation calculations involved in the complex FFT.

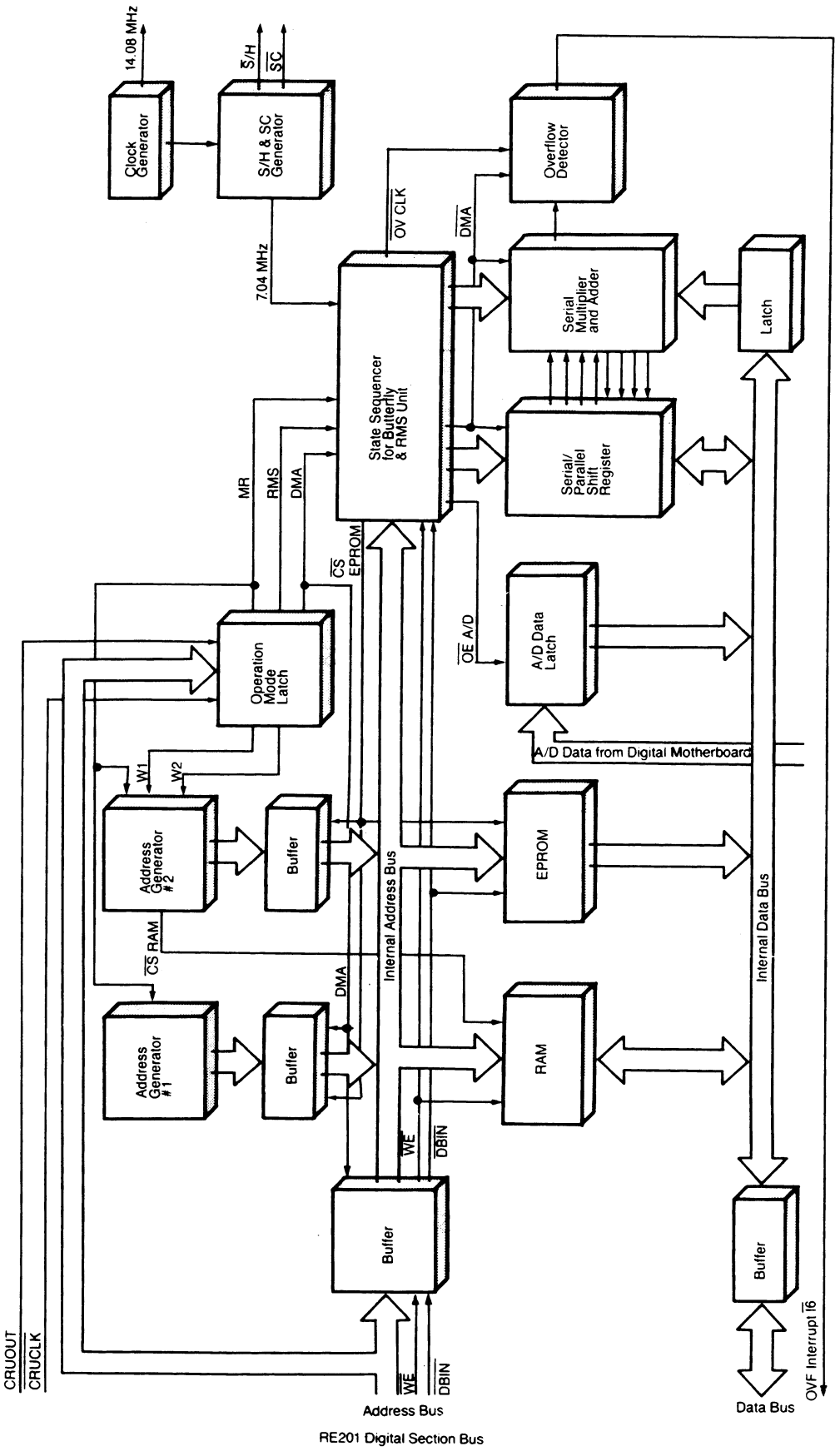


Fig. 3.3.6 - Arithmetical Unit Block Diagram

The relationship between the Modebits DMA, RMS and the operation obtained is shown below:

DMA	RMS	Operation
0	0	BUTTERFLY
0	1	N.U.
1	0	DMA
1	1	RMS

The two parameters W1 and W2 are used to select the appropriate window function during DMA, as shown below:

W1	W2	Window
0	0	Rectangular
0	1	N.U.
1	1	Sine
1	0	FTBH

The three remaining Modebits EN8, EN16 and EN32 determine the number of samples collected during DMA and RMS Operation. The relationship between the number of samples collected before the Data Ready Signal occurs, and the setting of these three bits is shown below:

EN32	EN16	EN8	Samples
X	X	1	512
X	1	0	1024
1	0	0	2048
0	0	0	4096

X: Either 0 or 1 - don't care.

DMA and Windowing

In order to increase the throughput of the instrument, collection of data from the Analog Input Section is done by means of a DMA - Unit (Direct Memory Access). In this mode the computer may perform other tasks while data collection is in progress.

By necessity, every signal which is processed by means of FFT analysis must be of finite length. As the first step in the FFT routine in the RE201, the signal is observed for 8 ms (512 samples of 15.625 micro secs. sample period). Processing these 512 real samples in an 256 point Complex FFT produces 256 Complex Frequency samples spaced 125 Hz apart. Due to the severe leakage found when applying the FFT on raw time-samples (truncation in the time domain) it is necessary to employ a time domain window which provides smooth transitions to zero at the edges of the signal. Hereby it is possible to reduce the leakage, however, the penalty will be reduced selectivity.

The output from the 512 point FFT analysis is equivalent to the output from 256 identical bandpass filters separated by fs/512 (fs is the

sampling frequency), the frequency response of the individual filters being the Fourier transform of the window time function.

The instrument provides three windows: the Rectangular Window, the Sine Window and the Four Term Blackmann-Harris Window.

The Rectangular Window (no windowing at all) has a side lope level as high as -13 dB (refer to fig. 3.3.7), and does introduce a large amount of leakage. The Sine Window has a side lope level of -23 dB (refer to fig. 3.3.8), while the Four Term Blackmann-Harris (FTBH) Window has a side lope level as low as -92 dB (refer to fig. 3.3.9). In the RE201, the last two are used in connection with the FFT processing.

The FTBH window is used for all distortion measurements due to the extremely low sidelobe level. The time-samples for the windows are stored in EPROM (QD41/42).

Referring to drawing No. 985-109 the operating sequence during DMA with windowing is as follows:

In order to initiate a data collection of samples from the A/D converter on the Analog Frontend the Computer uses the CRU interface to set the Arithmetical Unit. QD20/21 are loaded via the CRU interface to set the mode of operation, which is determined from the outputs of QD 21.

The window parameter in the operation word (W1 & W2) selects between three different setups for the three windows, as mentioned above. A 512 sample DMA is initiated by the following setup:

* MR low
* DMA high
* RMS low
* EN8, EN16, EN32 low
* W1 low for no window (Rectangular Window),
  high for window according to W2
* W2 high for FTBH Window, low for Sine Window

When the Arithmetical Unit has received this setup, the DMA controller (QD22-QD28 & QD43) together with the sequencer (QD73-QD74 & QD66-QD65) starts a 512 sample collection cycle. This cycle is shown in fig. 3.3.10:

* Fetch a 12 bit time-sample from the A/D Converter

* Fetch a window sample from EPROM (selected by W1 & W2)

* Enable Clock to the Multiplier (MCLK)

* Fetch result of Multiplication and store in RAM

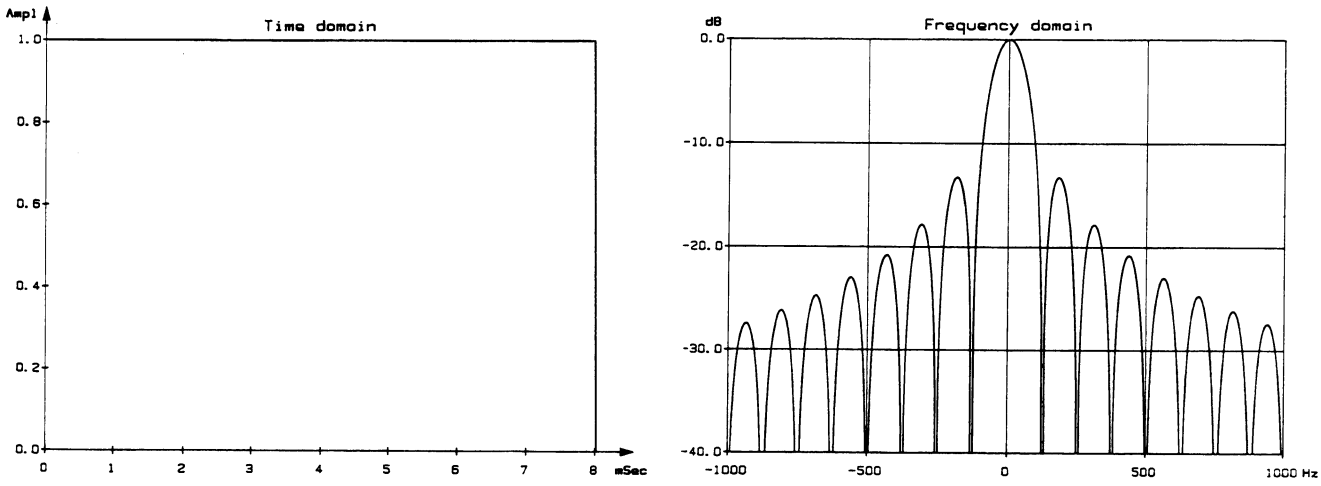


Fig. 3.3.7 - Rectangular Window

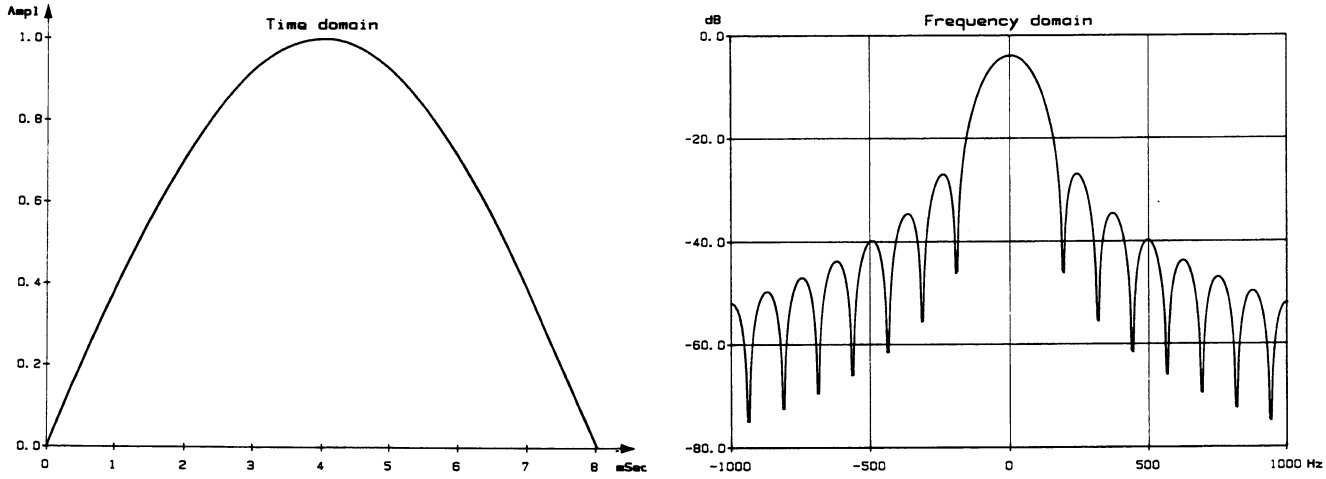


Fig. 3.3.8 - Sine Window

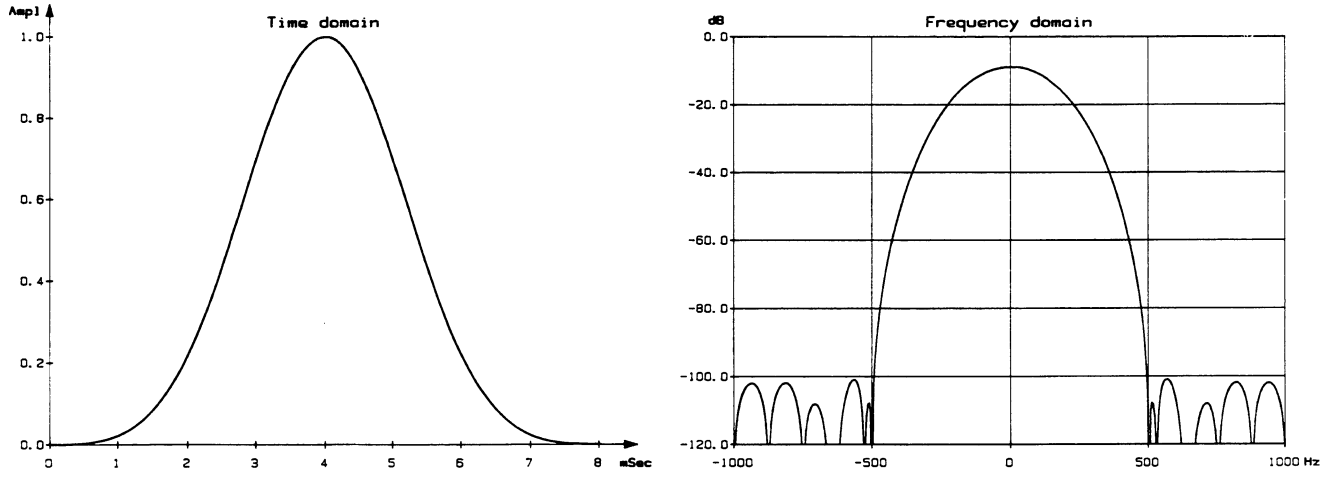


Fig. 3.3.9 - FTBH Window

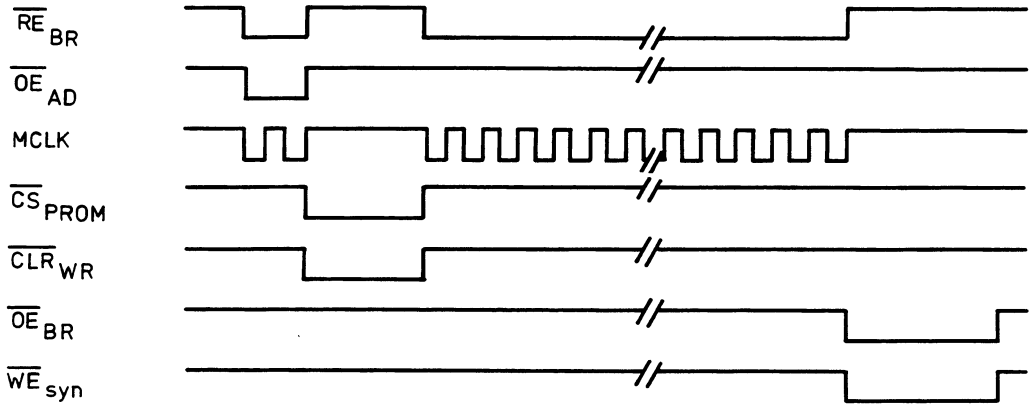


Fig. 3.3.10 - Sample Collection Cycle

Every time this cycle has been executed the sequencer clocks QD43. When all 512 samples have been placed in RAM, the Arithmetical Unit will generate an interrupt at level 7 ($\overline{INT7}$ goes low) telling the CPU that the DMA-unit has finished the requested data transfer. At the same time this signal ($\overline{DR}$==$\overline{INT7}$) will stop the sequencer.

The Butterfly Unit

The basic operation of a radix-2 FFT incorporates a so-called butterfly operation, which performs multiplications and additions of three complex numbers A, B and exp(-jφ) as outlined below:

A' = A + B * exp(-jφ) = (Ar+Br*Wr-Bi*Wi) + j(Ai+Bi*Wr+Br*Wi)

B' = A - B * exp(-jφ) = (Ar-Br*Wr+Bi*Wi) + j(Ai-Br*Wi-Bi*Wr)

Where: Ar: Real Part of A - Ai: Imaginary Part of A
Br: Real Part of B - Bi: Imaginary Part of B
Wr: cos(φ) - Wi: -sin(φ)

These computations can be illustrated as shown in fig. 3.3.11. The Arithmetical Unit uses a look-up table for the cosine- and sine values.

During butterfly operations the Arithmetical Unit is set via the CRU interface to the following conditions:

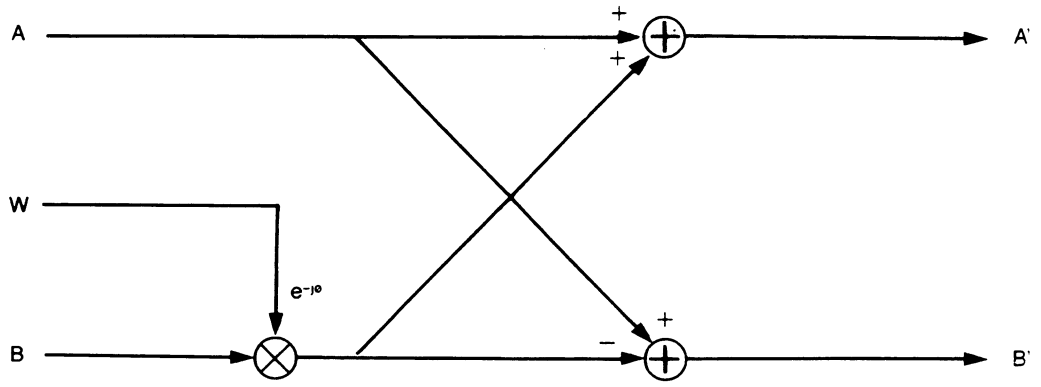


Fig. 3.3.11 - Butterfly

* MR low
* DMA low
* W1 XXX, W2 XXX
* RMS low
* EN8-EN32 XXX

where XXX indicate that the corresponding bits are "don't care". A butterfly operation is executed as follows:

* The CPU loads the real part of A into register Ar (QD48-49)

* The CPU loads the imaginary part of A into register Ai (QD52-53)

* The CPU loads the real part of B into register Br (QD46-47)

* The CPU loads the imaginary part of B into register Bi (QD50-51)

* The CPU loads cos(ϕ) into register Wr (QD54-56)

* The CPU loads -sin(ϕ) into register Wi (QD58-61)

Loading of register Wi automatically starts the sequencer so that the complex calculations involved in the butterfly are performed. Cos(ϕ) samples are stored in EPROM (QD40-41), sin(ϕ) values are derived from the cosinetable.

The simplified timing diagram, fig. 3.3.12, shows the Butterfly sequence.

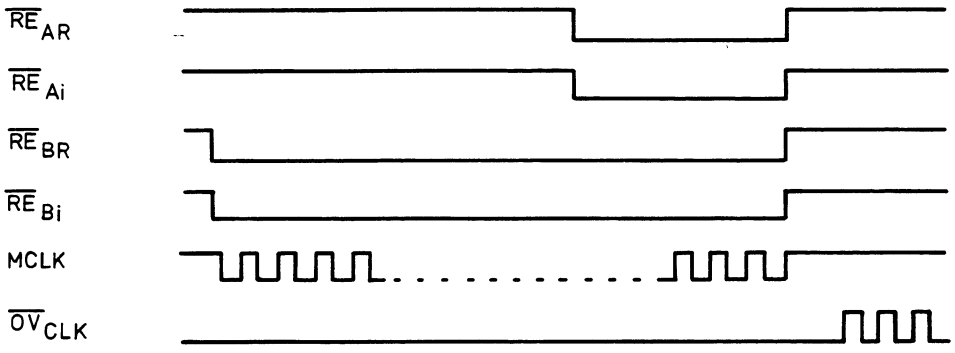


Fig. 3.3.12 - Butterfly Operation Timing

Overflow Detection

Due to the limited register length (16 bits) the arithmetical operations may result in numbers, which cannot be represented in the registers (overflow). In order to detect such a situation, an overflow detector has been implemented (QD70-QD72).

The sequencer clocks the circuit by means of the OV-CLK signal - in case an overflow occurs, an interrupt on level 6 will be generated ($\overline{INT6}$ goes low) to inform the CPU of the overflow in the Arithmetical Unit. The CPU then handles the overflow by shifting all numbers being processed in the FFT one position to the right, increments a block exponent and restarts the butterfly operation.

The interrupt is reset by the CPU via the signal $\overline{INTA}$ (QD20 pin 13). The overflow interrupt is only enabled during operation with DMA low (Butterfly Operation).

RMS Unit

The RMS Unit provides the instrument with the basic capability for measuring RMS as an integration of squared time-samples.

The RMS Unit is set via the CRU interface to the following conditions:

* MR low
* DMA high
* W1 XXX, W2 XXX
* RMS high

The three remaining bits EN8-32 are set according to the number of time-samples which should be added. EN8 provides summation over 512 samples, while EN16 provides summation over 1048 samples and EN32 provides a summation over 2048 samples. The corresponding integration periods are 8 ms, 16 ms and 32 ms, respectively. If all bits are 0, a 64 ms integration time is used. Higher integration periods are implemented as successive 64 ms sampling periods.

During initialization of the RMS Unit the CPU resets all registers in order to clear the integrator. The hardware used for the RMS Unit is the same as is used for the butterfly operations. A schematic diagram of the RMS Unit is shown in fig. 3.3.13.

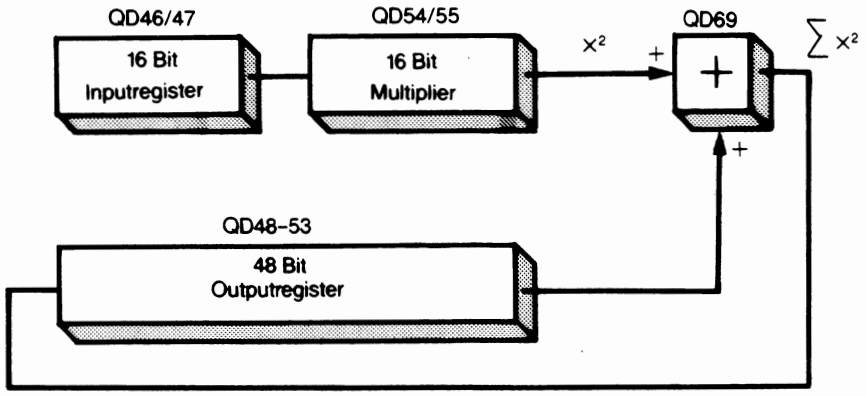


Fig. 3.3.13 - RMS Unit

The basic cycle performed by the sequencer during RMS calculations is as follows:

* Fetch a sample from the A/D Converter
* Transfer sample to Input Register and Multiplier
* Calculate the square and add to Output Register

A simplified diagram is shown in fig. 3.3.14.

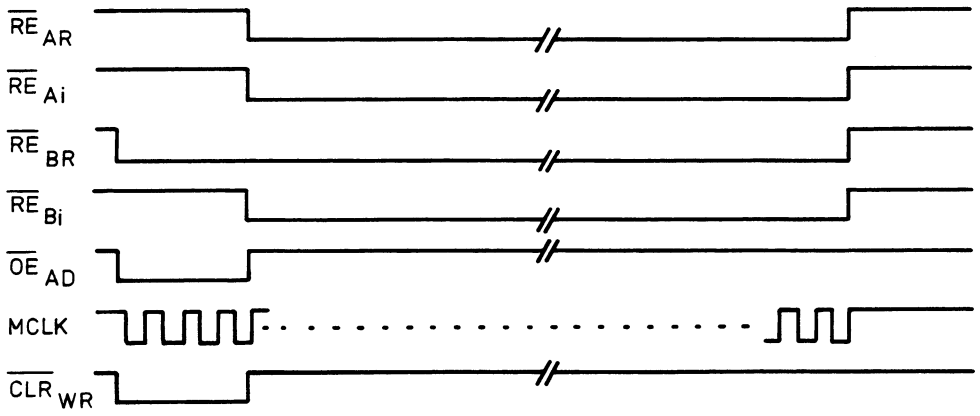


Fig. 3.3.14 - RMS Unit Operation

Each time this cycle has been executed the sequencer triggers QD43, which in turn counts the number of processed time-samples. When the requested number of samples is reached, the CPU is notified of the completion of the requested integration period by means of an interrupt on level 7 ($\overline{INT7}$ goes low). At the same time this signal will stop the sequencer.

Address Generator(s)

During data collection (DMA high) the RAM Addresses for the time-samples are generated by Address Generator 2 (QD22-23 & QD43). The 12 stage counter QD43 is reset by means of the Master Reset Signal from the Operation Word. The output from this counter is routed to the Address Bus, when the buffers QD22 and QD23 are enabled. This is controlled by DMA and $\overline{CS}$ PROM being high, signalling that the sequencer is storing time-samples. The outputs from the counter are "scrambled", ensuring that time-samples are stored in the requisite order for performing an in-place FFT.

During Window Multiplication and Butterfly operation, the PROM Addresses for the Window samples and SINE-COSINE-samples are generated by Address Generator 1 (QD9, QD16, QD22, QD26-28 and QD24-25). The binary Up/Down counter QD26-28 will select the appropriate Address Range in PROM depending on the two Modebits W1 & W2. Counting can be reversed by means of the trigger circuit QD9, QD16 & QD32, thereby reducing the size of both the Window tables and the SINE-COSINE-table.

Both Address Generators are clocked by the "WE syn" signal from the sequencer, which signals that a time-sample is to be written to RAM. The three most significant output bits from Address Generator 1

together with the extension made by the most significant output bit and flip-flop QD32 are used to trigger the Data Ready Circuit QD7, which informs the CPU that the requested number of time-samples has been processed. The Data Ready Circuit provides outputs for 512, 1024, 2048 and 4096 samples.

$\overline{S}/H$ and $\overline{SC}$ Generation

Also comprised in the Arithmetical Unit are the main clock (14.08 MHz) and the $\overline{S}/H$ (Sample/Hold) and $\overline{SC}$ (Start Conversion) signal generators. The $\overline{S}/H$ and $\overline{SC}$ timing pulses, which are routed to the Analog Frontend by two coaxial cables, are generated by QD75-76. The appearance of these signals should be as shown in fig. 3.3.15.

* 61 periods of 14.08 MHz, sample
* 159 periods of 14.08 MHz, hold
* 140 periods of 14.08 MHz, A/D conversion

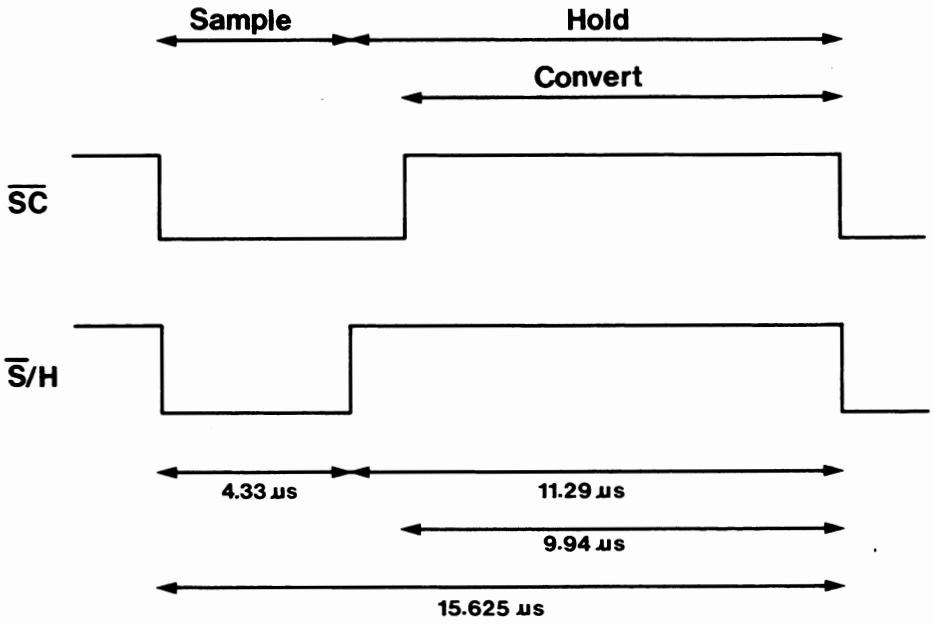


Fig. 3.3.15 - $\overline{SC}$ and $\overline{S}/H$ Signal Timing

The $\overline{SC}$ signal is also routed to the sequencer in order to synchronize the sequencer and the A/D Converter during RMS and DMA operations.

Furthermore, $\overline{S}/H$ is used for synchronization when the CPU reads the A/D Converter directly. The flip-flop QD72, which is clocked by the CPU Clock CLKOUT, ensures that READY for the CPU is kept inactive

until a conversion cycle for the A/D Converter is completed. In this way, reading of invalid data being present during conversion is prevented.

3.3.3 Digital Motherboard 901-790

The Digital Motherboard provides the base for distributing signals among the boards in the Digital Section. Address Bus, Data Bus, Power Bus and Various Control Signals are distributed on the common bus, which runs on this board. One special (SMPS) and seven general Bus Connectors are provided for Circuit Boards with an edge Connector.

The essential parts of the Digital Motherboard are shown in a block diagram (refer to fig. 3.3.16), while the schematic diagram is shown on drawing No. 985-253.

Besides distribution of the common bus signals, this Board provides the linkage to other sections of the instrument (J1 for the Analog Section, J3 for the CRT Section), and the connections to the external RS232C connector on the rear panel of the instrument (J2). Reference is made to the Top Level Interconnections and Block Diagram (drawing No. 985-217) at the rear of this manual.

A Serial to Parallel Latch (QD7-9) converts and latches the serial data from the A/D Converter on the Analog Frontend Board, feeding these to the Arithmetical Unit through a 14 wire flat-cable (J4).

Two TMS 9902 Asynchronous Communication Controllers (QD1 and QD4) provide the Interprocessor Communication Link and the RS232C link. The RS232C link (QD1) has an option which provides optoisolation of incoming signal lines. The optoisolation can be circumvented by mounting jumper K1. The TMS 9902 QD4 further provides a timer function, which is used for delays etc. in connection with the measurement execution.

The timer of QD1 is used for housekeeping purposes (fine slicing).

Jumpers

Various jumpers on the Digital Motherboard select different setups of the Board. A complete list of these jumpers is given below:

K1 - Mounting K1 will circumvent the optoisolation on the two RS232C signal lines RX & CTS

K2 - By means of this jumper it is possible to exchange the two RS232C data-lines RX & TX.

1-2 & 3-4: select DB-25 Connector Pin 2 as RX
and DB-25 Connector Pin 3 as TX

1-3 & 2-4: select DB-25 Connector Pin 2 as TX
and DB-25 Connector Pin 3 as RX

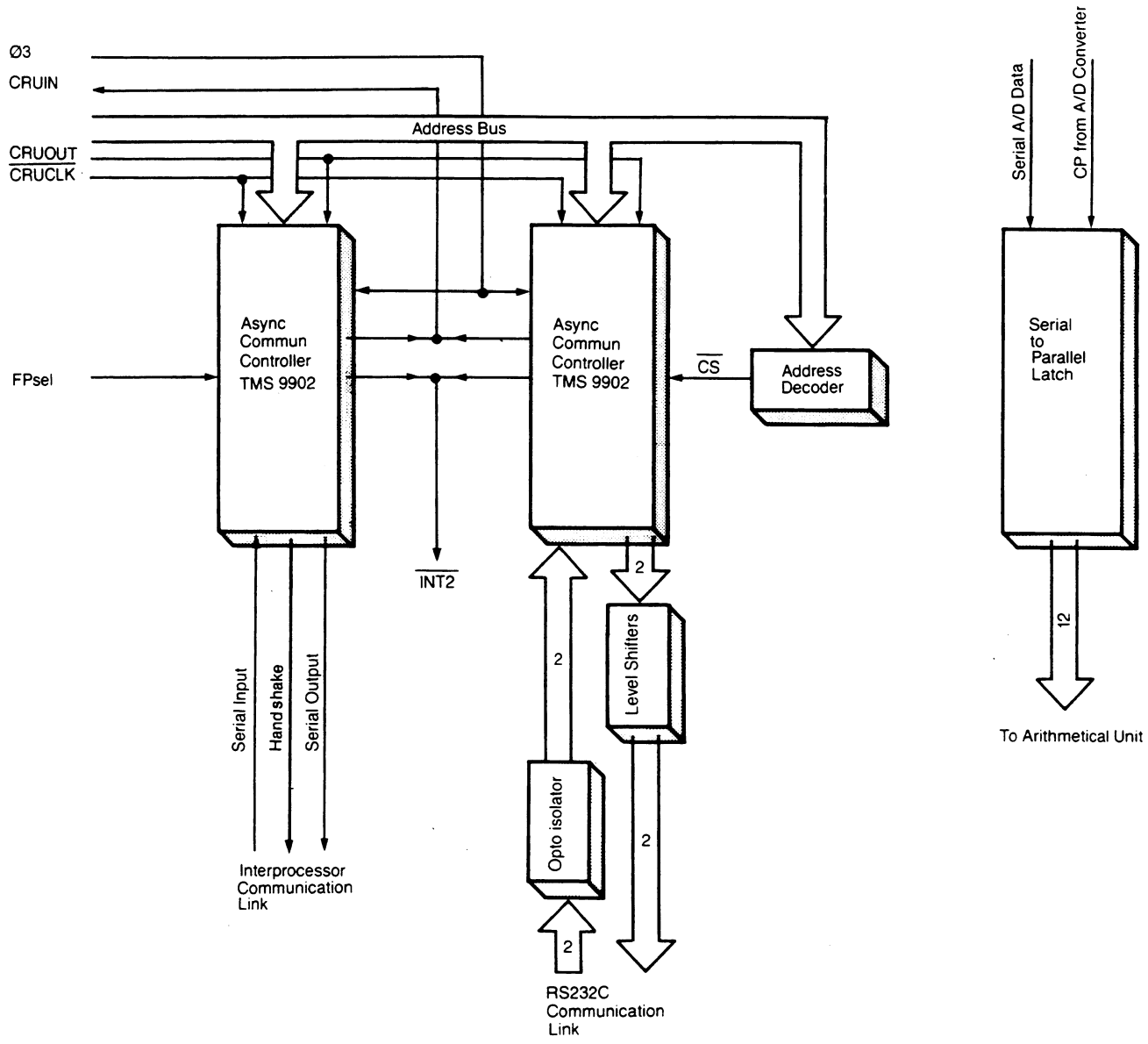


Fig. 3.3.16 - Digital Motherboard Block Diagram

K3 - Select handshake/no handshake on the RS232C Communication Link.

1-2: select CTS handshake signal active from DTE
2-3: select no handshake on Communication Link

The positions for the jumpers are highlighted in fig. 3.3.17.

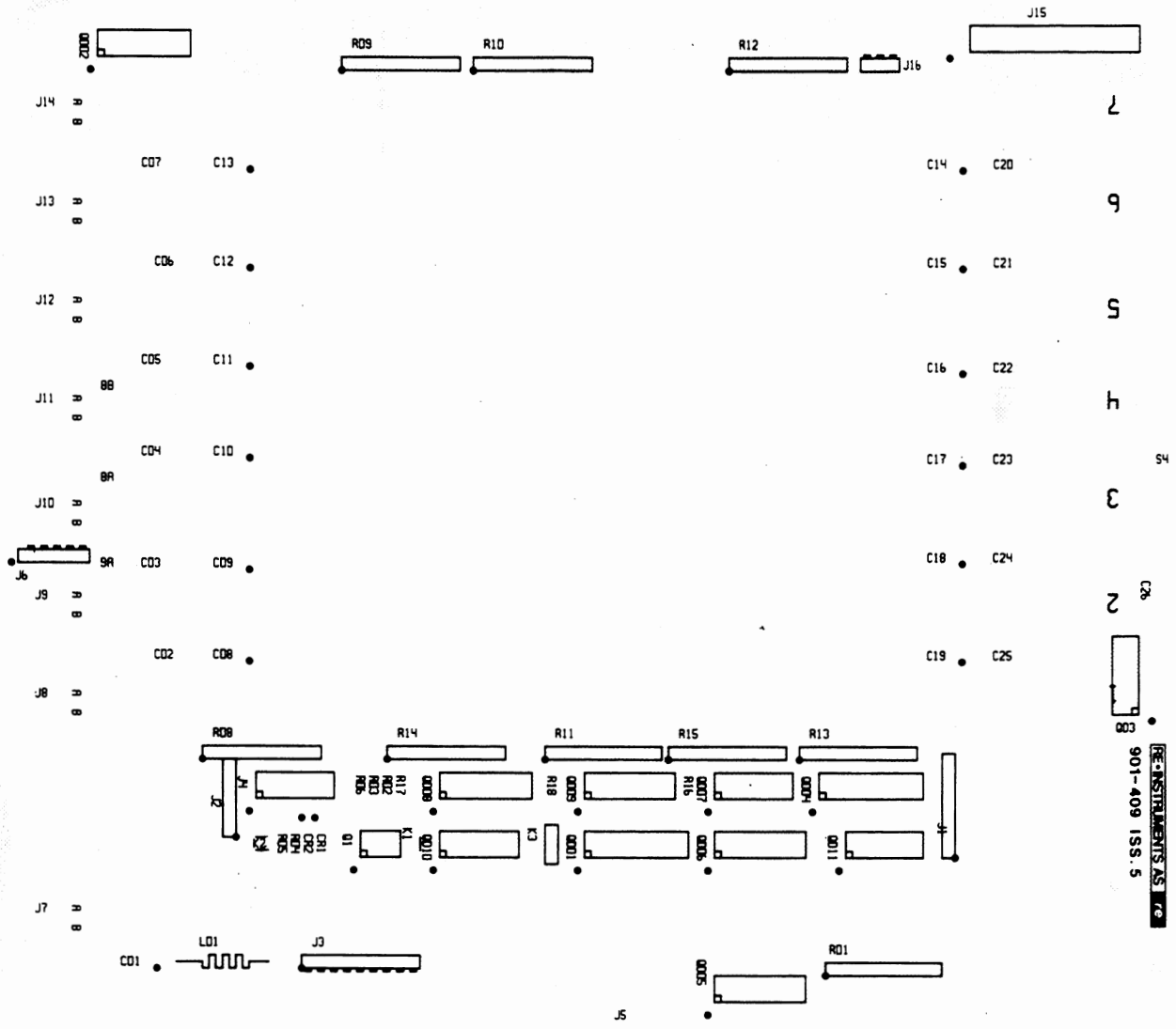


Fig. 3.3.17 - Digital Motherboard Component Layout

3.3.4 Switch Mode Power Supply

The Switch Mode Power Supply provides the instrument with +5 V/8 Amp for both the Analog and the Digital Section, +12 V/1.2 Amp for the CRT Section, and +/-15 V/150 milliamp for the Digital Section. The input voltage of +25 V unregulated DC is provided by a rectifier circuit located on the Linear Power Supply of the Analog Section.

A Block Diagram showing the essential parts of the Switch Mode Power Supply is shown in fig. 3.3.18, while the schematic diagram is shown on drawing No. 985-107.

A single-ended LC configuration is employed, built around a regulating pulse width modulator SG3524, which provides the switching pulses for the power switching element. This configuration is duplicated, making up one supply of +5 V (main elements QA1, Q1, L1, C9 and CR5) and another of +12 V (main elements QA3, Q4, L3, C25 and CR12). The +/-15 V supplies are tapped from the +5 V supply by means of supplementary windings on L1.

To describe the principles of operation, the +5 V supply is considered. The regulation is carried out by turning Q1 ON and OFF at a fixed frequency of 32 kHz, but with a variable duty cycle. During ON periods, current is supplied from the +25 V input to the energy reservoir L1 and C9. When Q1 is switched OFF, the current of L1 continues to flow via the free-run Schottky diode CR5. The controlling element, the Pulse Width Modulator QA1, varies the duty cycle to maintain constant output voltage (sensed by the voltage divider R13/R14), independent of the load current: if the load current increases, the ON period is increased and thereby, more energy is transferred through Q1 to the load.

The Pulse Width Modulators are synchronized with the Start Conversion signal ($\overline{SC}$) from the Arithmetical Unit in order to minimize the effects of the noise originating from the switching transients created during the switching of the power transistors.

A Dual Monostable Multivibrator (QD1) converts and shapes the $\overline{SC}$ signal to fit the required input of the Pulse Width Modulators. The correct appearance of the signal is shown in fig. 3.3.19. Since the Arithmetical Board generating the $\overline{SC}$ signal is supplied from the +5 V Power Supply, a relay (K1) is inserted in the signal path from the output of the Multivibrator to the oscillator input of the Pulse Width Modulators - the Pulse Width Modulators are self-oscillating if the OSC input is left open.

The output voltage obtained from the +5 Volt and the +12 Volt supplies can be adjusted by potentiometers R5 and R24, respectively. The regulation is obtained by changing the non-inverting input voltage reference to the Regulating Pulse Width Modulators.

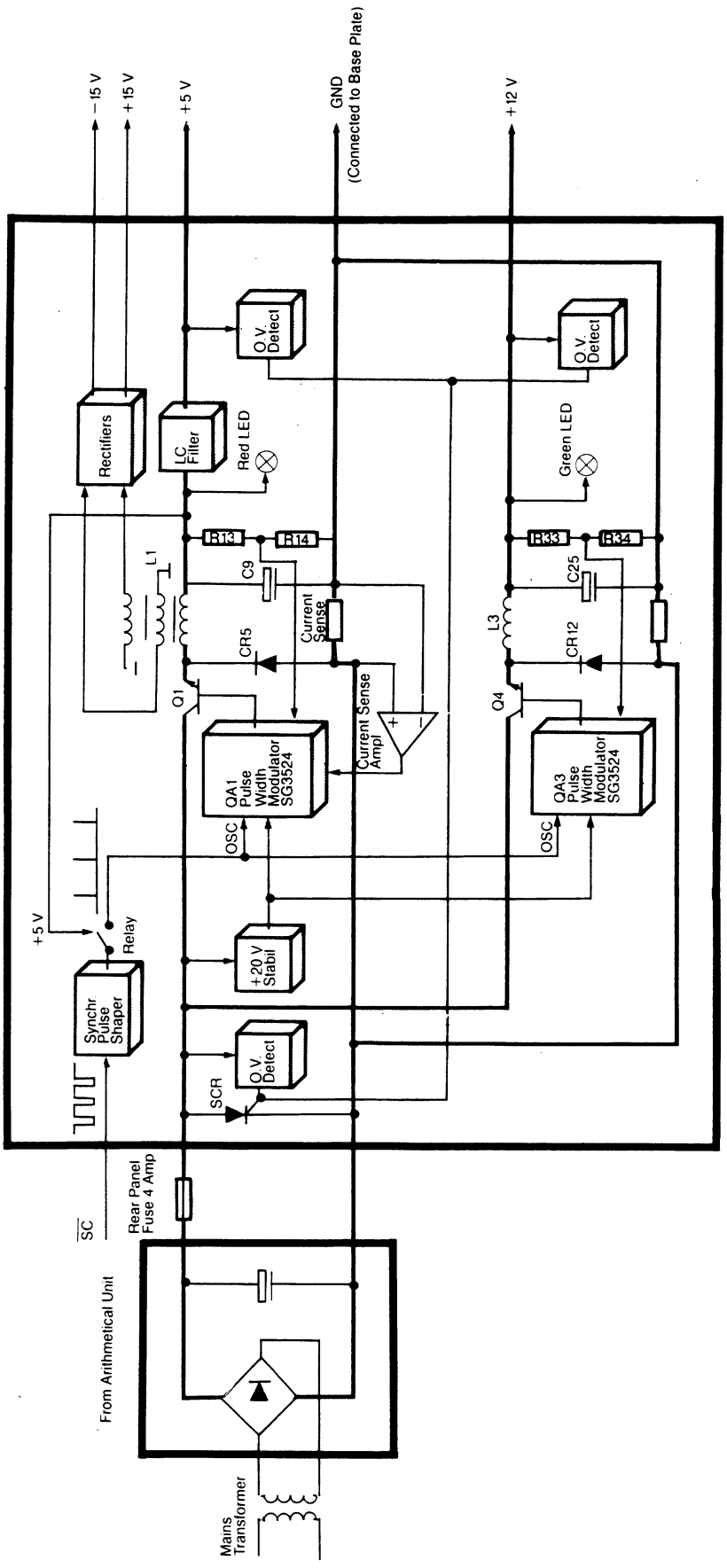


Fig. 3.3.18 - Switch Mode Power Supply Block Diagram

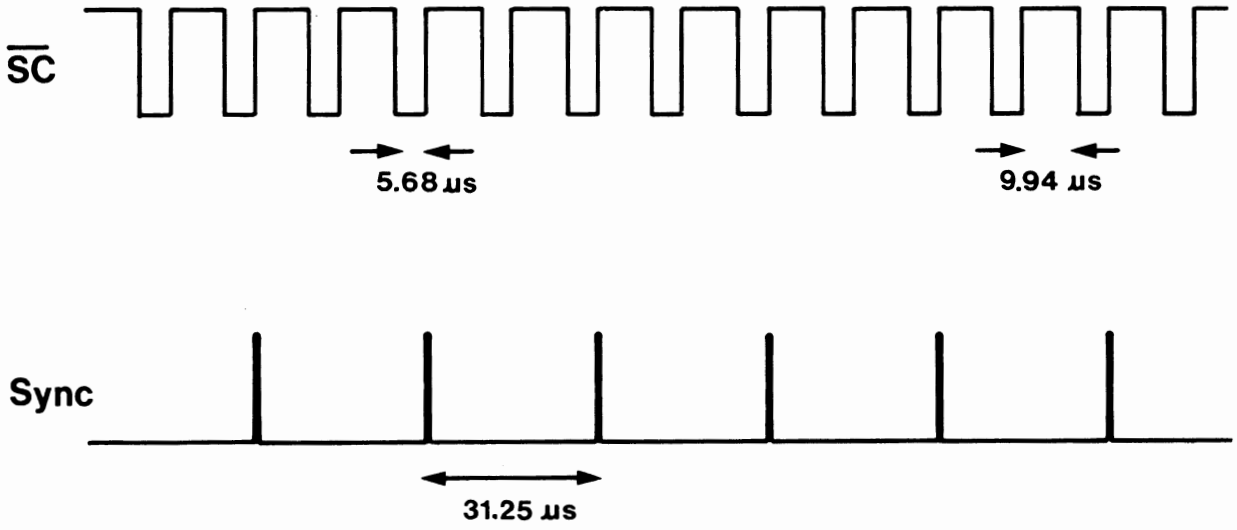


Fig. 3.3.19 - Generation of Synchronization Pulses

Protection Circuits

In order to protect the +5 Volt Power Supply from destruction in case of short circuits it is equipped with a current sensor. This sensor will shut down the Regulating Pulse Width Modulator in case of excessive current in the power resistor R12. Due to the high currents drawn from the +5 Volt Supply the current sensor is made by using a small resistor R12 together with an amplifier QA2. There is no short circuit protection on the +/-15 Volt supplies, since they are totally isolated from the rest of the power supply. A heavy load on one of these supplies is most likely to blow the diodes CR7, CR6.

In order to protect the switch transistors against inrush currents during power-up, a "soft start" is provided by CR3, R3 and R46, C5 for the +5 Volt supply and by CR11, R27 & C23 for the +12 Volt supply.

Crowbar protection in case of excessive voltages is provided by means of CR1 and applies to the 25 V input (CR15), to the +5 V supply (CR9) and to the +12 V supply (CR14).

A Red and a Green Light Emitting Diode located at the top of the Power Supply Board will announce the presence of the +5 Volt supply and the +12 Volt supply, respectively.

Test Points

Various Test Points on the Power Supply Board allow easy inspection of the fundamental signals. A complete list of these Test Points is given below. The locations of the Test Points are shown in fig. 3.3.20.

TP1 - +15 Volt regulated Supply
TP2 - GND for +/-15 Volt regulated Supply
TP3 - -15 Volt regulated Supply
TP4 - +5 Volt regulated Supply
TP5 - GND for +5 Volt regulated Supply
TP6 - +12 Volt regulated Supply
TP7 - Synchronizing pulses to the P.W.M.'s
TP8 - +5 Volt raw regulated Supply. 1)
TP9 - +12 Volt raw regulated Supply. 1)
TP10 - Regulator feedback for +5 Volt Supply
TP11 - N.U.
TP12 - GND for +12 Volt regulated Supply

Note 1: Unfiltered outputs.

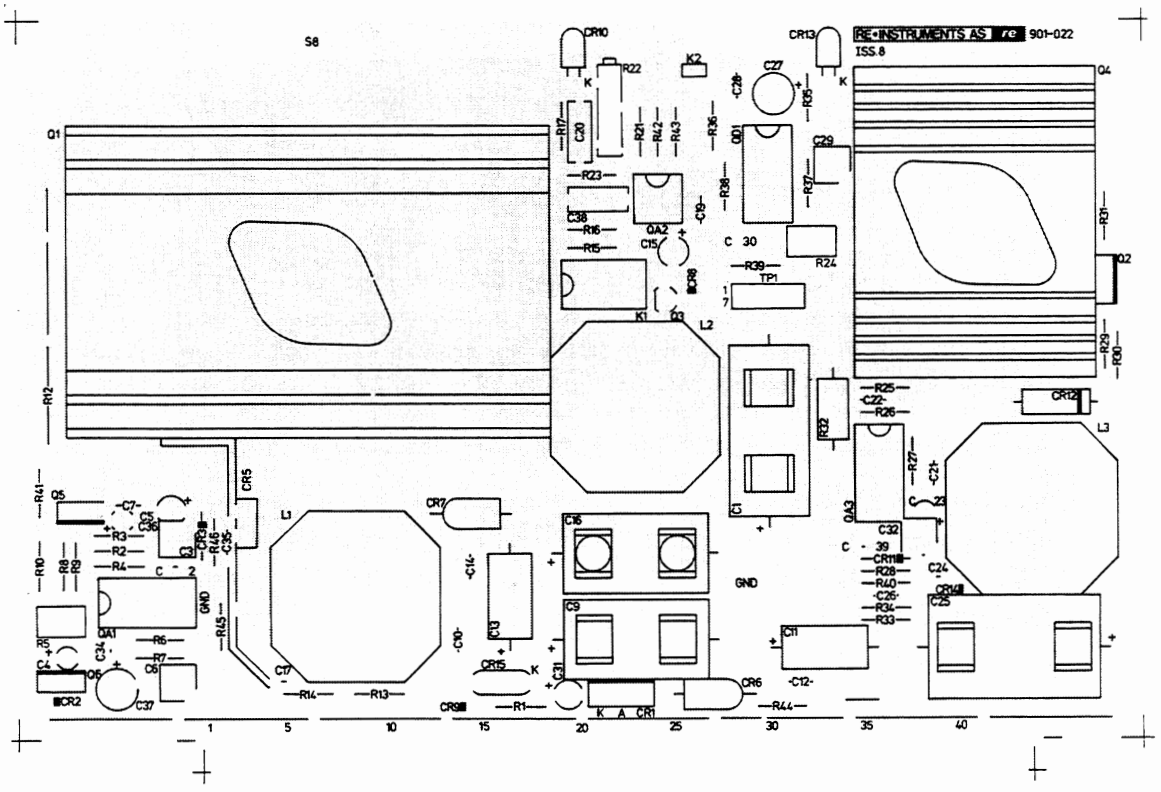


Fig. 3.3.20 - Switch Mode Power Supply Component Layout

3.4 CRT Section

The CRT Section provides the visual interface between the user and the RE201. The main purpose of the CRT Section is to display results and to guide the user through the learn mode.

The CRT Section comprises the CRT Driver (horizontal and vertical deflection circuits), the Tube Unit (video amplifier), the Deflection Unit and the 9-inch cathode ray tube (CRT).

To avoid electromagnetic interference (EMI) the CRT Section is covered by a metal shield box which is fastened to the RE201 base plate by means of 19 screws. In order to avoid radiation from the front section of the CRT tube this area is covered by a fine wire grid which is grounded to the metal shield box.

The CRT Section is controlled by separate signals for video, horizontal sync and vertical sync. All signals for the CRT are supplied from the Main CPU Board in the Digital Section. In the CRT Driver the three signals are combined to a composite video signal, which is available on a connector on the rear panel of the RE201.

The CRT Driver adjusts automatically to 625/525 lines per picture depending on whether the refresh rate is 50 or 60 cps. The brightness is controlled by three TTL lines allowing adjustment of brightness from the front panel.

3.4.1 CRT Driver 901-417

A block diagram of the CRT Section is shown in Figure 3.4.1 and the schematic diagram is shown in drawing No. 985-106.

The CRT Driver incorporates the following functions:

* Sync conditioning
* Line oscillator
* Line output stage
* Field time base
* Video conditioning
* Digital brightness control
* Internal 5 V Power Supply

Sync Conditioning

The sync conditioning circuit QD2 makes it possible to supply the CRT Section with inverted sync, non-inverted sync or composite sync. The RE201 uses separate sync with inverted vertical sync and non-inverted horizontal sync. The sync signals are controlled by the CRT Controller on the Main CPU Board in the Digital Section.

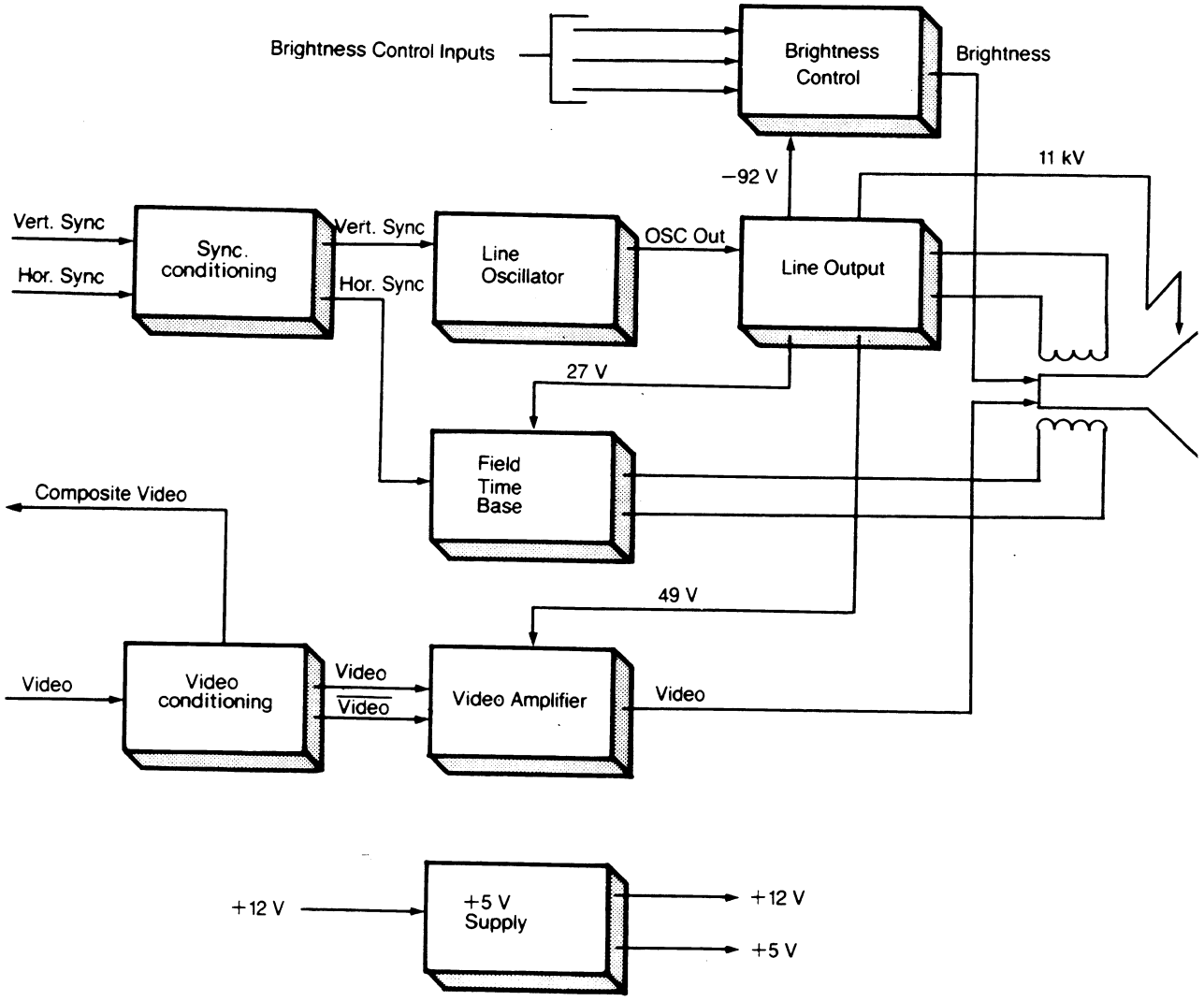


Fig. 3.4.1 - CRT Section Block Diagram

Line Oscillator

The line oscillator is built around QA1 (TDA2593), which is an integrated sync separator and line oscillator. The line oscillator circuit incorporates two adjustments: horizontal frequency and horizontal phase (electrical horizontal picture centering).

Line Output Stage

The line output transistor BU806 (Q6) is controlled by the line oscillator (QA1). Signal shaping for horizontal deflection is performed by Q6 and line output transformer TR1. TR1 supplies the picture tube with anode voltage (approximately 11 kV) and further by rectification with various grid voltages.

Several supply and control voltages for video amplifier, brightness control and field time base are generated in the line output stage.

The horizontal linearity can be adjusted by means of L1.

Field Time Base

The integrated circuit TDA2653 (QA2) is an integrated vertical deflection circuit.

TDA2653 contains vertical oscillator, synchronization circuitry and vertical output stage. The vertical ramp oscillator is boosted from the line output circuit at TDA2653 pin 11.

The field time base circuit contains adjustments for vertical linearity (R37), vertical amplitude (R4) and vertical frequency (R48).

Video Conditioning

The CRT Section may be supplied by inverted or non-inverted video signals selectable by K1 and K2. In the RE201 the non-inverted video position is used.

The video conditioning circuit outputs two video signals having opposite phase for differential inputs on the video amplifier.

A circuit combining sync and video signals for composite video is included in the video conditioning block.

Brightness Control

A binary controlled current source is used as brightness control. The current source controls the voltage drop across R5 and hereby the voltage for grid No. 1 on the picture tube.

Due to tolerances on picture tubes a basic brightness level adjustment is necessary (R6).

The binary signals for the brightness control are controlled in eight steps from a latch located on the Digital Motherboard.

Internal +5 V Supply

The CRT Section is supplied by +12 V from the Switch Mode Power Supply in the Digital Section. 5 V for the TTL circuitry is generated on the CRT Driver by QA3.

The total consumption for the CRT Section is approximately 0.8 amp (12 V).

Jumpers

A list of jumpers and their functions is given below. The locations are shown in fig. 3.4.2.

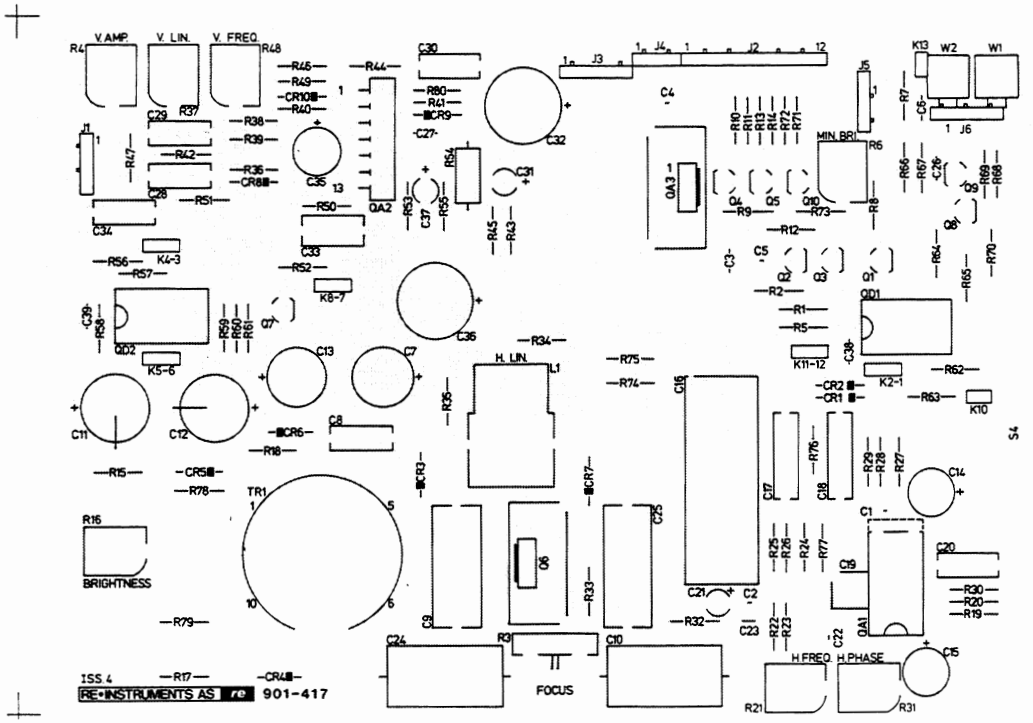


Fig. 3.4.2 - CRT Driver Jumpers

K1/K2	- K1 mounted	- non-inverted video *
	K2 mounted	- inverted video
K3/K4	- K3 mounted	- non-inverted composite or horizontal sync *
	K4 mounted	- inverted composite or horizontal sync
K5/K6	- K5 mounted	- non-inverted vertical sync
	K6 mounted	- inverted vertical sync *
K7/K8	- K7 mounted	- composite sync
	K8 mounted	- separate sync signals *
K10	- mounted	- separate sync signals *
	not mounted	- composite sync
K11/K12	- K11 mounted	- manual brightness control
	K12 mounted	- digital brightness control *
K13	- mounted	- ground to video input *
	not mounted	- capacitive ground to video input

* Indicates position used by the manufacturer.

3.4.2 Tube Unit 901-414

The Tube Unit contains the video amplifier and the spark gaps. This board is mounted directly on the picture tube socket in order to obtain the best video signal conditions.

Video Amplifier

The amplifier is of the differential type and driven by two differential video TTL signals from the CRT Driver. The amplifier is supplied from the line output stage through CR6 and R18 with +49 V.

Spark Gaps

The individual grids on the CRT Tube are supplied with very high voltages. To prevent damage on the CRT circuits in case of flashover in the picture tube, the Tube Unit is equipped with spark gaps on all socket pins.

To prevent electric shock, the rim band is connected by a green wire to the electrical ground of the spark gaps.

4 MAINTENANCE

This section describes maintenance, dismantling and adjustment procedures for the RE201 Basic Unit. Equivalent instructions for individual options are found in the pertinent technical manuals.

The reader is expected to be acquainted with the operation of the RE201.

Preventive maintenance is limited to cleaning of the dust filters. Such filters are found behind the side cover panels (upper and lower) on the left side structure, on the interior side of the bottom plate, and inside the rear filter frame. All filters should be cleaned every second month; more often if the RE201 is operated in contaminated environments.

4.1 Recommended Test Equipment

Table 4.1 lists the test equipment necessary to carry out a qualifying performance test and to adjust the RE201, if necessary. Equivalent equipment may be used, if the critical specifications are fulfilled.

Instrument	Critical Specifications	Recommended Model
1) LF Signal Generator	THD < -86 dB, Frequency range 20 Hz to 75 kHz	B&O, Model TG8
2) RMS/DC Voltmeter	Accuracy of reading 0.01 % at 20 Hz to 25 kHz	Fluke RMS differential Voltmeter, Model 8506A
3) Multi-tone Generator	8 sine wave components, individual relative levels	RE201 Audio Generator 901-500
4) DC Power Supply	DC Voltage Supply 0-15 V	Danica, TPS 20
5) Frequency Counter	Accuracy 10 ppm, frequency range 300 Hz to 25 kHz	Philips PM6674/01
6) Oscilloscope	None	

Table 4.1 - Recommended Test Equipment

In addition to the equipment listed, a simple circuit for phase shifting is required during the phase measurement test (refer to section 4.2.4).

If a test of the rear panel outputs is included, additional equipment is necessary. Details are specified in section 4.2.7.

4.2 Performance Tests

The performance test procedure describes the individual tests required to verify that the RE201 Basic Unit is operating correctly and in accordance with the specifications (as listed in section 1.4). As the measurements which can be performed by means of the RE201 to a large degree utilize the same subassemblies, only a subset of the measurements is used during the performance verification.

The tests described in the following sections emphasize the RE201 Basic Unit and should be supplemented with the performance tests prescribed for the various options installed. In the following, specific notes will be made whenever a result of a test specified for the RE201 Basic Unit is influenced by an option.

When no tolerances are stated for e.g. input level, the exact value is not critical. A tolerance of +/- 5 % is sufficient.

It is recommended to carry out all programming of the RE201 before the test is initiated. The following is a survey of the definitions necessary to carry out the entire performance test. The function numbers stated are arbitrary; they are only included for later reference purposes.

LEV0 - Channel TBD, Mode RMS25, Duration 512 ms, Representation VOLT
LEV1 - Channel BOTH, Mode RMS25, Duration 512 ms, Representation DB REF
LEV2 - Channel BOTH, Mode SEL, Window FTBH, Center Frequency 1 kHz, Representation VOLT
LEV3 - Channel BOTH, Mode SEL, Window FTBH, Center Frequency 15 kHz, Representation VOLT
LEV4 - Channel BOTH, Mode PEAK, Duration 500 ms

THD0 - Channel TBD, Frequency TRACK, 2nd to 9th Harmonics, Representation DB, Averaging LIN, 5 Loops

FREQ0 - Channel TBD, Representation HZ

PHASE0 - Duration 500 ms, Representation DEG

4.2.1 Selftest

At power-on or whenever the selftest feature is utilized, the RE201 performs a selftest of important circuit blocks, mainly digital circuits, such as program memory and the Arithmetical Unit. The exact extent of the selftest is outlined in section 5.2.

4.2.2 Test of Analog Frontend

This test verifies the proper operation of the analog input circuitry located on the Analog Frontend board. If errors are encountered during this test, the adjustment procedure is outlined in section 4.4.3.

The test includes verification of RMS level accuracy, channel separation, Peak level accuracy and Distortion measurement accuracy.

RMS Measurements

a. Adjust the LF generator (1) to a frequency of 1 kHz and an output level of 1.300 Vrms +/- 5 mV by means of the RMS voltmeter (2). Connect the generator to both channels of the RE201.

b. Activate an RMS25 measurement in the RIGHT channel with duration 512 ms and result display in Volts (LEV0), and check that the result is 1.28 V - 1.32 V.

c. Press <STO REF>.

d. Repeat b.-c. for the LEFT channel.

e. With the 1 kHz measurement as reference, check the flatness in both channels at the frequencies 20 Hz and 25 kHz by performing an RMS25 measurement with channel selection BOTH and representation in DBR (LEV1). The reading should be -0.1 dBr to +0.1 dBr.

f. Repeat the tests a.-e. for a signal level of 3 mV.

g. Adjust the generator to 6.600 V +/- 5 mV (1 kHz) and activate RMS measurements in both channels, results in Volts (LEV0). Verify that the reading is 6.60 V +/- 0.01 V for both channels.

h. Shortcircuit both inputs and check that the noise level is below 12 uV in either channel. The RE201 will issue a warning for input low.

Channel Separation

a. Terminate the LEFT channel with 600 Ohms, e.g. using the Audio Generator GND mode. Connect a 1 kHz, 5 Vrms sine wave signal to the RIGHT channel, and activate an RMS SELECTIVE measurement in BOTH channels (center frequency 1 kHz) (LEV2).

b. Verify the reading in the LEFT channel to be < 16 uV, corresponding to -110 dB. A warning for input low will be displayed.

c. Change the frequency to 15 kHz, activate an RMS SELECTIVE measurement in both channels (center frequency 15 kHz) (LEV3) and verify the reading to be < 88 uV, corresponding to -95 dB.

d. Repeat for test of separation LEFT to RIGHT.

Peak Measurements

a. Adjust the LF generator (1) to a frequency of 1 kHz and an output level of 1.000 Vrms +/- 5 mV by means of the RMS voltmeter (2).

b. Activate a PEAK measurement in BOTH channels, duration 500 ms (LEV4) and check that the result is 1.41 V +/- 0.04 V.

c. Repeat for frequencies 20 Hz, 15 kHz and 75 kHz.

Distortion Measurements

***** Note *****

If the Filter option is installed, the tests a.-b. below should be substituted by the Performance Test prescribed in section 4.3 of the Filter Option Technical Manual.

a. Apply a single-tone signal, either from the LF generator (1) or from the Audio Generator (3), with a frequency of 1 kHz and a level of 1 Vrms, to either channel of the RE201.

b. Verify that the reading for a THD measurement including 9 harmonics and 5 averaging loops, with representation in dB, is below -70 dB (THD0).

c. Define a multi-tone signal as outlined in table 4.2 with a total signal level of 1 Vrms.

Frequency	Relative Level
1000 Hz	999
2000 Hz	100
3000 Hz	50
4000 Hz	25
5000 Hz	10
6000 Hz	5
7000 Hz	2
8000 Hz	1

Table 4.2 - Multi-tone for THD test

Apply the multi-tone to either channel of the RE201, and check that the reading of the THD measurement outlined in b. is in accordance with table 4.3.

Result	Reading	Tolerance
THD	-18.8 dB	+/- 0.1 dB
2nd harmonic	-20.0 dB	+/- 0.1 dB
3rd harmonic	-26.0 dB	+/- 0.1 dB
4th harmonic	-32.0 dB	+/- 0.1 dB
5th harmonic	-40.0 dB	+/- 0.2 dB
6th harmonic	-46.0 dB	+/- 0.2 dB
7th harmonic	-54.0 dB	+/- 0.3 dB
8th harmonic	-60.0 dB	+/- 0.5 dB
9th harmonic	-80.0 dB	+/-10 dB

Table 4.3 - THD accuracy

Please note that the readings increase in fluctuation as the level of the harmonics approaches the noise floor (the quantization level of the A/D converter).

4.2.3 Frequency Accuracy

The frequency measurement accuracy test verifies the main clock oscillator. Thus, the Audio Generator Option, which utilizes the same clock, can not be used as input source.

a. Apply a sine wave signal, level 1 Vrms, to either channel of the RE201, and check that the reading of a frequency

measurement is within +/- 1.5 Hz at the following frequencies: 333 Hz, 1000 Hz and 25000 Hz (FREQ0).

b. Repeat the test for an input level of 3 mVrms.

4.2.4 Phase Measurements

This test verifies the operation of the Phase detector, located on the Analog Motherboard. If problems are encountered, the adjustment procedure to be employed is found in section 4.4.4.

a. Connect an LF generator (1), adjusted to 1 Vrms output level, to the RIGHT channel input of the RE201. Establish the phase shifting circuit as outlined in fig. 4.2.1, and insert it between the LF generator and the LEFT channel input (e.g. by means of a T-junction on the generator output).

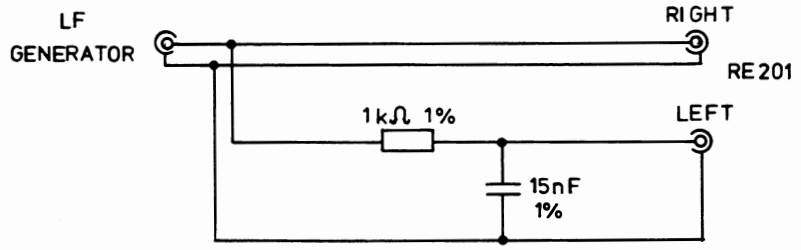


Fig. 4.2.1 - Phase Measurement Test Set-up

b. Initiate a Phase measurement, duration 500 ms and representation degrees (PHASE0). and check the phase reading in accordance with table 4.4.

Input Frequency	Reading (degrees)
930 Hz	355 +/- 1
10600 Hz	315 +/- 1
60000 Hz	280 +/- 1

Table 4.4 - Phase Test

4.2.5 DC Measurements

The DC inputs are found as follows:

DC1 - Pin 23 in the GPIO connector at the RE201 rear panel; pin positioned to the right in the BNO connector (male).

DC2 - Pin 24 in the GPIO connector at the RE201 rear panel; pin positioned to the left in the BNO connector (female).

The corresponding ground input is found at pin 25 in the GPIO connector or at the outer part of the BNO connector. The ground is connected to the RE201 structure.

If discrepancies are encountered during the test, the adjustment procedure is given in section 4.4.5.

a. Connect the DC Power Supply (4) to either of the DC1 inputs and check that the reading on the RE201, when a DC1 measurement is activated, is accurate within 128 mV at 0 Vdc, 1 Vdc and 10 Vdc input levels.

b. Repeat a. for the DC2 input.

4.2.6 Keyboard

A test comprising all buttons of the keyboard is performed as follows:

a. Press 'LEARN' and check that the green LED on the LOCAL key is turned on.

b. Press function key F1, <SYSTEM>, and check that the RE201 displays 'SYSTEM PARAMS'.

c. Press the 'cursor down' and 'cursor up' buttons one after another, and check that the cursor (>) moves down and up.

d. Press '2nd' and 'EXIT' and check that the red LED is lit when '2nd' is pressed and extinguishes when 'EXIT' is activated.

e. Press function key F5, <BASIC>, and check that the RE201 displays 'BASIC PARAMS'.

f. Press 'cursor right' and 'cursor left' and check that the cursor moves right and left.

g. Press 0 - 9 and check that all the digits when activated are displayed - in the right-handed character field in the square brackets.

h. Press '2nd' and 'EXIT'.

i. Press function key F2, <FUNCT>, and check that the RE201 displays 'ENTER FUNCTION'.

j. Press '2nd' and 'EXIT'.

k. Press function key F6, <DEFLT>, and check that the RE201 displays 'ENTER FUNCTION'.

l. Press '2nd' and 'EXIT'.

m. Press function key F3, <SEQUEN>, and check that the RE201 displays 'ENTER SEQUENCE NUMBER'.

n. Press '2nd' and 'EXIT'.

o. Press function key F7, <SETUP>, and check that the RE201 displays 'ENTER SETUP NUMBER'.

p. Press '2nd' and 'EXIT'.

q. Press function key F4, <PROGRAM>, and check that the RE201 displays 'SELECT USING SOFTKEY'.

r. Press '2nd' and 'EXIT' and '2nd' and 'EXIT'.

s. Press one by one: THD, IM, DFIM, TIM, PHASE, FREQ, SEP, LEV. Check that the RE201 starts executing each measurement when the pertinent key is activated.

t. Press '2nd' and 'TEST' and check that the RE201 performs a selftest.

u. Press 'COPY' and check that the RE201 displays 'PRINTER NOT READY' or 'PRINTING IN PROGRESS PLEASE WAIT' depending on whether a printer is connected to the RE201.

v. Press 'LEARN', 'PHASE' and function key F8, <DEFLT>, and check that the RE201 displays 'SELECT USING SOFTKEY'.

x. Press '2nd' and 'EXIT'.

4.2.7 Rear Panel Outputs

Normally, a performance test does not have to include all the rear panel outputs, as special equipment conforming to the various interfaces must be used. The rear panel outputs comprised in this test are the RS232C interface, the GPIO, the Memory Bus and the Composite Video output. For a test of the Audio Generator outputs, refer to the Technical Manual for this option.

RS232C

The RS232C interface is tested by connecting it to a line printer or a video terminal, complying to the standard. Then press COPY and verify

that the CRT display is transferred to the external device. Note that the Baud rate, the number of stop bits and the parity as configured for the RE201 in the system parameters must be in accordance with the receiving device. The RE201 always operates with 7 bit words. The pin connections are given in table 4.5. For handshake, pin 5 (CTS) should be used.

Signal	In/out	Pin No.
Rx (data in)	IN	2
Tx (data out)	OUT	3
RTS (Request to send)	OUT	4
CTS (Clear to send)	IN	5
Ground	-	7
DTR (Data Terminal Ready)	OUT	20

Table 4.5 - RS232C Pin Connections

GPIO

The binary outputs, pins 1-22 of the GPIO connector, are standard TTL outputs, i.e. HIGH ('1' in the set-up) corresponds to > 2.4 V, LOW ('Ø' in the set-up) corresponds to < 0.4 V. The outputs may be tested by the RE201 utilizing the DC inputs.

Memory Bus

The Memory Bus is most efficiently tested by connecting it to an RE INSTRUMENTS generator, equipped with a Memory Bus Interface (900-997). Alternatively, the output signals may be verified by means of a storage oscilloscope or a logic analyzer, to be in accordance with the timing diagrams depicted in fig. 3.2.12.

Composite Video

The composite video output is most conveniently tested by applying the signal to a standard TV monitor. Observe that the refresh rate defined as one of the SYSTEM PARAMETERS must be set in accordance with the line frequency for the monitor for proper functioning.

4.2.8 IEEE488 BUS INTERFACE

To verify the performance of the IEEE488 Bus Interface, access to an IEEE488 controller which operates in accordance with the IEEE488 standard protocol is required.

Connect the controller to the IEEE488 port of the RE201 by means of a standard bus cable and send the following command string:

"RS,1,8"

Note: The default IEEE488 address of the RE201 is 10.

This string will initiate an RMS level measurement with 8 msec. integration time in the right channel and the RE201 must respond by entering the REMOTE mode of operation and shortly after issue a service request to the controller.

Now perform a serial poll and verify that the status byte equals decimal 195.

Finally, let the controller fetch a result from the RE201 and verify that it is in accordance with the applied voltage (if the input is shorted, the reading should be approx. 7.0000E-6).

For examples on how to operate the RE201 by means of an IEEE488 Bus controller refer to the tutorial section in the description of the IEEE488 Commands in the RE201 Operation Manual.

4.3 Dismantling

This section gives detailed information on the dismantling of the RE201. Reassembling is not described except when special precautions are required.

The following dismantling description is subdivided into four sections.

4.3.1 Top and bottom plates, side cover panels, front cover, rear dust filters and side structures.

4.3.2 Analog Section: Fan, Analog Motherboard, Mains Transformer, I/O and Memory Bus Interface, Linear Power Supply and Keyboard. Use of Extender Board.

4.3.3 Digital Section: Shielding box, Digital Motherboard and IEEE488 Interface box. Use of Extender Board.

4.3.4 CRT Section: CRT Driver, Tube Unit, Deflection Unit and Tube.

4.3.1 Removing Outer Covers and Panels

Top Plate

Remove the two recessed head screws securing the top plate (refer to fig. 4.3.1). Remove the top plate. This is accomplished by sliding the cover backwards approx. 2 cm until it disengages along the front and rear edges.

Mounting the top plate is accomplished by pushing the front and rear edges downwards simultaneously and sliding the plate forwards until fully engaged. Fasten the screws to secure the plate.

Bottom Plate

Unscrew the two screws at the rear end of the plate and remove the plate.

Side Cover Panels

The side structures are each covered by two cover panels. Each cover panel is fixed by two screws located beneath the handles.

Two dust filters are mounted under the left side cover panels of the RE201. When reassembling the RE201 it is important that the filters are mounted correctly.

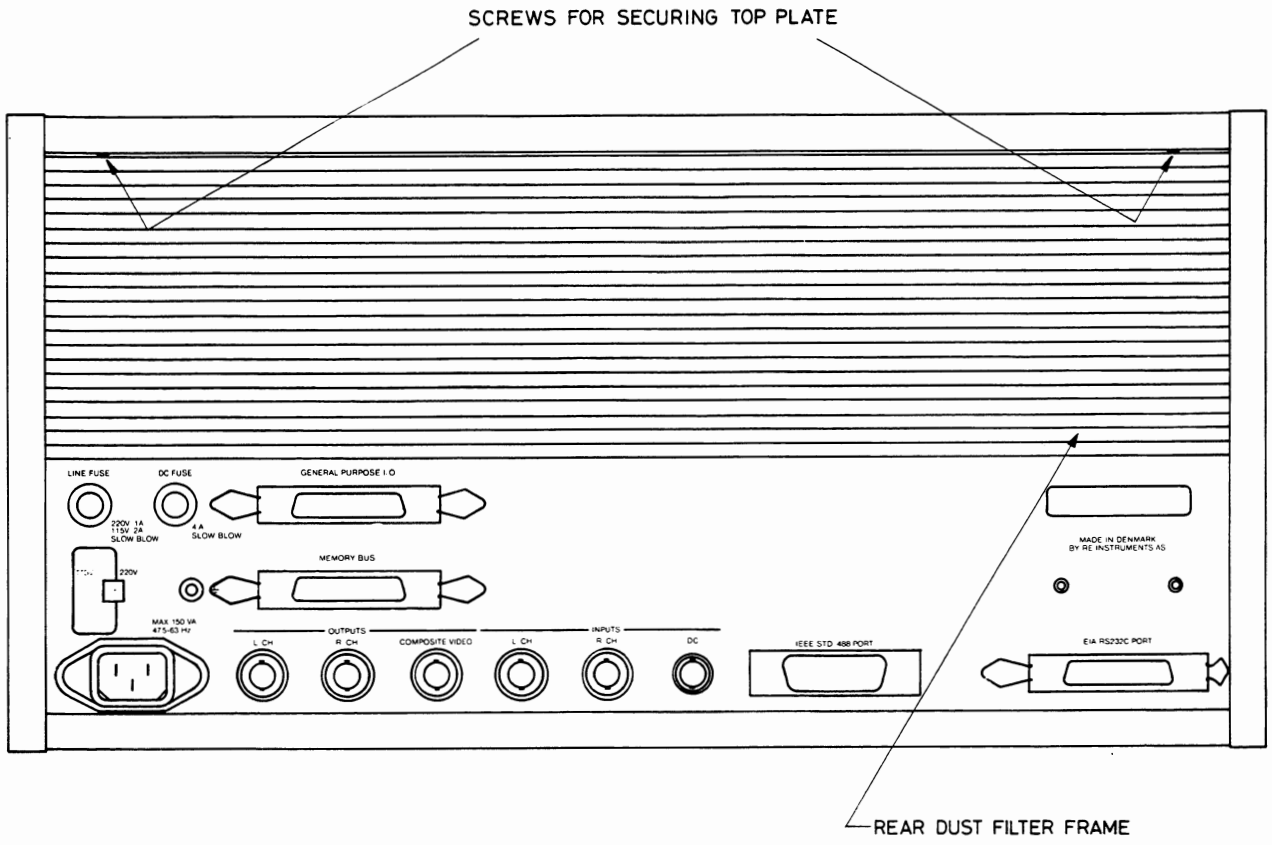


Fig. 4.3.1 - Top Plate Securing Screws

Front Cover

The front cover is removed by unfastening the two screws located at the bottom section of the front cover, and then pulling the cover outwards. Be sure to pull at the bottom and not at the top of the front cover, as pulling at the top may damage the unit.

Rear Dust Filters

The rear dust filters are placed in a frame at the rear of the RE201, as shown in fig. 4.3.1. After removing the top plate, the dust filters are removed by pushing the frame from the inside. Press at the top of the frame at both sides of the RE201 simultaneously.

The dust filter frame is locked by two adjustable snap locks on the beam above the frame. The locks are adjusted by loosening the lock

nut and adjusting the snap lock by means of a screw driver. Remember to tighten the lock nuts after the adjustment.

Side Structures

Before removing the side structures, the side cover panels and the rack mounting covers have to be removed. The rack mounting covers are located at the frontend of each side structure secured by two screws.

Before removing the screws holding the left side structure, the CRT Section has to be removed (refer to section 4.3.4).

*** Note ***

Never remove both side structures as the front and rear panels are only fixed by the side structures.

Remove the screws holding the side structure. 15 screws for the right side structure and 12 screws for the left side structure as shown in fig. 4.3.2. Two screws at each side structure holding the front frame are mounted from the inside, as shown in fig. 4.3.8. Before the right side structure is removed, it is necessary to disconnect the mains transformer connectors (2 pieces).

4.3.2 Analog Section

The Analog Section includes all non-shielded parts, placed at the right side of the RE201. It comprises of: Print magazine, Analog Motherboard, I/O & Memory Bus Interface, Keyboard and the Linear Power Supply. The locations of the PCB's are shown in fig. 3.2.1.

Before gaining access to the Analog Section, the top plate has to be removed (refer to section 4.3.1). Furthermore, the bar securing the boards in the print magazine must be removed.

Use of Extender Board (901-611)

When servicing and adjusting boards placed in the print magazine, it is often convenient to use extender boards in order to get easy access to circuitry and test points. The following describes how the extender board is inserted.

Remove all cables connecting the board to be inspected and disconnect the board by pulling the board extractors upwards. Place the extender board in the slot from which the board was extracted and place the board on top of the extender board. Connect extender cables (see below) to the board and the associated cables.

The extender board and various extender cables are included in a maintenance kit available from the factory (part No. 906-037). Refer to section 1.3.3 for a description of this service kit.

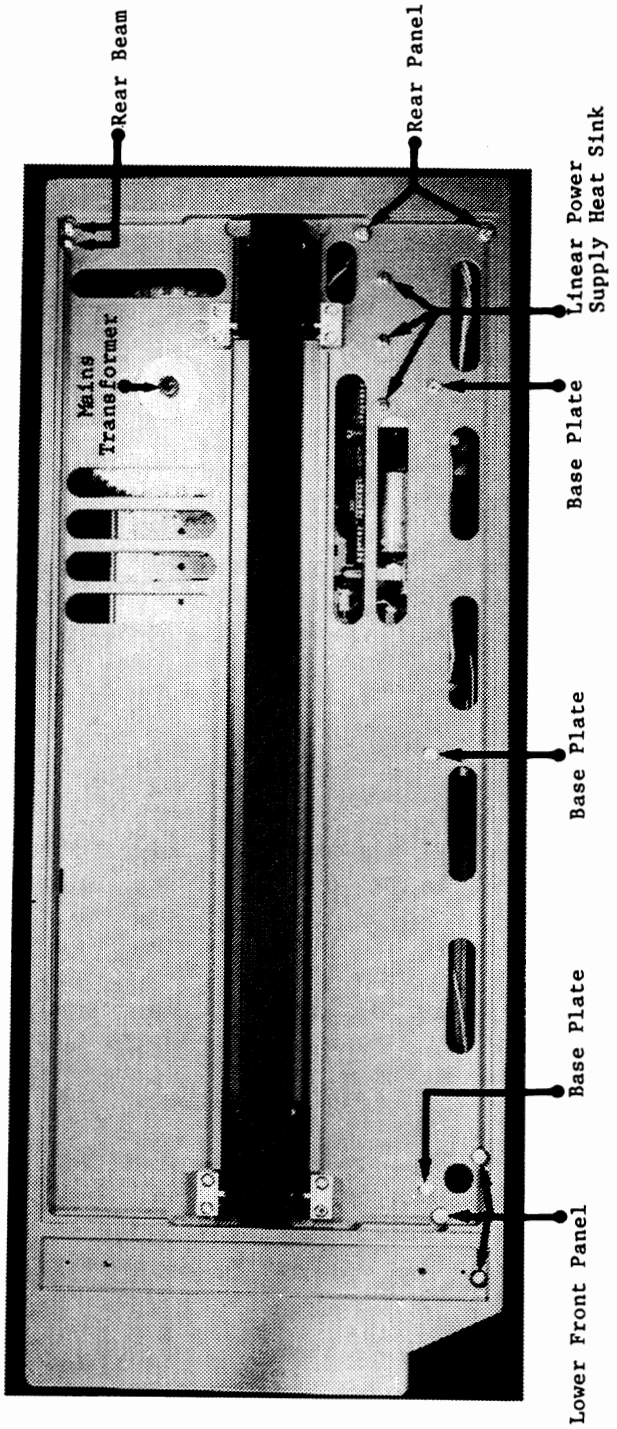


Fig. 4.3.2 - Right Side Structure

When mounting the Analog Frontend (901-421) on an extender board, only cables connecting to J1, J2 and J3 (J1 - input, J2 and J3 option connections) must be extended. The three coaxial cables W1, W2 and W3 at the right edge of the board (refer to fig. 4.3.3) do not need to be disconnected, as they are of sufficient length.

Fan

Disconnect the cable connected to the fan. Unscrew the two upper nuts holding the fan frame. Pull the fan out of the frame, starting at the left side (next to the CRT Section) and move the fan towards the CRT Section (refer to fig. 4.3.4).

Analog Motherboard (901-405) and Print Magazine

The Analog Motherboard may be removed without removing the plug-in boards, if a screw driver for recessed head screws with a blade length of min. 170 mm is used. Alternatively, all PC boards in the print magazine must be removed by disconnecting cables and pulling the board extractors upwards.

Remove the fan as outlined above.

Remove 3 connectors from the Analog Motherboard and one from the I/O Memory Bus Interfaces as shown in fig. 4.3.5 and unfasten the input cables and Audio Generator cables from the clamps on the print magazine. Unscrew the four screws, one placed in each corner of the Analog Motherboard.

Pull the Analog Motherboard and the print magazine towards the front of the RE201 until the connector connecting the Linear Power Supply at the rear end of the Analog Motherboard disengages. Lift out the Analog Motherboard and print magazine.

The print magazine is fixed to the Motherboard by two screws located beneath the board.

Mains Transformer

Before removing the mains transformer, the top plate and upper cover panel on the right side structure have to be removed (refer to section 4.3.1).

Remove the nut securing the transformer. As the transformer is very heavy, it is recommended to hold it with one hand while removing the bolt in order not to damage the boards below in case the transformer should be dropped.

Disconnect the connecting cables (2 pieces) while holding the transformer, and remove it.

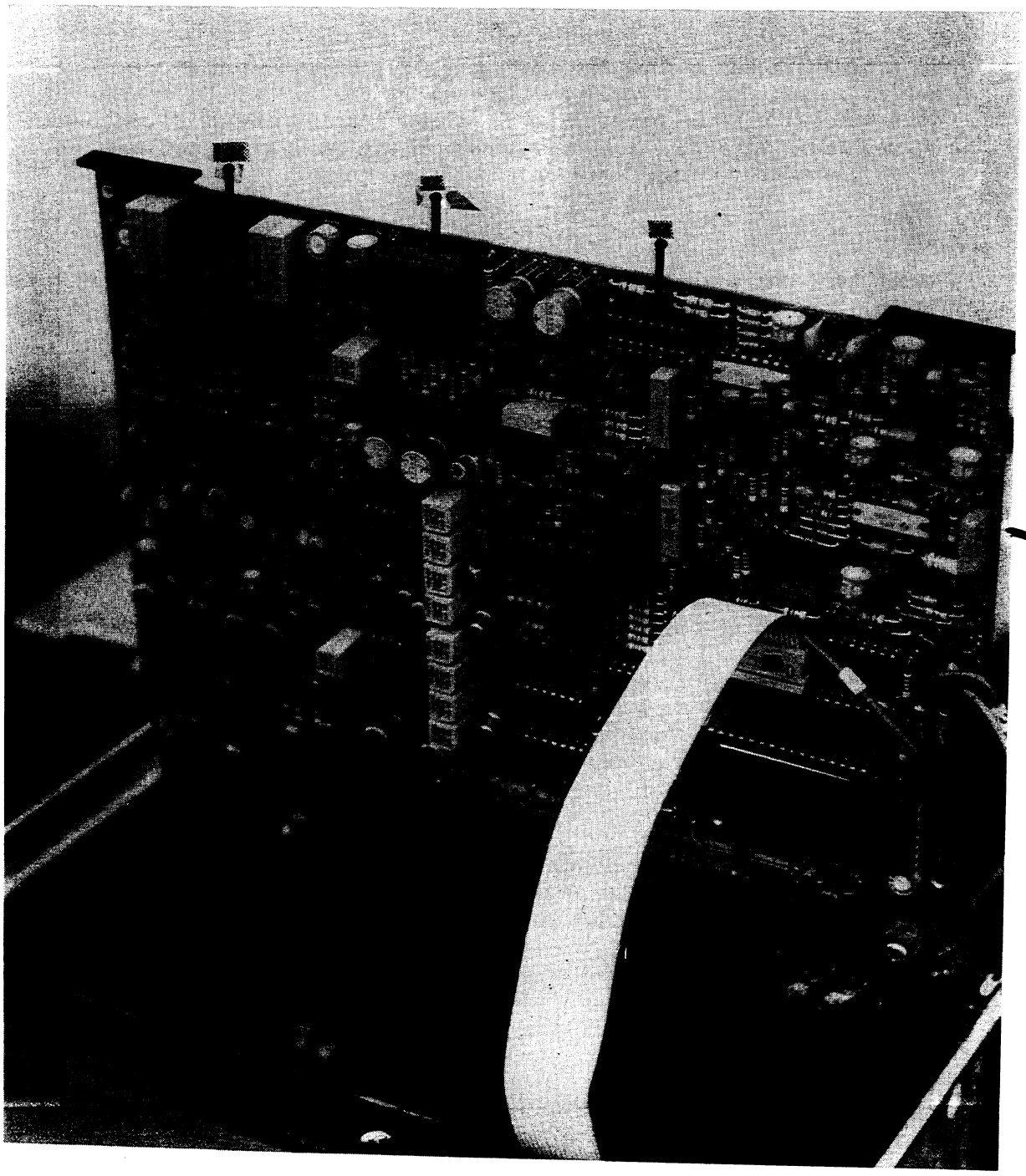


Fig. 4.3.3 - Analog Frontend on Extender Board

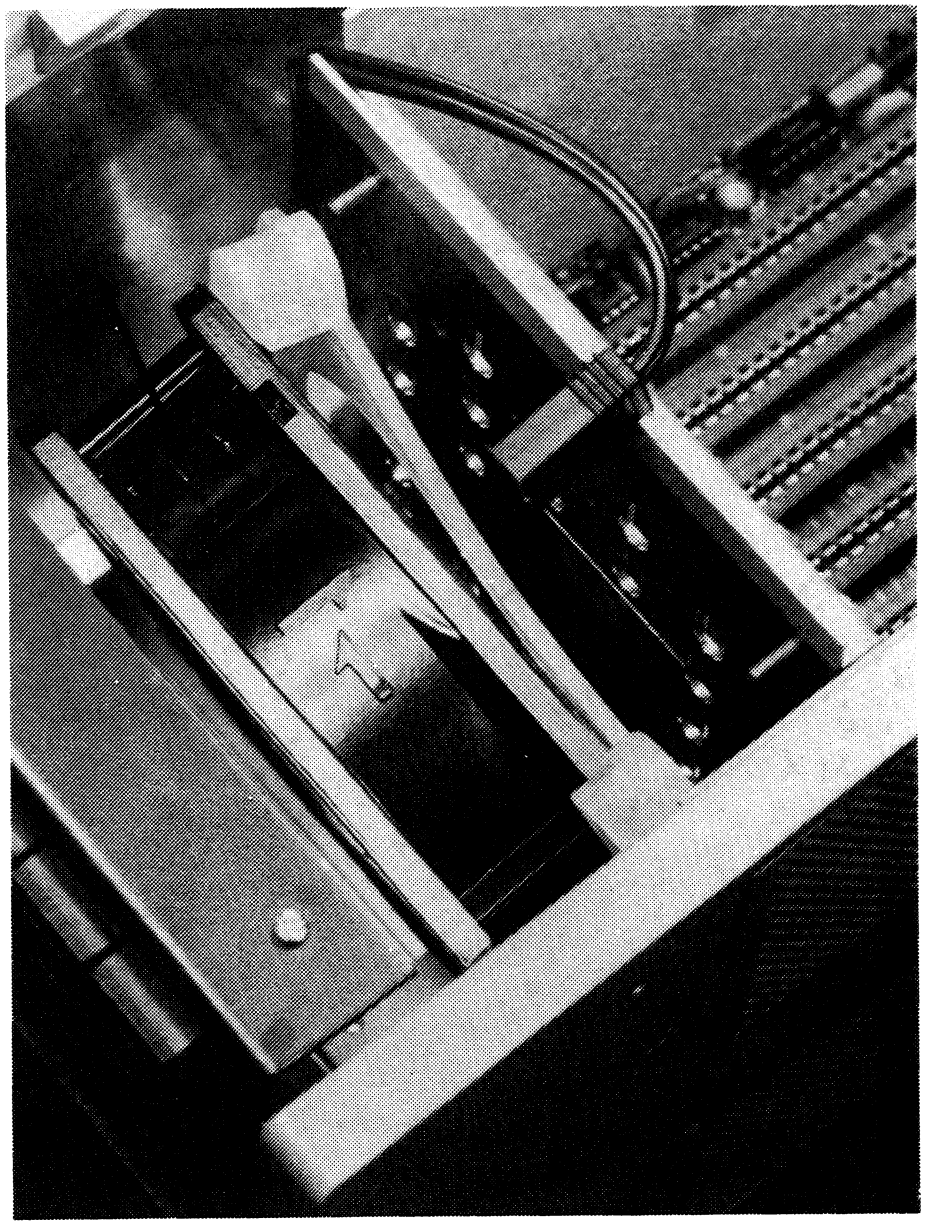


Fig. 4.3.4 - Removing the Fan

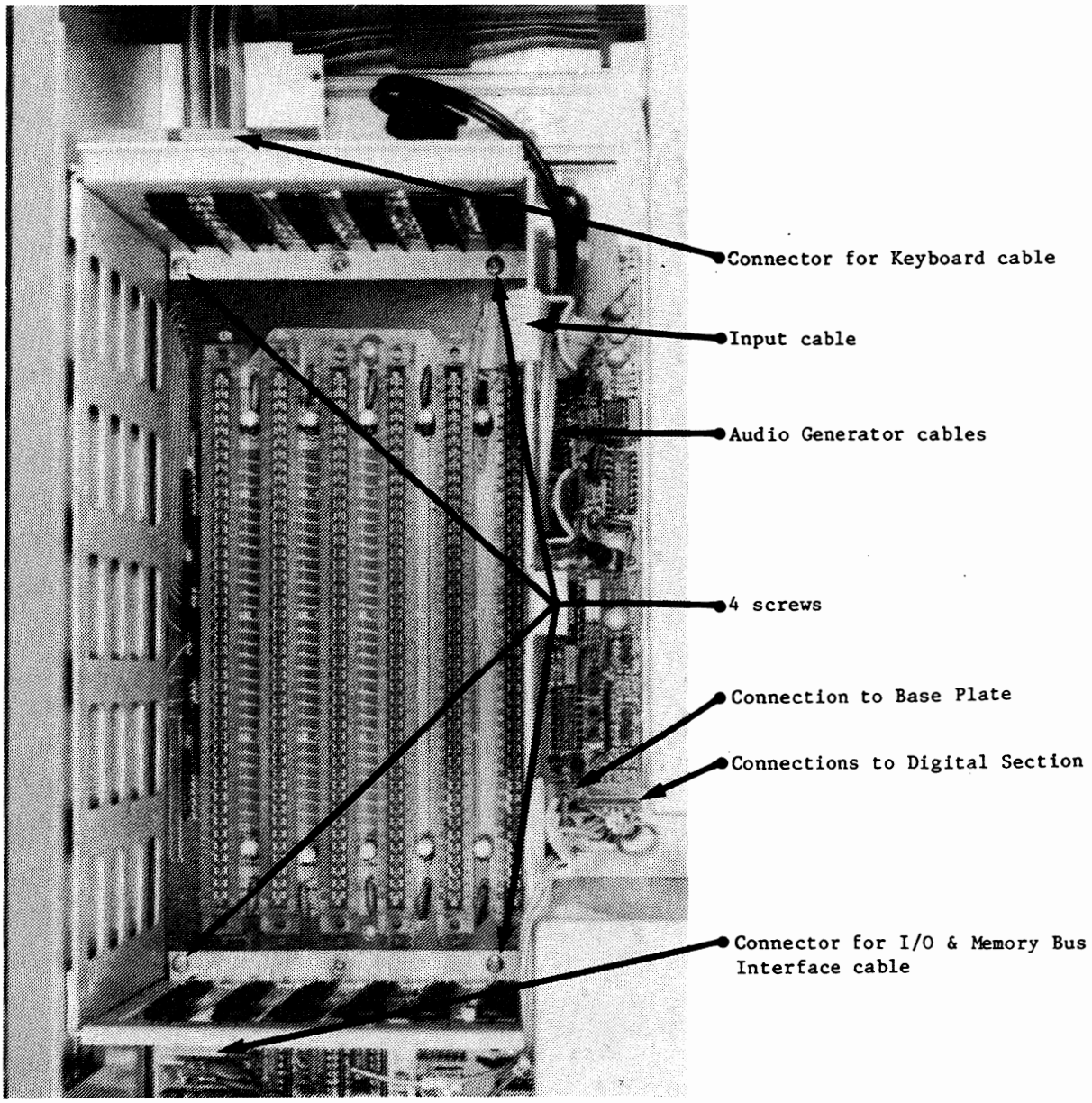


Fig. 4.3.5 - Analog Motherboard Connectors and Screws

I/O & Memory Bus Interface (901-407)

Before removing the I/O & Memory Bus Interface, located below the mains transformer, it is convenient to remove either the mains transformer (refer to the section above) or the shielding box of the Digital Section (refer to section 4.3.3).

Disconnect all connecting cables (3 pieces, refer to fig. 4.3.6) and carefully pull the board upwards to disengage the snap-on stands.

Linear Power Supply (901-406)

Before removing the Linear Power Supply the Analog Motherboard, the shielding box of the Digital Section, the Mains Transformer and the I/O & Memory Bus Interface have to be removed (refer to previous parts of this section).

Remove the lower part of the right side panel cover. Remove the three screws at the rear end of the right side structure holding the heat sink of the Linear Power Supply (refer to fig. 4.3.2).

Unscrew the four screws in each corner of the Linear Power Supply and the rectifier mounting screw located in the center of the board (refer to fig. 4.3.7).

Disconnect the connector J3 shown in fig. 4.3.7 and remove the Linear Power Supply.

Keyboard (901-410)

Before removing the Keyboard, the Analog Motherboard has to be removed (refer to previous parts of this section). However, if a very short (max. 80 mm) screw driver for 3 mm recessed head screws is available, only the fan on the analog print magazine has to be removed.

Disconnect the flat cable connecting the Keyboard to the Analog Motherboard. Unscrew the four screws securing the Keyboard (refer to fig. 4.3.8). Carefully move the Keyboard to the right and take it out.

4.3.3 Digital Section

All PCB's in the Digital Section are installed in a print magazine, fixed to the Digital Motherboard. The Digital Section is covered by a shielding box, which is secured to the Base Plate. Before dismantling the Digital Section, the top and bottom plates and rear dust filter frame have to be removed (refer to section 4.3.1).

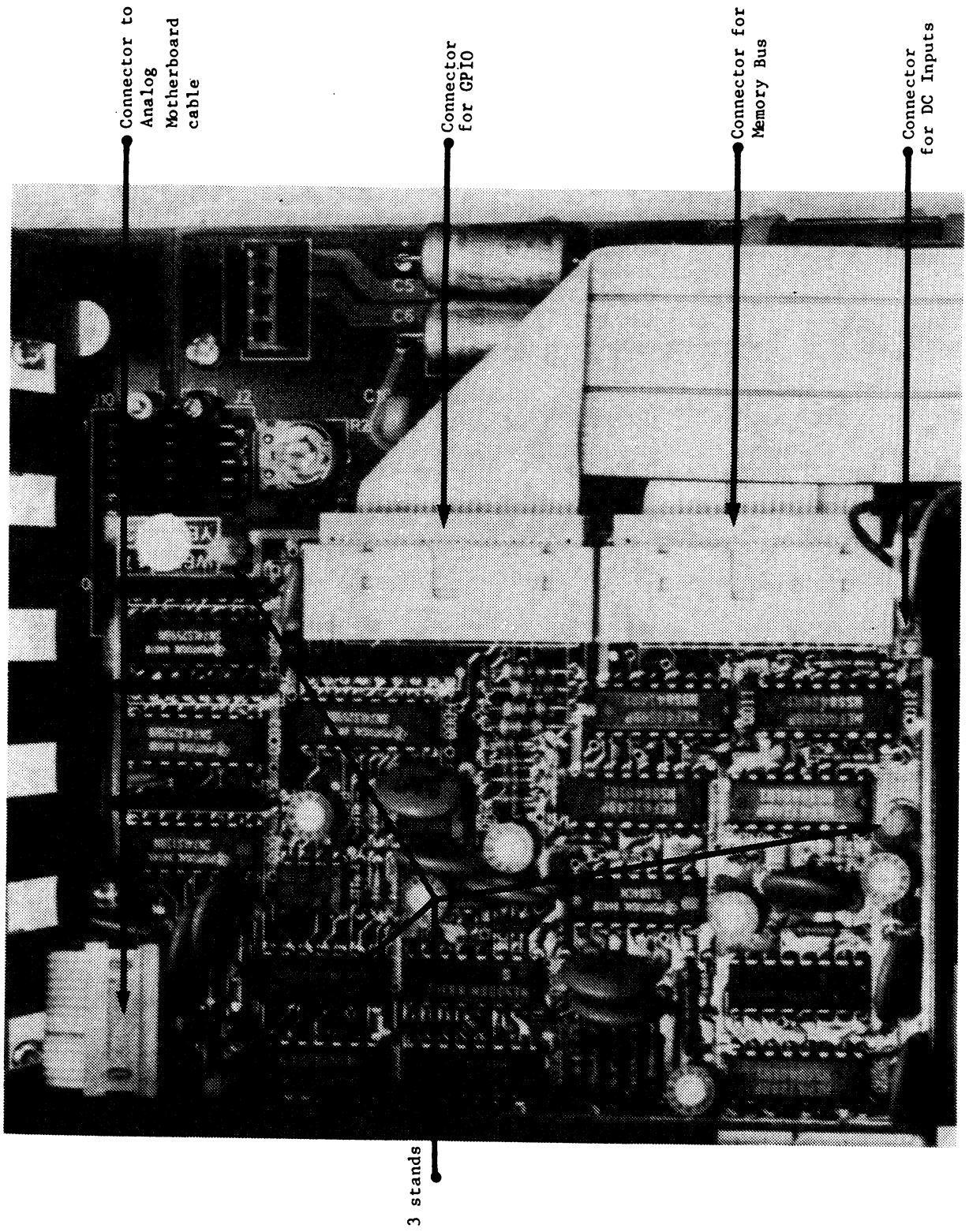


Fig. 4.3.6 - I/O & Memory Bus Interface Connectors and Stands

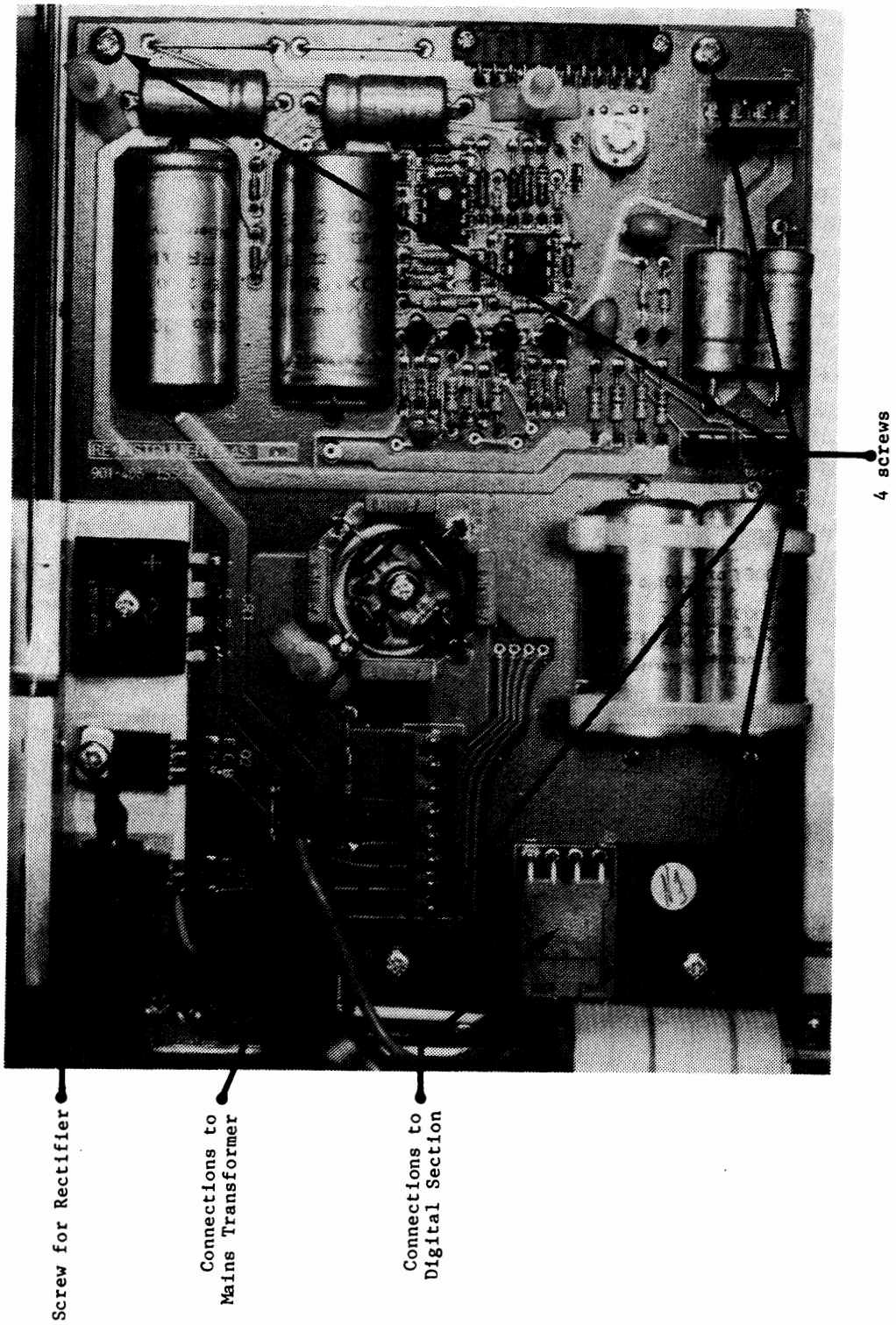


Fig. 4.3.7 - Linear Power Supply Connectors and Screws

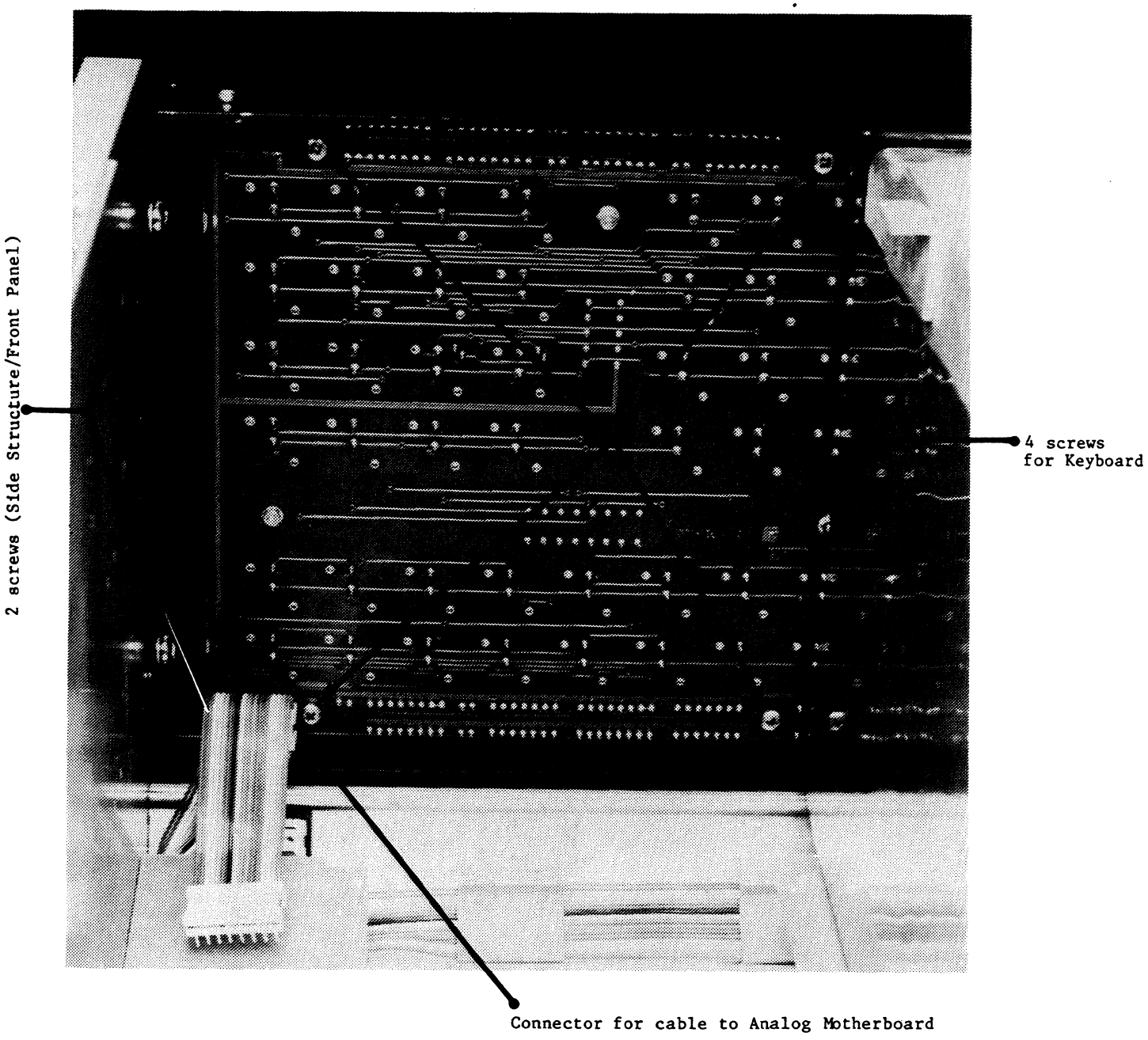


Fig. 4.3.8 - Keyboard Connector and Screws

Shielding Box

Unscrew the 18 screws securing the shielding box to the Base Plate. The screws are located beneath the Base Plate (refer to fig. 4.3.9).

Disconnect the cable connecting the fan mounted on the shielding box. Move the shielding box as far to the left as possible. Then move the box upwards.

Reassembling should be done very carefully due to the gasket placed in a groove in the Base Plate. When the shielding box is moved to the right in order to get it in the final position, it should be lifted a few millimetres. Otherwise, the gasket may be forced out of the groove or damaged. Damaging this gasket will increase EMI.

Use of Extender Board (901-611)

When servicing plug-in boards in the Digital Section, it is often convenient to mount these on extender boards as described in the following. The location of individual PCB's is shown in fig. 3.3.1.

Disconnect the cable attached to the board, if any. Remove the board by pulling the board extractors upwards. Place the extender board in the slot where the board was located and mount the board on top of the extender board. Connect the extender cables between the board and the associated cable if required.

***** Warning *****

No other boards than the Switch Mode Power Supply is to be mounted in the slot next to the CRT Section (No. 0).

Mounting a board in this slot will cause immediate damage to the board even if the RE201 is not powered, due to capacitors located on the Linear Power Supply.

Digital Motherboard (901-790)

Before removing the Digital Motherboard the shielding box covering the Digital Section has to be removed (refer to previous parts of this section).

Remove all boards mounted in the print magazine. Unscrew the six screws securing the Digital Motherboard (refer to fig. 4.3.10). Disconnect all attached cables (4 pieces) and bend the cables upwards.Remove the IEEE488 cable from the cable clamps. Lift out the Motherboard. Be careful to ensure that no cables or filters mounted on the Base Plate are damaged. When remounting the Digital Motherboard, remember to install the IEEE488 cable in the cable clamps.

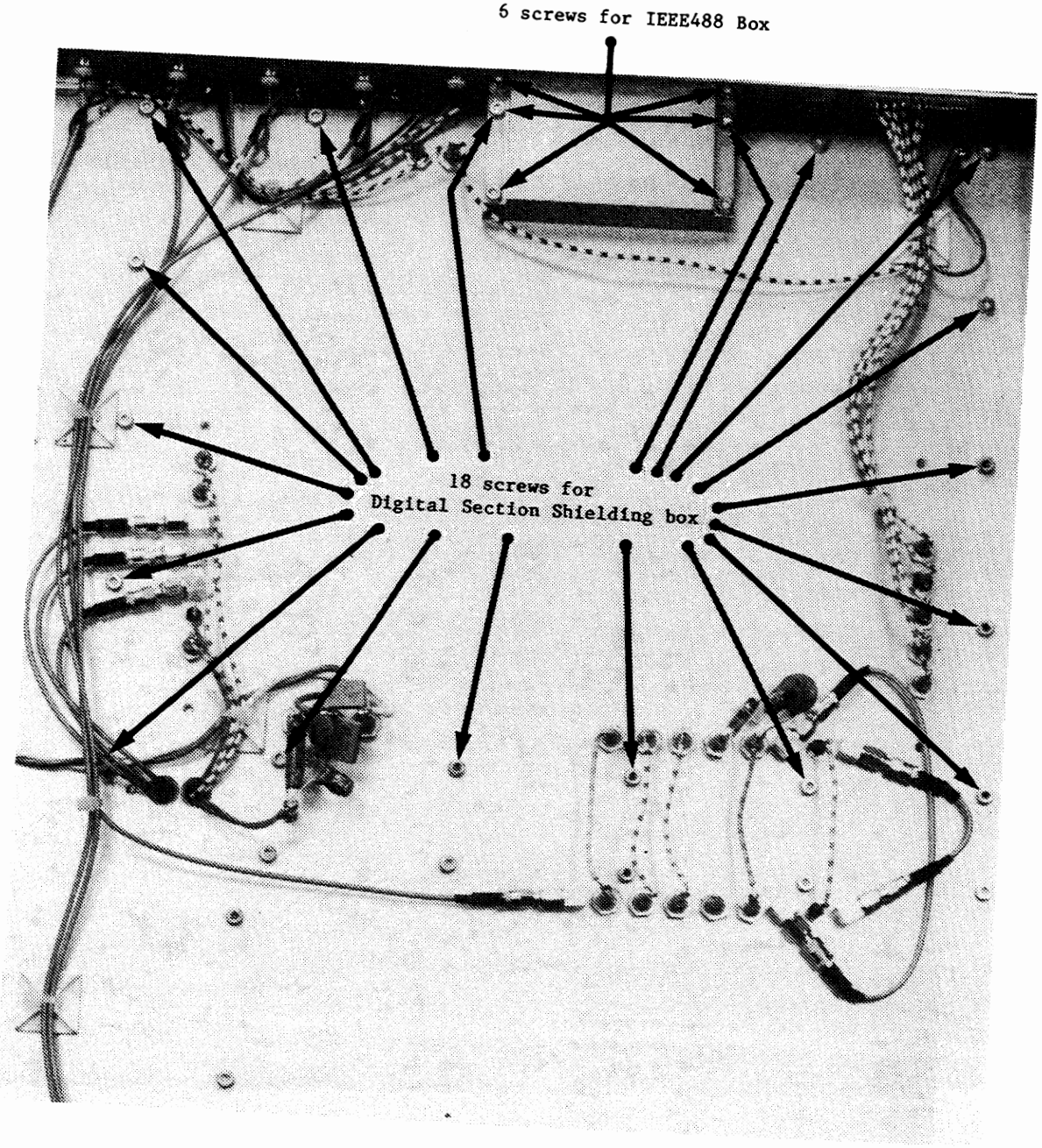


Fig. 4.3.9 - Digital Section Shielding Boxes Screws

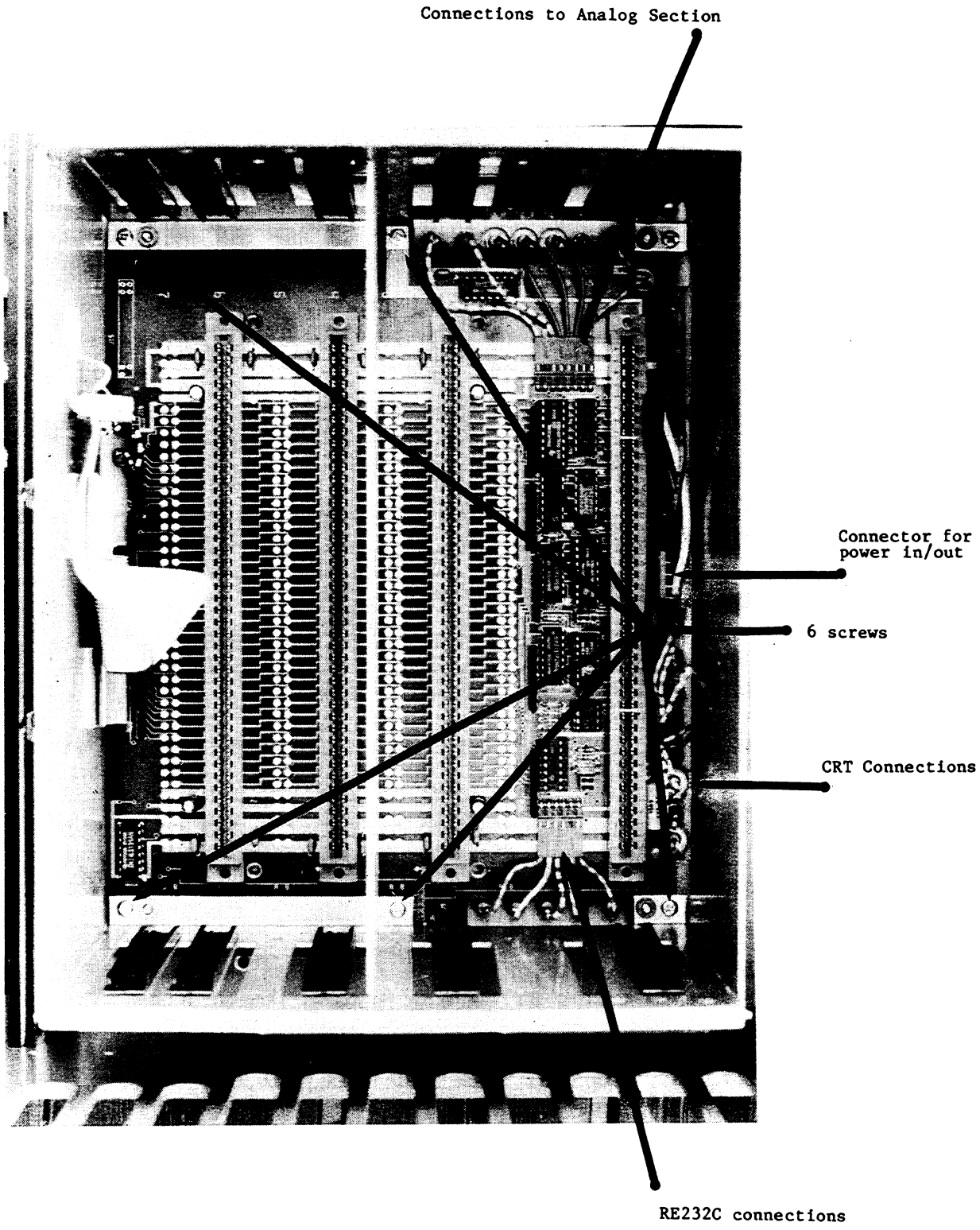


Fig. 4.3.10 - Digital Motherboard Connectors and Screws

IEEE488 Interface Box

The IEEE488 interface box is a small box placed beneath the Base Plate at the rear of the RE201.

If the internal IEEE488 cable or connector is damaged, the box has to be removed in order to replace or repair the cable or connector.

Remove the six screws securing the box and move it towards the RE201 front (refer to fig. 4.3.9). Disconnect the IEEE488 cable, either from the Main CPU.

When reassembling the box be sure that the gasket fitting in a groove in the Base Plate is placed correctly in the groove and not damaged. Damage to the gasket will increase EMI.

The IEEE488 connector may be removed by unscrewing the two screws fixing it to the box.

4.3.4 CRT Section

The CRT Section is configured of a shielding box into which the electrical circuitry is mounted. When removing the shielding box from the RE201, the entire CRT Section is dismantled.

Before removing the CRT Section the top and bottom plates have to be removed (refer to section 4.3.1). In order not to damage the front cover and to ease reassembling it is recommended to remove the front cover.

Removing the CRT Section

Unscrew the 20 screws fixing the CRT Section to the Base Plate. The screws are located beneath the Base Plate (refer to fig. 4.3.11). 7 screws, accessed through holes in the lower front profile do not have to be removed but only unscrewed (captive screws).

Move the CRT Section towards the Digital Section and lift it out very carefully. Place the CRT Section upside down beside the RE201 as shown in fig. 4.3.12.

If the unit has to be completely dismantled, it is necessary to remove all attached cables.

When the CRT Section is to be mounted in the RE201 special care should be taken to the cables connecting the CRT Section to the RE201. Check that the cables are placed inside the CRT box and not between the CRT Driver PCB and the Base Plate. This may easily be done if a hand is held under the CRT Section through the front panel (front cover

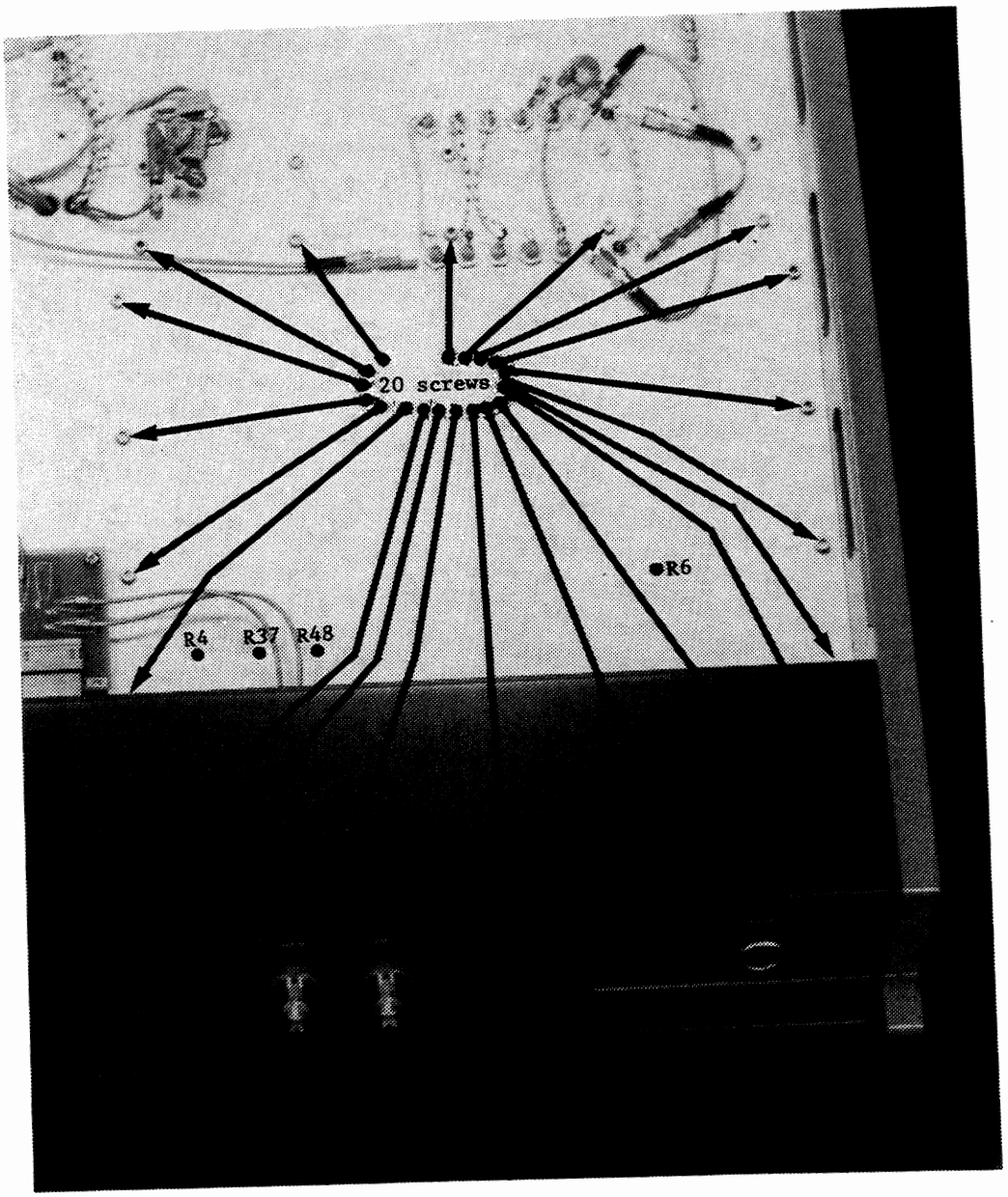


Fig. 4.3.11 - CRT Section Screws and Adjustment Holes

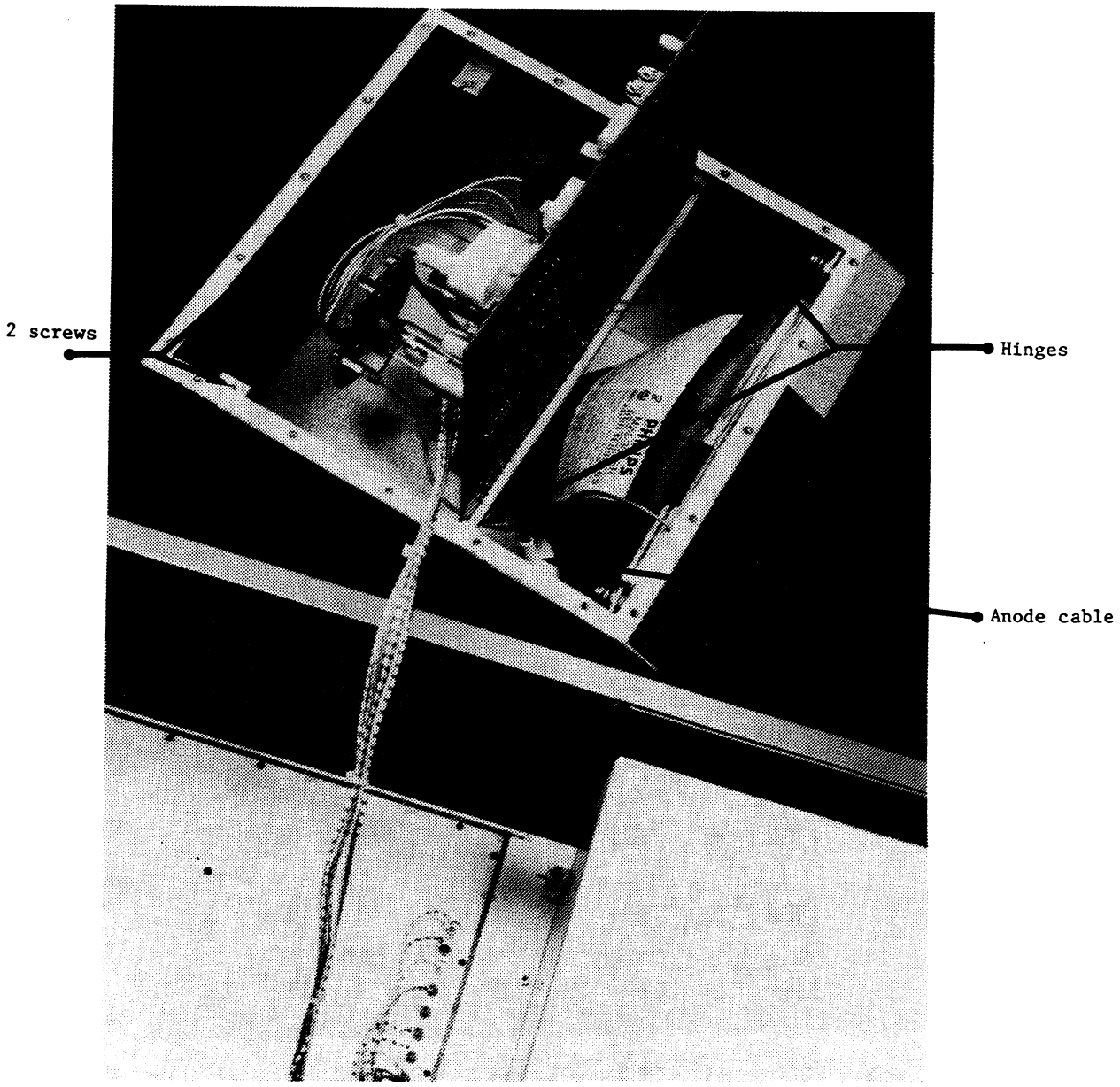


Fig. 4.3.12 - CRT Section Dismantled

removed), putting the cables into the CRT box when it is placed in the RE201.

CRT Driver (901-417)

Before removing or servicing the CRT Driver the CRT Section has to be removed from the RE201.

Unscrew the two screws securing the CRT Driver (refer to fig. 4.3.12).

When the CRT Driver is being serviced or during disconnection of the board it may be fixed in an upright standing position (refer to fig. 4.3.12).

For removal of the CRT Driver the attached cables are disconnected and the board is placed in a 45 deg. position and removed from the hinges in both sides of the board.

Be careful when disconnecting the anode cable connected to the one side of the tube.

***** Caution *****

Do not touch the anode of the tube as it carries very high voltage (11 kV). Even after very long periods without power on the RE201, a few kilovolts may be present at the anode.

Tube Unit (901-414)

Disconnect attached cables and wires and remove the Tube Unit very carefully from the the tube connector. Any strain to the tube neck may damage the tube.

Deflection Unit

Before removing the Deflection Unit, the CRT Driver and the Tube Unit must be removed (refer to previous parts of this section).

Unfasten the screw on the clip holding the Deflection Unit in place on the tube neck. Move the Deflection Unit very carefully off the neck, in order not to damage the tube neck.

CRT

Before removing the tube the CRT Driver, the Tube Unit and the Deflection Unit must be removed.

Place the CRT shielding box with the front downwards, the tube neck pointing upwards. Remove the four screws securing the tube. Remove the tube by holding around the neck and carefully lifting it out of the shielding box. Now handle the tube as shown in fig. 4.3.13.

***** Note *****

The person handling the tube should be wearing protective glasses and a scarf in case the tube is dropped as this might cause the tube to implode.

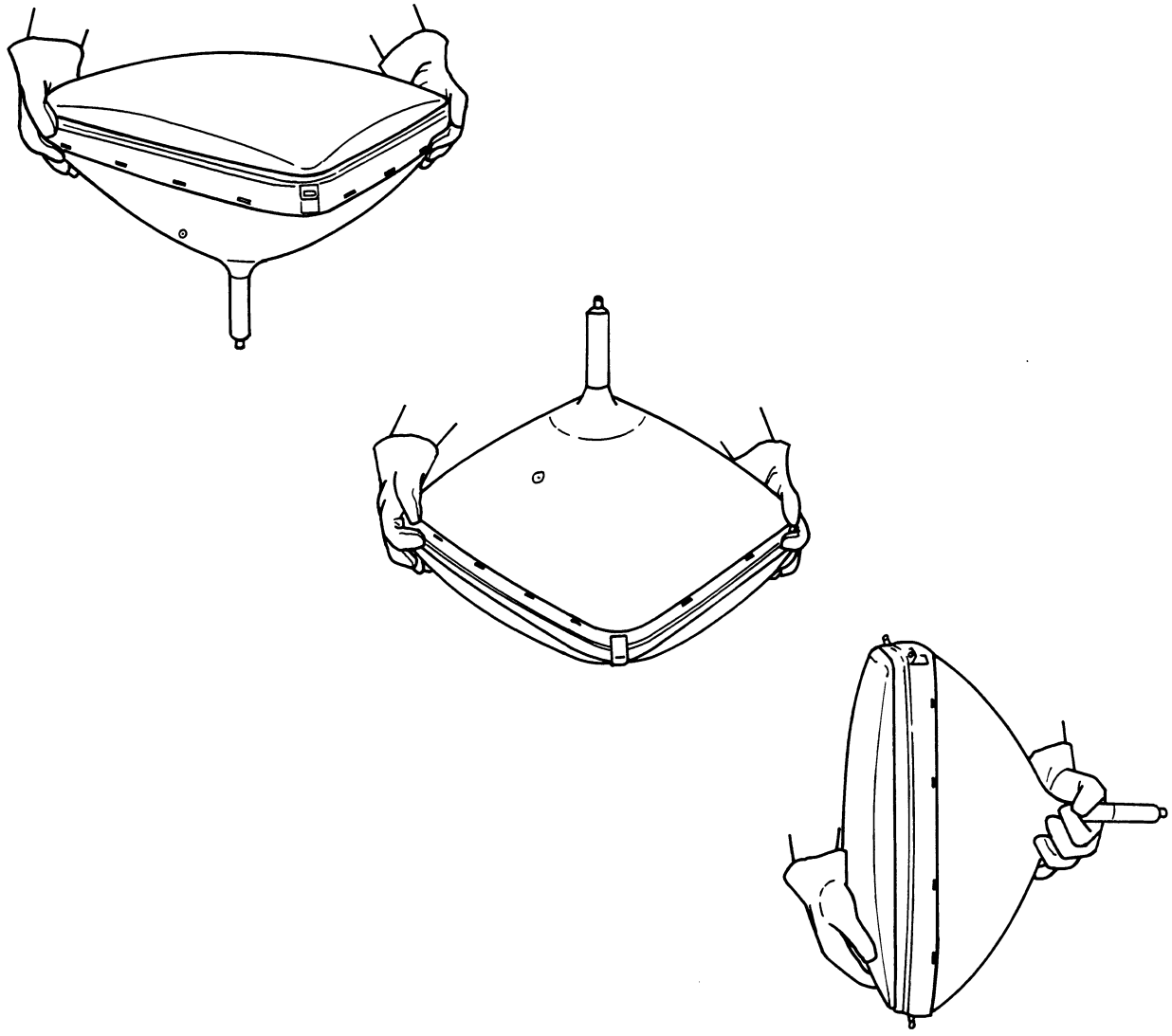


Fig. 4.3.13 - Handling the Tube

4.4 Adjustments

The following section gives instructions on how to perform adjustments on the RE201. Before adjustments are initiated, the RE201 must be allowed a warm-up period of at least one hour for all analog circuitry to stabilize. It is strongly recommended that an adjustment is only attempted in case of minor deviations from nominal performance. All major adjustments of the instrument or individual PCB boards should be done by the factory.

The dismantling of the instrument is described in section 4.3 and the recommended equipment for the adjustments is listed in section 4.1.

In section 6 component layouts for the individual prints show the locations of various test points and potentiometers used during the adjustment procedures described below.

An overview of the adjustment facilities provided on the individual boards and units in the RE201 is given in the following.

Linear Power Supply (901-406):

* +/- 15 V supply - R23

Switch Mode Power Supply (901-022):

* +5 V supply - R5
* +12 V supply - R24
* Current limiter for +5 V - R22

Analog Frontend (901-421):

* Input DC offset in right channel - R258
* Input DC offset in left channel - R257
* Amplification at 0 dB in right channel - R232
* CMRR at 0 dB in right channel - R231
* Amplification at 0 dB in left channel - R234
* CMRR at 0 dB in left channel - R233
* CMRR at -20 dB in left channel - R12
* CMRR at -20 dB in right channel - R11
* Gain in antialiasing filter - R83
* A/D converter offset - R206
* Sample/Hold offset - R193
* +Peak detector - R156
* -Peak detector - R157
* Overload detector - R208

Analog Motherboard (901-405), Phase Detector

* +5 V reference - R63
* Input DC offset in right channel, normal mode - R11
* Input DC offset in left channel, normal mode - R26
* Output offset - R53
* Output gain - R50
* Input DC offset in left channel, invert mode - R22

I/O & Memory Bus Interface (901-407) - DC inputs:

* DC1 D/A converter offset - R20
* DC1 D/A converter gain - R16
* DC2 D/A converter offset - R35
* DC2 D/A converter gain - R31

CRT Driver (901-417):

* Brightness white level - R6
* Horizontal frequency - R21
* Vertical frequency - R48
* Vertical amplitude - R4
* Dynamic picture centering - R31
* Vertical linearity - R37

Deflection Unit (CRT Section):

* Picture tilt - Deflection Unit position
* Static picture centering - centering rings
* Static linearity - linearity magnets

***** Note *****

During adjustments the operator will get access to areas which contain dangerous voltages (mains power and CRT deflection voltage (11 kV)). Thus, adjustments should be carried out by authorized personnel only.

Furthermore, note that extraction and insertion of PCB's while the RE201 is switched on may cause permanent damage to circuitry on the PCB itself and to other parts of the RE201.

4.4.1 Linear Power Supply (901-406)

The Linear Power Supply is located below the Mains Transformer and the I/O & Memory Bus Interface. Adjustment may be performed without removing any of these parts.

+/- 15 V Adjustment, R2

Adjust to +15.05 V +/- 0.05 V and -15.05 V +/- 0.05 V measured with

DVM at bus lines 5AB and 39AB on the Analog Motherboard (Ground on 4AB).

4.4.2 Switch Mode Power Supply (901-022)

The Switch Mode Power Supply is located in the Digital Section. Thus, to gain access, it is necessary to remove the digital shielding box covering the Digital Section (refer to section 4.3.3).

+5 V Adjustment, R5

Adjust to +5 V +/- 0.01 V measured with DVM at bus line 2AB on the Analog Motherboard (Ground on 1AB).

Check that the +5 V supply, measured at bus line 2AB on the Digital Motherboard does not exceed 5.10 V (Ground on 1AB).

+12 V Adjustment, R24

Adjust to +12 V +/- 0.05 V measured with DVM at TP6 on the Switch Mode Power Supply.

+5 V Current Limiter, R22

The current limiter should only be adjusted in case of replacement of components in the current limiter circuitry, and even in this case adjustment is only recommended, if the current limiter is active during normal operation.

If adjustment is required, the first step is to remove all the plug-in boards in the Digital and Analog Sections except the Switch Mode Power Supply.

Connect (preferably solder) a 10 amp load directly across C16 on the Switch Mode Power Supply (0.5 Ohm +/- 5 %, 50 W).

Connect an oscilloscope to QA2, pin 7 and adjust to constant high level (approx. 4 to 5 V) by means of R22.

4.4.3 Analog Frontend (901-421)

This section describes the following adjustment facilities on the Analog Frontend:

Input amplifiers:

Input DC offset	When the input offset adjustments have been performed the Phase Detector adjustments should be checked (refer to section 4.4.4)

Gain at 0 dB in RIGHT channel
CMRR at 0 dB in RIGHT channel
Gain at 0 dB in LEFT channel
CMRR at 0 dB in LEFT channel
CMRR at -20 dB in LEFT channel
CMRR at -20 dB in RIGHT channel

These six adjustments of the input amplifier should be performed in the stated order and all six should be performed

Antialiasing Filter:

Gain in antialiasing filter

A/D converter circuit:

A/D converter - zero adjustment

This adjustment should be followed by the Sample/hold zero adjustment

Sample/hold - zero adjustment

Detectors:

+ Peak Detector adjustment
- Peak Detector adjustment
Overload detector adjustment

The adjustment may be performed independently with the exceptions described above. All voltage measurements should be performed using a high precision (0.1 % or better) digital voltmeter.

For easier access the Analog Frontend should be mounted on Extender Board (901-611) (refer to section 4.3.1). Furthermore, before the adjustments are initiated, it is convenient to program the RE201 to the three LEVEL measurements outlined in table 4.7.

The location of potentiometers is shown in fig. 3.2.7.

	Channel	Mode	Duration	Representation
LEV1:	TBD	RMS25	256 ms	DBR
LEV2:	TBD	RMS25	256 ms	VOLT
LEV3:	RIGHT	PEAK	100 ms	VOLT

Table 4.7 - Measurements Used for Analog Frontend Adjustments

Input Amplifiers

Input DC Offset

Shortcircuit RIGHT channel and LEFT channel inputs on the front panel of the RE201 and execute the LEV2 measurement (RIGHT channel).

By means of R257 adjust DC voltage measured at Bus line 7A on the Extender Board to 0.0 mV +/- 0.01 mV (Ground to 4A).

By means of R258 adjust to 0.0 mV +/- 0.01 mV measured at Bus line 8A on the Extender Board (Ground to 4A).

As earlier mentioned, the following six adjustments must be carried out as one sequence.

Gain at 0 dB in RIGHT Channel

Test signal 1 kHz, 1.500 Vrms. Remove QA16 and short pin 5 in J2 to pin 6 in QA16 socket.

Remove the flat cable attached to J1.

R.CH+ = 0V (J1 pin 7)
R.CH- = signal (J1 pin 10)

Execute LEV2 measurement (RIGHT channel).

By means of R232 adjust the signal level at the S/H output, J1 pin 1 to be equal to the input level within +/- 0.5 %.

CMRR at 0 dB in RIGHT Channel

Press <STO REF>.

R.CH+ = signal
R.CH- = signal

(Short R.CH+ and R.CH- in J1 and connect ground on the generator to ground on the Analog Frontend J1 pin 8).

Execute LEV1 measurement (RIGHT channel). Adjust R231 to obtain minimum reading on the RE201 (<- 70 dB below 1.5 Vrms).

Gain at 0 dB in LEFT Channel

L.CH+ = 0V (J1 pin 4)
L.CH- = signal (J1 pin 13).

Execute LEV2 measurement (LEFT channel). By means of R234 adjust the

signal level at the S/H output (J1 pin 1) to be equal to the input level within +/- 0.5%.

CMRR at 0 dB in LEFT Channel

L.CH+ = signal
L.CH- = signal.

Execute LEV1 measurement (LEFT channel). Adjust R233 to obtain minimum reading on the RE201 (<- 70 dB below 1.5 Vrms).

CMRR at -20 dB in LEFT Channel

Test signal 1 kHz, 1.8 Vrms.

L.CH+ = 0V
L.CH- = signal.

Execute LEV2 measurement (LEFT channel).
Press <STO REF>.

L.CH+ = signal
L.CH- = signal.

Execute LEV1 measurement (LEFT channel). Adjust R12 to obtain minimum reading on the RE201 (<- 86 dB below 1.8 Vrms).

CMRR at -20 dB in RIGHT Channel

R.CH+ = signal
R.CH- = signal.

Execute LEV1 measurement (RIGHT channel). Adjust R11 to obtain minimum reading on the RE201 (<- 86 dB below 1.8 Vrms).

Remove the connection between J2 pin 5 and pin 6 in QA16 socket.
Mount QA16.

Gain in Antialiasing Filter

R.CH input signal 1 kHz, 1.500 Vrms.

Execute LEV1 measurement (RIGHT channel). By means of R83 adjust signal level at the S/H output (J1 pin 1) to be equal to the input level within +/- 0.5 %.

Digitizing Circuitry

A/D Converter - Zero Adjustment

Shortcircuit R.CH and L.CH inputs. Execute LEV2 measurement (RIGHT channel). Adjust DC voltage at P1 pin 3 to 0 mV +/- 0.3 mV using R193. Adjust to minimum reading on the RE201 using R206.

Sample/Hold - Zero Adjustment

Adjust to minimum reading on the RE201 using R193 (typical < 8 uV).
Adjust to 0 mV +/- 0.3 mV at the S/H output J1 pin 1 using R198.

Detectors

Peak Detector Adjustments

R.CH input signal 1 kHz, 1.00 Vrms.
Execute LEV3 measurement.
Adjust to obtain a + Peak reading of 1.41 V +/- 0.01 V using R156.
Adjust to obtain a - Peak reading of 1.41 V +/- 0.01 V using R157.

Overload Detector Adjustment

Connect pin 16 on relay K1 to ground.
R.CH input signal 1 kHz, 1.700 RMS.
Execute LEV2 measurement (RIGHT channel).

If the RE201 indicates "Input Overload", turn the potentiometer R208 counter clockwise until the overload information disappears. Then turn R208 clockwise very slowly until "Input Overload" reappears on the CRT.

4.4.4 Phase Detector - Analog Motherboard (901-405)

The adjustment of the Phase Detector is quite sensitive and it may be necessary to repeat the adjustment procedure two or three times before correct Phase measurements are obtained.

Except for adjustment of the +5 V reference voltage supply, all adjustments are carried out while monitoring the measurement results provided by a default Phase measurement executed by the RE201.

The locations of test points and potentiometers are shown in fig. 3.2.9.

+5 V Reference, R63

Adjust to +5 V +/- 0.01 V measured at TP2 (Ground on TP1 or TP3).

Offset - Normal Mode

R.CH and L.CH input signals 1 kHz, 20 mVrms.
Execute PHASE measurement.
Be sure that the label for softkey F7 is <INVERT> else press F7.

Adjust R11 to a reading as close to 0 deg. as possible, then adjust R26 to a reading as close to 0 deg. as possible.

It is very important that these two adjustments are performed carefully and with accuracy.

Adjust to 0 deg. by means of R53.

Gain Adjustment

Invert the input signal 180 deg. for R.CH by swapping the leads of the input cable connected to the R.CH input.

Adjust to 180 deg. by means of R50.

Offset - Invert Mode

R.CH and L.CH input signals 1 kHz, 20 mVrms (signals in phase).
Press <INVERT> softkey F7.

Adjust to 180 deg. by means of R22.

4.4.5 DC Inputs

The DC measuring circuits are comprised on the I/O & Memory Bus Interface board located below the Mains Transformer. The locations of test points and potentiometers are shown in fig. 3.2.15.

To make the following adjustments easier, it is convenient to remove the transformer without disconnecting it electrically (refer to section 4.3.2 for removal of the Mains Transformer).

DC1 Input

Input 0.00 V DC at DC1 input.
Execute DC1 measurement.
Adjust R20 and note the two positions of R20 at which the RE201 reading is 125 mV and -125 mV, respectively, and leave R20 in a position exactly in the middle.

Input +10.0 V DC at DC1 input.
Note the two positions of R16 where the RE201 reading is +10.1 V and 9.88 V, respectively, and leave R16 in a position exactly in the middle.

DC2 Input

The DC2 circuitry is adjusted as DC1. Instead of potentiometers R20 and R16, R35 and R31 should be used and the DC2 measurement is executed.

4.4.6 CRT Section

The adjustments of the CRT Section are, with four exceptions, performed inside the CRT shielding box on the CRT Driver and the Deflection Unit. Refer to section 4.3.4 for dismantling of the CRT Section.

The CRT Section includes the following nine adjustments:

* Brightness white level
* Horizontal frequency
* Vertical frequency
* Picture tilt
* Vertical amplitude
* Static picture centering
* Dynamic picture centering
* Vertical linearity
* Static linearity

Four adjustments may be performed through holes in the Base Plate. For these adjustments, only the bottom plate has to be removed. The four adjustments are:

* Brightness white level
* Vertical frequency
* Vertical linearity
* Vertical amplitude

Refer to fig. 4.3.11 to locate the adjustment holes and to fig. 3.4.2 to locate the potentiometers on the CRT Driver.

All adjustments are performed while the RE201 is turned on. The nine adjustments may be performed independently.

Brightness White Level

Press 'INT' and 'CURSOR UP' simultaneously until maximum brightness is obtained on the CRT.

Adjust to maximum brightness without flyback lines by means of R6 on the CRT Driver.

Press 'INT' and 'CURSOR DOWN' until normal brightness is obtained.

Horizontal Frequency

Turn R21 as far as possible counter-clockwise. Slowly turn R21 clockwise and note the range in which a stable picture is obtained. Leave R21 in a position approx. in the middle of this range.

Vertical Frequency

Adjust R48 in the same way as described for R21 during the adjustment of the 'horizontal frequency'.

Picture Tilt

Loosen the screw on the clip securing the Deflection Unit on the tube neck (refer to fig. 4.4.1).

Turn the Deflection Unit to a position where the dotted line at the bottom of the picture is parallel with the front frame edge. Tighten the screw securing the Deflection Unit.

Vertical Deflection

Adjust to correct vertical picture size using R4 (upper and lower CRT text lines approx. 1 cm from front frame edges).

Static Picture Centering

Adjust the two centering rings on the Deflection Unit to obtain correct centering of the picture (refer to fig. 4.4.1).

The adjustment is performed by turning only one centering ring at a time until the picture is placed in the middle of the CRT (one ring for horizontal centering and one for vertical).

Dynamic Picture Centering

This adjustment is used if only horizontal picture centering is necessary.

Adjust R31 to correct picture centering (same distance from dotted line on the CRT to both vertical edges on front frame).

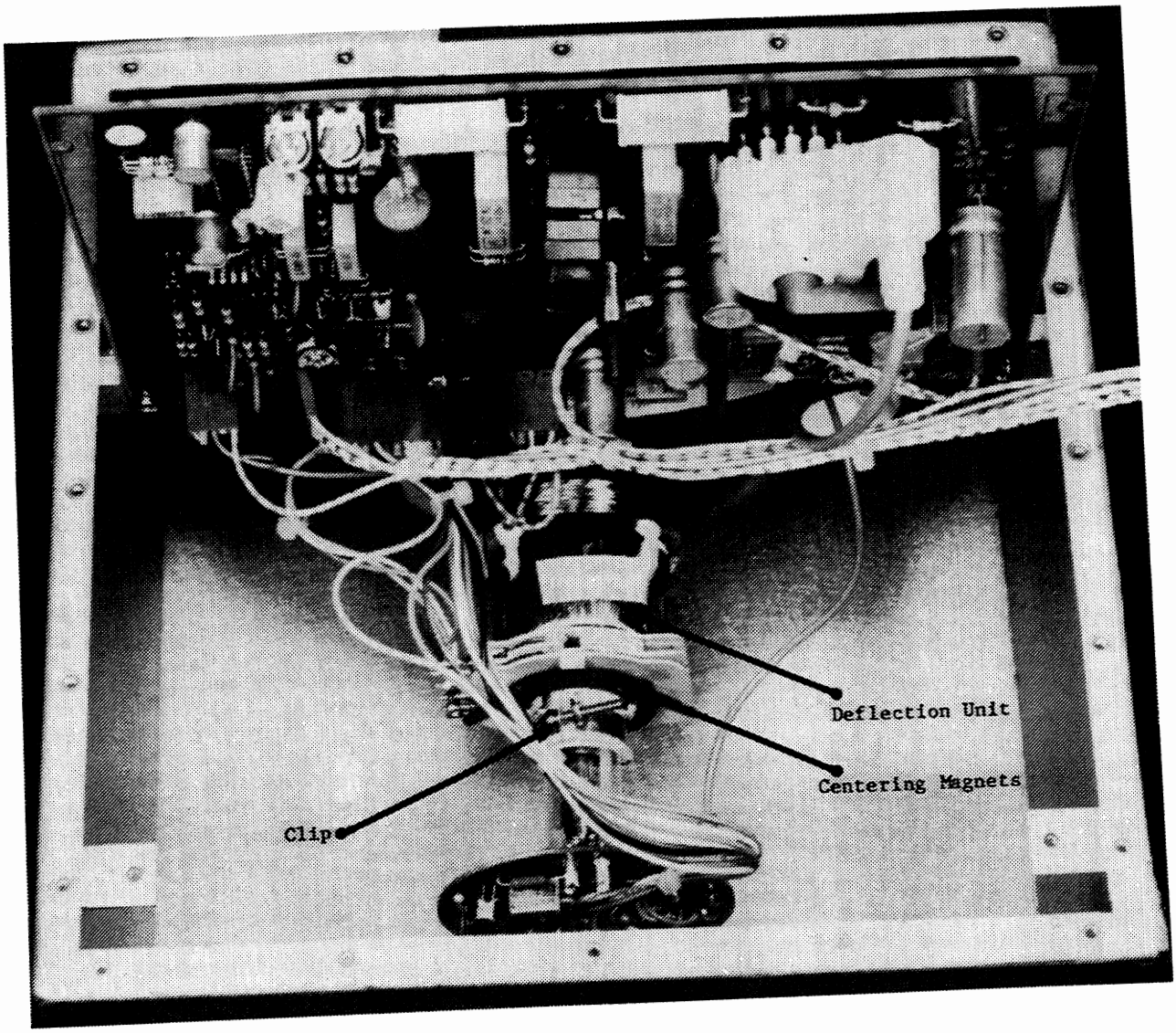


Fig. 4.4.1 - Interior CRT Section View

Static Linearity

The static linearity is adjusted by means of small magnets mounted on taps on the Deflection Unit.

Turn the magnets to obtain correct linearity in the corners of the picture. Use a picture with characters in the lower corners (e.g. LEARN LEV, mode RMS25, cursor pointing at REPRESENTATION).

Linearity in the upper corners may only be monitored and adjusted correctly, if an IEEE488 Bus controller is available.

Vertical Linearity

Adjust to equal character height in upper and lower character lines on the CRT by means of R37.

5 TROUBLESHOOTING

Although the RE201 system has been carefully designed for high reliability it is possible that faults may occur with time. Errors may originate from drifting or failing components or may be introduced via mechanical strains such as shock, vibration, or incorrect handling during mounting of options and associated cables.

In a complicated instrument as the RE201, there are possibilities for errors which may be difficult to track, as the errors may originate from many different parts of the system. Consequently, it requires an in-depth knowledge of and familiarity with the circuitry and the internal signal routing to perform a thorough troubleshooting to component level. Furthermore, special test equipment is in most cases a necessity in order to be able to establish special setups of the circuitry.

The following sections aim at providing troubleshooting information sufficient to perform diagnosis to board level. Then, it is usually uncomplicated to remove the PCB for service at the local RE INSTRUMENTS representative or the factory. Alternatively, the board may be substituted by a correctly functioning unit. The locations of the various boards are shown in fig. 3.2.1 for boards in the Analog Section, and in fig. 3.3.1 for boards in the Digital Section. Dismantling of the instrument is described in section 4.3.

Before commencement of troubleshooting, it is recommended that Section 2, Principles of Operation, and Section 3, Circuit Descriptions, is studied. Acquaintance with these sections is anticipated in the following.

The troubleshooting information is divided into two main parts:

* Detailed discussion of the selftest routines

* Discussion of errors which may be observed during operation of the RE201.

In case it is desired to localize the error on the board, please refer to the description of the individual PCB's in section 3 of this manual. For options, refer to the Technical Manuals for the respective options.

5.1 Power-up Errors

If the RE201 does not respond when the mains power switch is turned on, please check the mains supply, the power cables and the fuses (line fuse and DC fuse). If everything is found to work correctly,

the error most probably is found in the Switch Mode Power Supply, located in the Digital Section.

A schematic diagram of the mains input is found at the back of this manual (drawing No. 985-211).

5.2 Selftest Errors

When power is applied, or whenever a selftest has been instigated from the keyboard or via the IEEE488 Bus Interface, the RE201 performs a test of vital circuit parts. This test mainly comprises verification of the function of digital circuitry and communication links. The Analog Section is tested by the Static CPU, and the Digital Section by the Main CPU. As the Main CPU has direct access to the CRT, the result from the selftest in this section is displayed on the CRT. Further details are read out on a LED array, located on the Main CPU board. Contrary to the LED array in the Digital Section, which is not easily accessible due to the shielding box, the Analog Section array may be observed simply by removing the top plate. The information displayed on the CRT is in clear text, whereas the LED arrays display error codes, the interpretations of which are listed in tables 5.1 and 5.2 (for Analog and Digital Section, respectively).

It should be noted, that before a specific test is initiated, the corresponding error code is read out on the LED array. If the test is successfully completed, the array is cleared. Furthermore, note that the RE201 as soon as an error is encountered halts execution of the test in order to freeze the error condition and the error message.

5.2.1 Analog Section Selftest

Table 5.1 presents the interpretation of the error codes, which are displayed on the LED array of the Static CPU board. Details of the individual tests are given below.

The test and initialization, carried out by the Static CPU, goes off as follows:

a. DC inputs, phase detector and Memory Bus "out of range" are disabled. All options are deselected.

b. The RAM, QD36 on the Static CPU board is partly tested.

c. The UART used for serial communication with the Main CPU is tested (QD14 on the Static CPU board).

   *** Note ***

   General errors in the CRU interface will cause error at this point.

Error code	Circuitry/function tested
Basic Unit	
0110 0001	QD36, Static CPU (Part of Housekeeping RAM)
0000 0010	QD14, Static CPU (Interprocessor Communication UART)
0000 0100	No $\overline{SC}$ signal for A/D Converter
0000 0011	Discharge function on Analog Frontend, alternatively bad connection Analog Frontend/Static CPU
0001 0001	QD37, Static CPU (User definition RAM) Note 1
0010 0001	QD37, Static CPU (User definition RAM) Note 1
0011 0001	QD37, Static CPU (User definition RAM) Note 1
0100 0001	QD37, Static CPU (User definition RAM) Note 1
0101 0001	QD36, Static CPU (User definition RAM) Note 1
1000 0001	QD34, Static CPU (Program EPROM)
1000 0010	QD34, Static CPU (Program EPROM)
1000 0100	QD34, Static CPU (Program EPROM)
1000 1000	QD34, Static CPU (Program EPROM)
1001 0000	QD35, Static CPU (Program EPROM)
1010 0000	QD35, Static CPU (Program EPROM)
Options	
1100 0111	QD12, Weighting Filters (Program EPROM)
1100 0110	QD12, Filter Option (Program EPROM)
0001 0101	QD1, Audio Generator (Sine Table EPROM)
0010 0101	QD2, Audio Generator (Sine Table EPROM)
0011 0101	QD3, Audio Generator (Sine Table EPROM)
0100 0101	QD4, Audio Generator (Sine Table EPROM)
0101 0101	QD5, Audio Generator (Program EPROM)
0110 0101	QD6, Audio Generator (Multitone RAM)
0111 0101	QD7, Audio Generator (Multitone RAM)
System Crash	
0101 0101 1010 1010	Blinking sequence, indicating fault in the interface to either Weighting Filters, Filter Option or Audio Generator, if encountered during selftest

Note 1: This test is only performed, if the buttons "2nd" and "TEST" are depressed during power-up.

Table 5.1 - Analog Section error codes

d. The discharge facility of the Analog Frontend is activated, for the signal path as well as for the peak and overload detectors. After 500 ms, the Static CPU reads the output from the A/D converter. This may generate two different error messages:

   * $\overline{SC}$ signal missing (Start Conversion clock for the A/D).

   * Input signal to A/D converter too high, probably due to a malfunctioning discharge circuit.

e. If buttons "2nd" and "TEST" are depressed, the RAM's containing the user definitions on the Static CPU are tested in the order:

   QD37 and QD36.

f. The EPROM's on the Static CPU are tested in the order:

   QD34 and QD35.

   In this specific case, the test is not halted if an error is detected. Instead, the Static CPU keeps the information about the error until the options test and initialization procedure is completed (item i. below).

g. The Analog Frontend is initialized as follows:

   -20 dB gain setting in both channels
   RIGHT channel input selected
   25 kHz antialiasing filter inserted
   AC input to A/D converter selected

h. The presence of the various analog options is tested in the order:

   * Wow & Flutter
   * Weighting Filters
   * Filter Option
   * Audio Generator

   If an option is detected, it is initialized. For the last-mentioned three options, a selftest is performed using the on-board program memory. If the communication with the memory circuit or the memory itself do not function correctly, the Static CPU will "crash", i.e. the program execution is jeopardized. This situation is detectable by observing, that the diodes of the LED array are switched ON and OFF, four by four as outlined in table 5.1.

i. When the options have been initialized, the Static CPU will check for errors encountered during test of the EPROM's, on the CPU board as well as on option boards (item 'f' above). If any, the corresponding error code is displayed and the test execution is halted. At the same time, the red LED of the "2nd" button is blinking, indicating an EPROM error.

j. If the test is successfully completed, the Static CPU will switch the diodes in the buttons "2nd" and "LOCAL" ON and OFF by turns, while waiting for the Main CPU to finish the selftest of the Digital Section.

k. When the Main CPU has completed its selftest, it initiates the communication by pulling the handshake line of the Interprocessors Communication Link low (normal stand-by condition is high). Upon detection of this, the Static CPU responds by transmitting the ASCII character "ACK". Then, the Main CPU transfers the result of the selftest, including information of options installed in the Digital Section, to the Static CPU.

l. When the selftest result from the Digital Section is correctly received, the blinking of the LED's on the Front Panel is stopped, and the Static CPU transfers the result of the selftest in the Analog Section, including information of installed options and software revisions, to the Main CPU. The Main CPU then establishes the options and software revisions display.

m. If "2nd" and "TEST" are depressed the content of all setups and the SYSTEM and BASIC PARAMETERS are set to default values.

n. The Memory Bus is initialized:
   * Setup No. 0
   * REMOTE low
   * LOAD high

   The GPIO outputs assume HIGH/LOW states as defined in setup No. 0.

o. Finally, all user definitions are checked for possibly destroyed content. No parameter check is done, i.e. if an option has been dismounted, illegal parameters may be present. However, this is detected if execution of a function including such a parameter is attempted, but no error message is displayed.

A selftest activated from the keyboard or via the IEEE488 Bus will proceed in the same way, with the only exception being that the absence of the Start Conversion cannot be detected (as during 'd' above).

5.2.2 Digital Section Selftest

The test of the Digital Section verifies important circuit block, such as the Main CPU, the Arithmetical Unit and the ZOOM facility. Furthermore, the serial communication link to the Static CPU is checked. The error codes, which may be displayed on the LED array of the Main CPU board, are given in table 5.2. Details of the individual tests are given below.

Error code	Circuitry/function tested
Basic Unit	
0001 0000	Access to Arithmetical Unit
0000 1011	QD12, Main CPU (CRT Refresh RAM's)
0000 1100	QD 4, Main CPU (Program EPROM)
0000 1101	QD 5, Main CPU (Program EPROM)
0000 1001	QD 8, Main CPU (RAM)
0000 1110	QD14, CRT Controller
0000 1111	QD 3, Interrupt Controller
0000 1010	QD 2, IEEE Controller
0000 0001	QD41/QD42, Arithmetical Unit (EPROM tables)
0000 0011	QD37-QD40, Arithmetical Unit (Data samples RAM)
0000 0101	QD46-QD53, Arithmetical Unit (Multiplier registers)
0000 0111	QD46-QD61, QD67-QD72 Arithmetical Unit (Butterfly Unit)
0001 0101	QD4, Digital Motherboard (Interprocessor UART)
0001 0110	QD1, Digital Motherboard (RS232C UART)
0001 1000	ZOOM Facility
0001 1001	ZOOM Facility
0001 1010	ZOOM Facility
0001 1011	ZOOM Facility
0001 1100	ZOOM Facility
0001 1101	ZOOM Facility

Table 5.2 - Digital Section Error Codes

The test is executed in parallel with the test of the Analog Section. The test comprises the following steps:

a. The UART used for communication with the Static CPU (Digital Motherboard, QD4) is reset as the first act to ensure proper synchronization between the processors.

b. The Arithmetical Unit is initialized, and the Main CPU attempts to read the content of address location 4200H on the board. If the content read is FFFFH, an error code is issued. The fault may be caused by buffers on the CPU board or on the Arithmetical Unit board, by EPROM's or address decoding circuitry on the Arithmetical Unit, or by the connections in the Digital Motherboard.

c. The Interrupt Controller, QD3, on the Main CPU is initialized.

d. The CRT Refresh RAM's are filled with characters for blanking of the CRT.

e. The EPROM's on the Main CPU board are tested in the order:

QD4, and QD5.

f. The RAM memory on the Main CPU board is tested (QD8).

g. The EPROM's on the Arithmetical Unit are tested (QD41, QD42).

h. The RAM memory on the Arithmetical Unit is tested (QD37-QD40).

i. The registers for the multipliers on the Arithmetical Unit, used for the Butterfly Unit and the RMS Unit, are tested (QD46-QD53)

j. The operation of the Butterfly Unit is tested, including the operation of the overflow interrupt (QD46-QD61, QD67-QD72).

k. The UART used for Interprocessor Communication is tested (QD4 on the Digital Motherboard).

1. The UART used for the RS232C Interface is tested (QD1 on the Digital Motherboard).

m. The ZOOM board is tested.

n. Information of the selftest/options installed is exchanged with the Static CPU as described in the previous section.

5.3 Errors Observed During Operation

In this section is given a commented list of errors, which could be found during operation of the RE201. Together with each example is given a prioritized list of possible reasons for the error observed.

For an overview of the signal routing inside the RE201 and other aspects of measurement setups, please refer to sections 2.4 and 2.5 of the present manual.

If one of the three coaxial cables to the Analog Frontend are not connected properly, the following will be observed:

W1: Sample/Hold - the RE201 does not measure at all

W2: Start Conversion Clock - RE201 inactive when a measurement is started

W3: A/D Data Clock - level measurements yield constant results

Error	Indicated by	Possible reasons
Continuous autoranging	No results appear when a measurement is started. Rightmost LED in the array on the Static CPU board blinking	1. Spurious or low-frequency components in the input signal 2. The connection between Analog Frontend and Static CPU 3. Analog Frontend (gain sections, signal routing) 4. Static CPU
RE201 halts operation at arbitrary intervals - no response to keyboard inputs	Static CPU displays a "crash" code on the LED array (refer to table 5.1)	1. Static CPU (clock restart circuitry)
INPUT TOO LOW regardless of input signal	Text on CRT	1. Analog Frontend (discharge malfunction, FFT switches, missing plug in J2) 2. Cables to/from Interconnection board (Note 1) 3. Data transfer to Digital Section (cable to pi-filters, serial/parallel conversion register on Digital Motherboard, cable to Arithmetical Unit)
RMS75, Quasipeak, Peak, Phase and W&F detector not working, except for one	Measurement readings	1. FET switch connecting one of the detectors to the DETECTOR OUT bus is malfunctioning
FREQUENCY OUT OF RANGE combined with constant level measurement results	Text on CRT and measurement readings	1. Coaxial cable W3 to Analog Frontend disconnected 2. Data transfer to Digital Section (as above)
All level measurements incorrect	Measurement readings	1. Analog Frontend (gain sections, signal switching)
RMS25 incorrect, other level measurements correct	Measurement reading	1. RMS Unit on Arithmetical Unit
RMS75 incorrect, other level measurements correct	Measurement reading	1. RMS Detector on Filter Option board
Peak incorrect, other level measurements correct	Measurement reading	1. Peak Detector on Analog Frontend (typically only +Peak or -Peak)
Quasipeak incorrect, other level measurements correct	Measurement reading	1. Quasipeak detector on Weighting Filters board
DC measurement incorrect	Measurement reading	1. I/O & Memory Bus Interface 2. Cable from I/O & Memory Bus Interface to Analog Motherboard
THD incorrect, Filter Option not used (Note 2)	Measurement reading	1. Analog Frontend (excess distortion) 2. Arithmetical Unit
THD incorrect, Filter Option included (Note 2)	Measurement reading	1. Filter Option 2. Analog Frontend (excess distortion) 3. Arithmetical Unit
SINAD incorrect	Measurement reading	1. Filter Option (notch filters, RMS detector) 2. Analog Frontend (excess distortion)
Weighted measurements	Measurement reading	1. Weighting Filters (actual filter, if only one incorrect, otherwise gain sections or FET switches) 2. Cables connecting Weighting Filters to Analog Frontend
Wow & Flutter	Measurement reading	1. Wow & Flutter board
Phase	Measurement reading	1. Phase Detector 2. Excessive noise level
RS232C Interface	Data not transmitted or received	1. SYSTEM parameters not defined correctly; jumper K2 on Digital Motherboard not positioned correctly 2. RS232C UART on Digital Motherboard (QD1) 3. Cables and pi-filters
GPIO	Incorrect signals on GPIO outputs	1. I/O & Memory Bus Interface 2. Connection to Analog Motherboard 3. Cable to Rear Panel
Memory Bus	Incorrect handling of attached generators	1. I/O Memory Bus Interface 2. Connection to Analog Motherboard 3. Cable to Rear Panel or Memory Bus cables
IEEE488 Bus Interface	Data not received or transmitted	Refer to IEEE488 Bus Interface option Technical Manual
Internal Keyboard	Incorrect or no operation	1. Keyboard PCB 2. Connection to Analog Motherboard 3. Buffers on Analog Motherboard
RE905 Keyboard	Incorrect or no operation	1. Flexible cord (presumably at the connector) 2. RE905 3. Buffers on Analog Motherboard
CRT displays arbitrary characters	CRT	1. CRT controller on Main CPU board
CRT blanked	CRT	1. +12V power supply (from Switch Mode Power Supply) 2. Connections from Digital Section to CRT Section 3. CRT Driver board
CRT very bright (Note 3)	CRT	1. CRT Driver board
Narrow stripe	CRT	1. Vertical deflection circuitry

Note 1: When mounting flat cables, it is important to assure, that one or more of the pins of the connectors are not bent.

Note 2: The Filter Option Technical Manual provides information of the conditions for which the Filter Option is used.

Note 3: Remember the brightness control ('INT' and 'CURSOR UP', 'CURSOR DOWN' respectively).

Table 5.3 - Errors during Operation

6 PARTS LISTS AND SCHEMATIC DIAGRAMS

6.1 Parts Lists

All electronic components are included in the parts lists. Parts marked with an * are manufactured by RE INSTRUMENTS AS.

When ordering spare parts it is important that you give the following information:

* Code No. and description of the part.
* Circuit reference from the schematic diagram.
* Complete type designation of RE product.

Main Parts List

Assembled Units	Code No.	Page
* Switch Mode Power Supply	901-022	2
* Analog Motherboard	901-405	5
* Linear Power Supply	901-406	10
* I/O & Memory Bus Interface	901-407	13
* Keyboard	901-410	16
* Tube Unit	901-414	19
* CRT Driver	901-417	21
* Analog Frontend	901-421	26
* Arithmetical Unit	901-527	38
* Static CPU	901-788	42
* Main CPU	901-789	46
* Digital Motherboard	901-790	50
* Mains Input and Power Supply Filters	985-211	53
* PI-Filters	985-217	54

The parts lists as well as the schematic diagrams are arranged according to code No.

Switch Mode Power Supply (901-022)

CAPACITORS

C 1	Electrolytic 2200/40, 2000h/85°, A:18*40, RM18	260-053
C 2	C Ceramic 330p 2% 100V N750	213-214
C 3	C Polyst 10n0 1% 63V	243-302
C 4	C Solid alu 4u7 20% 25V	265-000
C 5	C Tantalum 47u 20% 6,3V	267-012
C 6	C Polystyrene 6n34 1% 63V	243-314
C 7	C Ceramic 100n 20% 50V	213-400
C 9	Electrolytic 2000/16, 2000h/85°, A:12.5*30, RM14	260-063
C 10	C Ceramic 100n 20% 50V	213-400
C 11	Electrolytic 220/25, 2000h/85°, A:10*18, RM10	260-042
C 12	C Ceramic 100n 20% 50V	213-400
C 13	Electrolytic 220/25, 2000h/85°, A:10*18, RM10	260-042
C 14	C Ceramic 100n 20% 50V	213-400
C 15	C Tantalum 22u 20% 16V	267-019
C 16	Electrolytic 2000/16, 2000h/85°, A:12.5*30, RM14	260-063
C 17	C Ceramic 470p 20% 100V	213-014
C 19	C Ceramic 100n 20% 50V	213-400
C 20	MKT, 0.22/100/10, R:4*9*13, RM4	241-032
C 21	C Ceramic 100n 20% 50V	213-400
C 22	C Ceramic 100n 20% 50V	213-400
C 23	C Solid alu 4u7 20% 25V	265-000
C 24	C Ceramic 10n0 -20+80% 63V	213-020
C 25	Electrolytic 2200/40, 2000h/85°, A:18*40, RM18	260-053
C 26	C Ceramic 100n 20% 50V	213-400
C 27	C Tantal 68u 20% 16V	267-015
C 28	C Ceramic 100n 20% 50V	213-400
C 29	C Polyst 2n00 1% 63V	243-305
C 30	C Ceramic 220p 2% 100V N750	213-129
C 31	C Tantalum 22u 20% 16V	267-019
C 32	C Polystyrene 6n34 1% 63V	243-314
C 34	C Ceramic 100p 2% 100V NP0	213-211
C 35	C Ceramic 100n 20% 50V	213-400
C 36	C solid AL 10u 20% 16V	265-008
C 37	Electrolytic 100/25, 2000h/85°, R:6.3*11, RM2	261-073
C 38	MKT, 0.033/400/10, R:4*10*13,RM4	241-021

DIODES

CR 1	Thyristor 2N4441	345-001
CR 2	Diode Zener C20 0.4W DO-35	350-650
CR 3	Diode MSP145 Schottky 1A	350-439
CR 5	Diode 10TQ45 S 45V 10A TO-220 AC Schottky	350-436
CR 6	Diode BYV27-200V 2A SOT-57 Fast Recovery	350-437
CR 7	Diode BYV27-200V 2A SOT-57 Fast Recovery	350-437
CR 8	Diode BAV20 Si Vr-150V If-250mA	350-023
CR 9	Diode zener BZX79-C7V5 0.4W	350-621
CR 10	LED 3mm red	350-043
CR 11	Diode BAV21 SI 200V 250mA DO-35	350-064
CR 12	Diode 80SQ045 S 45V 8A Power Schottky	350-434
CR 13	LED 3mm green	350-060

CR 14	Diode Zener C15-0.4W DO-35	350-611
CR 15	Diode Zener C56-1.3W	350-608

RELAYS & JUMPERS

K 1	Reed Relay 5V 360E	570-053

CHOKES

L 1	Coil 46uH	740-165
L 2	Coil 13uH	740-166
L 3	Coil 246uH	740-167

TRANSISTORS

Q 1	Transistor 2N5039 SI NPN 75V 20A 140W TO-3	360-164
Q 2	Transistor BD132 SI PNP 45V 3A 15W TO-126	360-163
Q 3	Transistor BC547B npn	360-159
Q 4	Transistor 2N5039 SI NPN 75V 20A 140W TO-3	360-164
Q 5	Transistor BD132 SI PNP 45V 3A 15W TO-126	360-163
Q 6	Transistor BD139 npn	360-137

INTEGRATED ANALOG CIRCUITS

QA 1	IC SG3524 switch reg.	364-442
QA 2	IC LM311N comparator	364-024
QA 3	IC SG3524 switch reg.	364-442

INTEGRATED DIGITAL CIRCUITS

QD 1	IC 74LS221 dual monostab	364-272

RESISTORS

R 1	R Carbon Film 1K 5% 0.2W	106-410
R 2	R Metal Film 4K99 1% 0.5W TC50	114-499
R 3	R Carbon 47K 5% 0.2w	106-547
R 4	R Carbon Film 39K 5% 0.2W	106-539
R 5	R.var 2K2 20% 0.5w	182-031
R 6	R Metal Film 4K42 1% 0.5W TC50	114-442
R 7	R Carbon Film 6K8 5% 0.2W	106-468
R 8	R Carbon Film 470E 5% 0.2W	106-347
R 9	R Carbon Film 56E 5% 0.2W	106-256
R 10	R Carbon Film 10E 5% 0,2W	106-210
R 12	R Low Ohmic LE005 3% 3W	173-000
R 13	R Metal Film 49K9 1% 0.5W TC50	115-499
R 14	R Metal Film 49K9 1% 0.5W TC50	115-499
R 15	R Carbon Film 33K 5% 0.2W	106-533
R 16	R Carbon Film 33K 5% 0.2W	106-533
R 17	R Carbon Film 680E 5% 0.2W	106-368
R 21	R Metal Film 3K40 1% 0.5W TC50	114-340
R 22	R Cermet Trimpot 200E 10% W Panel Mounting	182-404
R 23	R Metal Film 1K00 1% 0.5W TC50	114-100
R 24	R var 1K0 20% 0.5W	182-030

R 25	R Metal Film 4K53 1% 0.5W TC50	114-453
R 26	R Metal Film 4K99 1% 0.5W TC50	114-499
R 27	R Carbon 47K 5% 0.2w	106-547
R 28	R Carbon Film 33K 5% 0.2W	106-533
R 29	R Carbon Film 680E 5% 0.2W	106-368
R 30	R Carbon Film 39E 5% 0.2W	106-239
R 31	R Carbon Film 10E 5% 0,2W	106-210
R 32	R Wire Wound 0.1E 10% 2.5W	130-511
R 33	R Metal Film 13K3 1% 0.5W TC50	115-133
R 34	R Metal Film 3K50 1% 0.5W TC50	114-350
R 35	R Carbon Film 1K5 5% 0.2W	106-415
R 36	R Carbon Film 1K 5% 0.2W	106-410
R 37	R Metal Film 13K3 1% 0.5W TC50	115-133
R 38	R Carbon Film 1K 5% 0.2W	106-410
R 39	R Metal Film 3K57 1% 0.5W TC50	114-357
R 40	R Carbon Film 6K8 5% 0.2W	106-468
R 41	R Carbon Film 6K8 5% 0.2W	106-468
R 42	R Metal Film 3K40 1% 0.5W TC50	114-340
R 43	R Metal Film 1K00 1% 0.5W TC50	114-100
R 44	R Carbon Film 10E 5% 0,2W	106-210
R 45	R Carbon Film 100K 5% 0.2W	106-610
R 46	R Carbon Film 100E 5% 0.2W	106-310

MISCELLANEOUS

Screw pozidriv panhead M3x6	008-306
Screw Pozidrive Pan Head M3,5X10	008-310
Screw pozidriv panhead M3*12	008-312
Nut hexagon M3	031-302
Washer 3mm	042-315
Lock washer D3,2/5,5x0,45	046-405
tubular rivet 02.5x0.25x7	060-270
Soldering lug 3,2x12	061-132
Solder Terminal	062-107
Wire Wrap Terminal	805-727
Mounting Set for TO-3 Case	816-102
16 Pin Dil Socket	816-133
Mounting Acc. for TO-220	816-163
Rectangular Washer F. TO220	816-178
Insulation Bushing F. TO-220	816-214
Heat Sink SK48 50mm	816-249
Heat Sink SK48 100mm	816-253
Heat Sink Insulator for SK48 50mm	816-256
Heat Sink Insulator for SK48 50mm	816-257
Heat Sink	816-269
Silicon Washer for TO-3	816-270
Solder Terminal 0.1 O2	823-303
TY-Wrap 150X3.6mm	832-200
Attachment for TY-Wrap	832-204
Board Extractor	857-017
Conducter Rail C1	931-036
PCB for SMPS	970-921

Analog Motherboard (901-405)

CAPACITORS

C 1	C Ceramic 100n 20% 50V	213-400
C 2	C Ceramic 100n 20% 50V	213-400
C 3	C Ceramic 100n 20% 50V	213-400
C 4	C Ceramic 100n 20% 50V	213-400
C 5	C Ceramic 100n 20% 50V	213-400
C 6	C Ceramic 100n 20% 50V	213-400
C 7	C Tantalum 22u 20% 16V	267-019
C 8	C Ceramic 100n 20% 50V	213-400
C 9	C Ceramic 100n 20% 50V	213-400
C 10	C Ceramic 100n 20% 50V	213-400
C 11	C Ceramic 100n 20% 50V	213-400
C 12	MKT, 0.15/100/10, R:4*9.5*13, RM4	241-060
C 13	C Ceramic 100n 20% 50V	213-400
C 14	MKT, 0.22/100/10, R:4*9*13, RM4	241-032
C 15	C Ceramic 10n0 -20+80% 63V	213-020
C 16	C Ceramic 100p 2% 100V NP0	213-211
C 17	C Ceramic 33p0 2% 100V NP0	213-208
C 18	C Ceramic 100n 20% 50V	213-400
C 19	C Ceramic 100n 20% 50V	213-400
C 20	C Ceramic 100n 20% 50V	213-400
C 21	C Ceramic 100n 20% 50V	213-400
C 22	C Ceramic 100n 20% 50V	213-400
C 23	C Ceramic 100n 20% 50V	213-400
C 24	C Ceramic 100n 20% 50V	213-400
C 25	C Ceramic 100n 20% 50V	213-400
C 26	C electrolytic 10u0 25V	261-081
C 27	C electrolytic 10u0 25V	261-081
C 28	C electrolytic 10u0 25V	261-081
C 29	C electrolytic 10u0 25V	261-081
C 30	C electrolytic 10u0 25V	261-081
C 31	C electrolytic 10u0 25V	261-081
C 32	C electrolytic 10u0 25V	261-081
C 33	C electrolytic 10u0 25V	261-081
C 34	C electrolytic 10u0 25V	261-081
C 35	C electrolytic 10u0 25V	261-081
C 36	C Ceramic 100n 20% 50V	213-400
C 37	C Ceramic 100n 20% 50V	213-400
C 38	C Ceramic 100n 20% 50V	213-400
C 39	C Ceramic 100n 20% 50V	213-400
C 40	C Ceramic 100n 20% 50V	213-400
C 41	C Ceramic 4n70 -20+80% 63V	213-010
C 42	C Ceramic 8p20 p25 100V NP0	213-224
C 43	C Ceramic 8p20 p25 100V NP0	213-224

DIODES

CR 1	Diode zener 1N825 C6V2 0.4W	350-637

CONNECTORS

J 1	Bus Connector	805-790
J 2	Bus Connector	805-790
J 3	Bus Connector	805-790
J 4	Bus Connector	805-790
J 5	Bus Connector	805-790
J 6	Bus Connector	805-790
J 7	Terminal strip 7-pol Mod.II W.lock	805-897
J 9	16 Pin Dil Socket	816-133
J 10	12 pin SIL Connector	805-794
J 11	16 Pin Dil Socket	816-133
J 12	Conn Flat Plug F/PCB	804-613
J 13	16 Pin Dil Socket	816-133

TRANSISTORS

Q 1	Transistor BC557B pnp	360-160
Q 2	Transistor BC547B npn	360-159
Q 3	Transistor J109-18 n Fet	360-188
Q 4	Transistor J109-18 n Fet	360-188
Q 5	Transistor J109-18 n Fet	360-188
Q 6	Transistor BC547B npn	360-159
Q 7	Transistor BC547B npn	360-159
Q 8	Transistor BC547B npn	360-159
Q 9	Transistor BC557B pnp	360-160
Q 10	Transistor J109-18 n Fet	360-188
Q 11	Transistor J109-18 n Fet	360-188
Q 12	Transistor BC547B npn	360-159
Q 13	Transistor BC547B npn	360-159
Q 14	Transistor BC547B npn	360-159
Q 15	Transistor BC557B pnp	360-160

INTEGRATED ANALOG CIRCUITS

QA 1	IC TL084 quad op amp	364-276
QA 2	IC LM311N comparator	364-024
QA 3	IC LM311N comparator	364-024
QA 4	IC TL084 quad op amp	364-276

INTEGRATED DIGITAL CIRCUITS

QD 1	IC 74LS74 dual D ff	364-185
QD 2	IC 4049 hex inv buffer	364-224
QD 3	IC SN74LS367N HEX buffer/driver 3-state	364-400
QD 4	IC SN74LS367N HEX buffer/driver 3-state	364-400

RESISTORS

R 1	R Metal film 10K0 5% 0.2W TC250	107-510
R 2	R Metal film 56K0 5% 0.2W TC250	107-556
R 3	R Metal film 33K0 5% 0.2W TC250	107-533
R 4	R Metal Film 4K99 1% 0.5W TC50	114-499
R 5	R Metal Film 20K0 1% 0.5W TC50	115-200
R 6	R Cermet Trimpot 220K 10% 0.1W TC70	182-308
R 7	R Carbon Film 2M2 5% 0.2W	106-722
R 8	R thick film Sil 8x47K	146-005
R 9	R Metal film 3K30 5% 0.2W TC250	107-433
R 10	R Metal film 33K0 5% 0.2W TC250	107-533
R 11	R Cermet Trimpot 220K 10% 0.1W TC70	182-308
R 12	R Carbon Film 2M2 5% 0.2W	106-722
R 13	R Metal Film 5K76 1% 0.5W TC50	114-576
R 14	R Metal Film 16K9 1% 0.5W TC50	115-169
R 15	R Metal film 33K0 5% 0.2W TC250	107-533
R 16	R Metal film 100K 5% 0.2W TC250	107-610
R 17	R Metal film 10K0 5% 0.2W TC250	107-510
R 18	R Metal film 100K 5% 0.2W TC250	107-610
R 19	R Metal film 33K0 5% 0.2W TC250	107-533
R 20	R Metal Film 20K0 1% 0.5W TC50	115-200
R 21	R Metal Film 4K99 1% 0.5W TC50	114-499
R 22	R Cermet Trimpot 220K 10% 0.1W TC70	182-308
R 23	R Carbon Film 2M2 5% 0.2W	106-722
R 24	R Metal film 3K30 5% 0.2W TC250	107-433
R 25	R Metal film 33K0 5% 0.2W TC250	107-533
R 26	R Cermet Trimpot 220K 10% 0.1W TC70	182-308
R 27	R Carbon Film 2M2 5% 0.2W	106-722
R 28	R Metal Film 5K76 1% 0.5W TC50	114-576
R 29	R Metal Film 16K9 1% 0.5W TC50	115-169
R 30	R Metal film 33K0 5% 0.2W TC250	107-533
R 31	R Metal film 100K 5% 0.2W TC250	107-610
R 32	R Metal film 10K0 5% 0.2W TC250	107-510
R 33	R Metal film 100K 5% 0.2W TC250	107-610
R 34	R Metal film 33K0 5% 0.2W TC250	107-533
R 35	R Metal film 100E 5% 0.2W TC250	107-310
R 36	R Metal film 22K0 5% 0.2W TC250	107-522
R 37	R Metal film 100E 5% 0.2W TC250	107-310
R 38	R Metal film 68K0 5% 0.2W TC250	107-568
R 39	R Metal film 100E 5% 0.2W TC250	107-310
R 40	R Metal film 1K00 5% 0.2W TC250	107-410
R 41	R Metal film 100E 5% 0.2W TC250	107-310
R 42	R Metal film 1K00 5% 0.2W TC250	107-410
R 43	R Metal film 100E 5% 0.2W TC250	107-310
R 44	R Metal film 22K0 5% 0.2W TC250	107-522
R 45	R Metal film 100E 5% 0.2W TC250	107-310
R 46	R Metal film 68K0 5% 0.2W TC250	107-568
R 47	R Metal film 2K20 5% 0.2W TC250	107-422
R 48	R Metal Film 23K7 1% 0.5W TC50	115-237
R 49	R Metal Film 10K0 1% 0.5W TC50	115-100
R 50	R Cermet Trimpot 1K 10% 0.5W TC70	182-310
R 51	R Metal Film 115K 1% 0.5W TC50	116-115
R 52	R Metal Film 115K 1% 0.5W TC50	116-115

R 53	R Cermet Trimpot 220K 10% 0.1W TC70	182-308
R 54	R Metal film 1M00 5% 0.2W TC250	107-710
R 55	R Metal film 2K70 5% 0.2W TC250	107-427
R 56	R Metal Film 115K 1% 0.5W TC50	116-115
R 57	R Metal film 100E 5% 0.2W TC250	107-310
R 58	R Metal film 1K00 5% 0.2W TC250	107-410
R 59	R Metal film 1K00 5% 0.2W TC250	107-410
R 60	R Metal film 100E 5% 0.2W TC250	107-310
R 61	R Metal Film 1K10 1% 0.5W TC50	114-110
R 62	R Metal film 1K00 5% 0.2W TC250	107-410
R 63	R Cermet Trimpot 1K 10% 0.5W TC70	182-310
R 64	R Metal film 5K60 5% 0.2W TC250	107-456
R 65	R thick film Sil 8x10K	146-003
R 66	R thick film Sil 8x10K	146-003
R 67	R thick film Sil 8x10K	146-003
R 68	R thick film Sil 8x10K	146-003
R 69	R thick film Sil 8x10K	146-003
R 70	R thick film Sil 8x10K	146-003
R 71	R thick film Sil 8x10K	146-003
R 72	R thick film Sil 8x10K	146-003

TESTPOINTS

TP 1	Wire Wrap Terminal	805-727
TP 2	Wire Wrap Terminal	805-727
TP 3	Wire Wrap Terminal	805-727
TP 4	Wire Wrap Terminal	805-727
TP 5	Wire Wrap Terminal	805-727
TP 6	Wire Wrap Terminal	805-727
TP 7	Wire Wrap Terminal	805-727
TP 9	Wire Wrap Terminal	805-727
TP 10	Wire Wrap Terminal	805-727
TP 11	Wire Wrap Terminal	805-727
TP 12	Wire Wrap Terminal	805-727

MISCELLANEOUS

Screw pozidriv panhead M2x8	008-108
Nut hexagon M2	031-200
Spacing Nipple 03,5/8-1,5	065-675
Analog Motherboard PCB	971-152

Linear Power Supply (901-406)

CAPACITORS

C 1	Electrolytic 2200/40, 2000h/85°, A:18*40, RM18	260-053
C 2	Electrolytic 2200/40, 2000h/85°, A:18*40, RM18	260-053
C 3	Electrolytic 1000/63,	260-057
C 4	Electrolytic 1000/63,	260-057
C 5	Electrolytic 220/25, 2000h/85°, A:10*18, RM10	260-042
C 6	Electrolytic 220/25, 2000h/85°, A:10*18, RM10	260-042
C 7	Electrolytic 220/25, 2000h/85°, A:10*18, RM10	260-042
C 8	Electrolytic 220/25, 2000h/85°, A:10*18, RM10	260-042
C 9	C solid AL 6u8 20% 25V	265-003
C 10	C solid AL 6u8 20% 25V	265-003
C 11	MKT, 0.1/100/10, R:4*9*13, RM4	241-025
C 12	MKT, 0.1/100/10, R:4*9*13, RM4	241-025
C 13	MKT, 0.1/100/10, R:4*9*13, RM4	241-025
C 14	MKT, 0.1/100/10, R:4*9*13, RM4	241-025
C 18	C Ceramic 10n0 -20+80% 63V	213-020
C 19	C Ceramic 33p0 2% 100V NP0	213-208
C 20	C Ceramic 33p0 2% 100V NP0	213-208
C 21	C Ceramic 10n0 -20+80% 63V	213-020

DIODES

CR 1	Bridges Rectifier Vin:140 Io:6A	340-212
CR 2	Bridge Rectifier Vin:280V Io:25A	340-211
CR 3	Diode Zener C20 0.4W DO-35	350-650
CR 4	Diode Zener C20 0.4W DO-35	350-650
CR 7	Diode BAV20 Si Vr-150V If-250mA	350-023
CR 8	Diode BAV20 Si Vr-150V If-250mA	350-023
CR 9	Diode BAV20 Si Vr-150V If-250mA	350-023
CR 10	Diode zener 1N825 C6V2 0.4W	350-637
CR 11	Diode zener BZX79-C13V 0.4W	350-634
CR 12	Diode zener BZX79-C13V 0.4W	350-634
CR 13	Diode BAV20 Si Vr-150V If-250mA	350-023
CR 14	Diode BAV20 Si Vr-150V If-250mA	350-023
CR 15	Diode BAV20 Si Vr-150V If-250mA	350-023

CONNECTORS

J 1	8 Pin AMP mod. I Terminal List, Straight	806-001
J 2	12 Pin SIL Connector	805-793
J 3	4 Pin AMP mod. I Terminal List, Angled	805-915

TRANSISTORS

Q 1	Transistor BD132 SI PNP 45V 3A 15W TO-126	360-163
Q 2	Transistors BDT64 Darlington 60V PNP TO220	360-270
Q 3	Transistor BC557B pnp	360-160
Q 4	Transistor BC547B npn	360-159
Q 5	Transistor BC557B pnp	360-160
Q 6	Transistor BC547B npn	360-159
Q 7	Transistors BDT65 Darlington 60V NPN TO220	360-271

Q 8	Transistor BD139 npn	360-137

INTEGRATED ANALOG CIRCUITS

QA 3	IC LM301AH OP-AMP	364-016
QA 4	IC LM301AH OP-AMP	364-016

RESISTORS

R 2	R var 10K 20% 0.5w	182-008
R 3	R Carbon Film 22E 5% 0.2W	106-222
R 4	R Carbon Film 680E 5% 0.2W	106-368
R 5	R Carbon Film 22E 5% 0.2W	106-222
R 6	R Carbon Film 680E 5% 0.2W	106-368
R 11	R ww 0E68 10% 5w TC140	130-515
R 12	R Metal film 22E0 5% 0.2W TC250	107-222
R 13	R Metal film 270E 5% 0.2W TC250	107-327
R 14	R Metal film 1K80 5% 0.2W TC250	107-418
R 15	R Carbon Film 470E 5% 0.2W	106-347
R 16	R Metal film 10K0 5% 0.2W TC250	107-510
R 17	R Metal film 6K80 5% 0.2W TC250	107-468
R 18	R Carbon Film 470E 5% 0.2W	106-347
R 19	R Metal film 4K70 5% 0.2W TC250	107-447
R 20	R Metal Film 750E 0.5% 1/8W TC50	140-765
R 21	R Metal Film 4K99 1% 0.5W TC50	114-499
R 22	R Metal Film 3K48 1% 0.5W TC50	114-348
R 23	R Metal film 39K0 5% 0.2W TC250	107-539
R 24	R Carbon Film 470E 5% 0.2W	106-347
R 25	R Metal film 1K80 5% 0.2W TC250	107-418
R 26	R Carbon Film 470E 5% 0.2W	106-347
R 27	R Metal film 270E 5% 0.2W TC250	107-327
R 28	R Metal film 22E0 5% 0.2W TC250	107-222
R 29	R ww 0E68 10% 5w TC140	130-515
R 30	R Metal film 4K70 5% 0.2W TC250	107-447
R 31	R Metal Film 10K0 1% 0.5W TC50	115-100
R 32	R Metal Film 10K0 1% 0.5W TC50	115-100

TESTPOINTS

TP 1	Wire Wrap Terminal	805-727
TP 3	Wire Wrap Terminal	805-727
TP 4	Wire Wrap Terminal	805-727

MISCELLANEOUS

Screw pozidriv panhead M2x8	008-108
Screw pozidriv panhead M3x16	008-316
Nut hexagon M2	031-200
Lock washer D3,2/5,5x0,45	046-405
Threaded Nipple gt m3/3.5-1.25	065-435
Spacing Nipple 03,5/8-1,5	065-675
Strap 0.070m	648-070
Shrink Sleeve 4.8*15 Black	692-820
Mounting Acc. for TO-220	816-163

Rectangular Washer F. TO220	816-178
Insulation Bushing F. TO-220	816-214
TY-Wrap 150X3.6mm	832-200
Heat Sink	932-885
PCB for Linear Power Supply	971-153

I/O & Memory Bus Interface (901-407)

CAPACITORS

C 1	C Ceramic u1 -20%+80% 12V	213-017
C 2	C Ceramic u1 -20+80% 30V	213-009
C 3	C Ceramic u1 -20+80% 30V	213-009
C 4	C Tantal 15u 20% 35V	267-008
C 5	C Tantalum 4u7 20% 25V	267-004
C 6	C Tantalum 4u7 20% 25V	267-004
C 7	C Ceramic u1 -20+80% 30V	213-009
C 8	C Ceramic u1 -20+80% 30V	213-009
C 9	C Ceramic u1 -20+80% 30V	213-009
C 10	C Ceramic u1 -20+80% 30V	213-009
C 11	C Ceramic u1 -20%+80% 12V	213-017
C 12	C Ceramic u1 -20+80% 30V	213-009
C 13	C Ceramic u1 -20+80% 30V	213-009
C 14	C Ceramic u1 -20+80% 30V	213-009
C 15	C Ceramic u1 -20+80% 30V	213-009
C 16	C Ceramic 22n -20+80% 63V	213-028
C 17	C Ceramic 22n -20+80% 63V	213-028
C 18	C Ceramic 1n -20+80% 63V	213-024

DIODES

CR 1	Diode zener 1N825 C6V2 0.4W	350-637
CR 2	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 3	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 4	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 5	Diode BAV10 Si Vr-60V If-600mA	350-022

CONNECTORS

J 1	Connector Socket for 16-Pin	816-217
J 2	DIN 41651 26-POL PCB Mounted	805-918
J 3	DIN 41651 26-POL PCB Mounted	805-918
J 4	5 Pin Connector Male mod II W. Lock	805-895

INTEGRATED ANALOG CIRCUITS

QA 1	IC TL084 quad op amp	364-276
QA 2	IC LM311N comparator	364-024
QA 3	IC LM311N comparator	364-024

INTEGRATED DIGITAL CIRCUITS

QD 1	IC SN74LS138N 1-of-8 decoder/demultiplexer	364-308
QD 2	IC SN74LS259 8-bit adressable latch	364-397
QD 3	IC SN74LS259 8-bit adressable latch	364-397
QD 4	IC SN74LS259 8-bit adressable latch	364-397
QD 5	IC HEF4724BP 8-bit adessable latch	364-412
QD 6	IC HEF4724BP 8-bit adessable latch	364-412
QD 7	IC HEF4724BP 8-bit adessable latch	364-412
QD 8	IC HEF4724BP 8-bit adessable latch	364-412

QD 9	IC NE5008N D/A converter 8-bit	364-311
QD 10	IC NE5008N D/A converter 8-bit	364-311
QD 11	IC 4050 hex buffer	364-240
QD 12	IC 4050 hex buffer	364-240
QD 13	IC SN74LS03 Quad 2-input Nand gate open collector	364-329
QD 14	IC 74LS00 quad NAND gate	364-213

RESISTORS

R 1	R thick film Sil 8x10K	146-003
R 2	R thick film Sil 8x10K	146-003
R 3	R thick film Sil 8x10K	146-003
R 4	R thick film Sil 8x10K	146-003
R 5	R Metal Film 1K00 1% 0.5W TC50	114-100
R. 6	R Metal Film 1K00 1% 0.5W TC50	114-100
R 7	R Metal film 680E 5% 0.2W TC250	107-368
R 8	R Metal Film 200K 0.1% 0.1W TC15	141-059
R 9	R Metal Film 800K 0.1% 0.1W TC15	141-060
R 10	R Metal Film 10K 0.1% 0.1W TC25	141-010
R 11	R Metal film 220K 5% 0.2W TC250	107-622
R 12	R Metal film 220K 5% 0.2W TC250	107-622
R 13	R Cermet Trimpot 220K 10% 0.1W TC70	182-308
R 14	R Metal film 1K00 5% 0.2W TC250	107-410
R 15	R Metal Film 10K 0.1% 0.1W TC25	141-010
R 16	R Cermet Trimpot 1K 10% 0.5W TC70	182-310
R 17	R Metal Film 12K4 1% 0.5W TC50	115-124
R 18	R Metal film 10K0 5% 0.2W TC250	107-510
R 19	R Metal Film 5K62 1% 0.5W TC50	114-562
R 20	R Cermet Trimpot 1K 10% 0.5W TC70	182-310
R 21	R Metal Film 3K09 1% 0.5W TC50	114-309
R 22	R Metal film 4K70 5% 0.2W TC250	107-447
R 23	R Metal Film 200K 0.1% 0.1W TC15	141-059
R 24	R Metal Film 800K 0.1% 0.1W TC15	141-060
R 25	R Metal Film 10K 0.1% 0.1W TC25	141-010
R 26	R Metal film 220K 5% 0.2W TC250	107-622
R 27	R Metal film 220K 5% 0.2W TC250	107-622
R 28	R Cermet Trimpot 220K 10% 0.1W TC70	182-308
R 29	R Metal film 1K00 5% 0.2W TC250	107-410
R 30	R Metal Film 10K 0.1% 0.1W TC25	141-010
R 31	R Cermet Trimpot 1K 10% 0.5W TC70	182-310
R 32	R Metal Film 12K4 1% 0.5W TC50	115-124
R 33	R Metal film 10K0 5% 0.2W TC250	107-510
R 34	R Metal Film 5K62 1% 0.5W TC50	114-562
R 35	R Cermet Trimpot 1K 10% 0.5W TC70	182-310
R 36	R Metal Film 3K09 1% 0.5W TC50	114-309
R 37	R Metal film 4K70 5% 0.2W TC250	107-447
R 38	R Metal film 4K70 5% 0.2W TC250	107-447

TESTPOINTS

TP 1	Wire Wrap Terminal	805-727
TP 2	Wire Wrap Terminal	805-727
TP 3	Wire Wrap Terminal	805-727
TP 4	Wire Wrap Terminal	805-727

MISCELLANEOUS

	PCB for I/O & Memory Bus Interface	971-154

Keyboard (901-410)

CAPACITORS

C 1	C Tantalum 10u 20% 16V	267-000
C 2	C Ceramic u1 -20%+80% 12V	213-017
C 3	C Ceramic u1 -20%+80% 12V	213-017
C 4	C Ceramic u1 -20%+80% 12V	213-017

DIODES

CR 1	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 2	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 3	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 4	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 5	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 6	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 7	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 8	Diode BAV10 Si Vr-60V If-600mA	350-022

CONNECTORS

J 1	Connector Socket for 16-Pin	816-217

INTEGRATED DIGITAL CIRCUITS

QD 1	IC HEF4724BP 8-bit adessable latch	364-412
QD 2	IC HEF4512BP 8-input multiplexer	364-279
QD 3	IC SN74HC386N Exclusive OR-gates	364-642
QD 4	IC SN74HC386N Exclusive OR-gates	364-642
QD 5	IC 4078 8-input NOR gate	364-268
QD 6	IC HEF4013BP Dual D-type Flip-Flop	364-222
QD 7	IC SN74LS05N HEX inverters (open collector)	364-214
QD 8	IC SN74LS259 8-bit adressable latch	364-397

RESISTORS

R 1	R Metal film 1K00 5% 0.2W TC250	107-410
R 2	R Metal film 1K00 5% 0.2W TC250	107-410
R 3	R Metal film 1K00 5% 0.2W TC250	107-410
R 4	R Metal film 1K00 5% 0.2W TC250	107-410
R 5	R Metal film 390E 5% 0.2W TC250	107-339
R 6	R Metal film 390E 5% 0.2W TC250	107-339
R 7	R Metal film 2K20 5% 0.2W TC250	107-422
R 8	R Metal film 2K20 5% 0.2W TC250	107-422
R 9	R Metal film 2K20 5% 0.2W TC250	107-422
R 10	R Metal film 2K20 5% 0.2W TC250	107-422
R 11	R Metal film 2K20 5% 0.2W TC250	107-422
R 12	R Metal film 10K0 5% 0.2W TC250	107-510

SWITCHES

S 1	Marquardt Keyboard Switch	520-209
S 2	Marquardt Keyboard Switch	520-209
S 3	Marquardt Keyboard Switch	520-209
S 4	Marquardt Keyboard Switch	520-209
S 5	Marquardt Keyboard Switch	520-209
S 6	Marquardt Keyboard Switch	520-209
S 7	Marquardt Keyboard Switch	520-209
S 8	Marquardt Keyboard Switch	520-209
S 9	Marquardt Keyboard Switch	520-209
S 10	Marquardt Keyboard Switch	520-209
S 11	Marquardt Keyboard Switch	520-209
S 12	Marquardt Keyboard Switch	520-209
S 13	Marquardt Keyboard Switch	520-209
S 14	Marquardt Keyboard Switch	520-209
S 15	Marquardt Keyboard Switch	520-209
S 16	Marquardt Keyboard Switch	520-209
S 17	Marquardt Keyboard Switch with Red LED	520-210
S 18	Marquardt Keyboard Switch	520-209
S 19	Marquardt Keyboard Switch with Green LED	520-211
S 20	Marquardt Keyboard Switch	520-209
S 21	Marquardt Keyboard Switch	520-209
S 22	Marquardt Keyboard Switch	520-209
S 23	Marquardt Keyboard Switch	520-209
S 24	Marquardt Keyboard Switch	520-209
S 25	Marquardt Keyboard Switch	520-209
S 26	Marquardt Keyboard Switch	520-209
S 27	Marquardt Keyboard Switch	520-209
S 28	Marquardt Keyboard Switch	520-209
S 29	Marquardt Keyboard Switch	520-209
S 30	Marquardt Keyboard Switch	520-209
S 31	Marquardt Keyboard Switch	520-209
S 32	Marquardt Keyboard Switch	520-209
S 33	Marquardt Keyboard Switch	520-209
S 34	Marquardt Keyboard Switch	520-209
S 35	Marquardt Keyboard Switch	520-209
S 36	Marquardt Keyboard Switch	520-209
S 37	Marquardt Keyboard Switch	520-209
S 38	Marquardt Keyboard Switch	520-209
S 39	Marquardt Keyboard Switch	520-209
S 40	Marquardt Keyboard Switch	520-209
S 41	Marquardt Keyboard Switch	520-209
S 42	Marquardt Keyboard Switch	520-209
S 43	Marquardt Keyboard Switch	520-209
S 44	Marquardt Keyboard Switch	520-209

MISCELLANEOUS

Philips Screw with Countersunk Head M2*8	009-108
Nut hexagon M2	031-200
Washer 1.6/5*0.5	042-105
Keyboard Plate	932-057
Keyboard PCB	971-156

Tube Unit (901-414)

CAPACITORS

C 1	C Ceramic 100p 2% 100V NP0	213-211
C 2	C Ceramic 100p 2% 100V NP0	213-211
C 3	C Ceramic u1 -20%+80% 12V	213-017
C 4	C electrolytic 10u0 25V	261-081
C 5	MKT, 0.1/100/10, R:4*9*13, RM4	241-025
C 6	C Polycarbonate 100n 10% 400V 150PPM	242-026
C 7	C Ceramic 220p 2% 100V N750	213-218

DIODES

CR 1	Diode zener BZX79-C7V5 0.4W	350-621

CONNECTORS

J 1	CRT Socket	810-504

CHOKES

L 1	Choke HF 10uH 20% 0.3A	703-019

TRANSISTORS

Q 1	Transistor BC547B npn	360-159
Q 2	Transistor BC547B npn	360-159
Q 3	Transistor BF422 SI NPN 250V 10mA 830mW TO-92	360-230
Q 4	Transistor BF422 SI NPN 250V 10mA 830mW TO-92	360-230
Q 5	Transistor BC547B npn	360-159
Q 6	Transistor BC547B npn	360-159

RESISTORS

R 1	R Carbon Film 15E 5% 0.2W	106-215
R 2	R Carbon Film 15E 5% 0.2W	106-215
R 3	R Carbon 150E 5% 0.2W	106-315
R 4	R Carbon 150E 5% 0.2W	106-315
R 5	R Metal Film 1K5 5% 1W TC250	121-213
R 6	R Metal Film 1K5 5% 1W TC250	121-213
R 7	R Carbon Film 22K 5% 0.2W	106-522
R 8	R Carbon Film 2K7 5% 0.2W	106-427
R 9	R Carbon 150E 5% 0.2W	106-315
R 10	R Carbon Film 39E 5% 0.2W	106-239
R 11	R Carbon Film 820E 5% 0,2w	106-382
R 12	R Carbon Film 220E 5% 0.2W	106-322
R 13	R Carbon Film 100K 5% 0.2W	106-610

MISCELLANEOUS

Solder sleeve	062-622
Crimpsocket Mod. IV	805-820
Codepin Mod IV	805-821
Housing for Multiplug 12-Polet Mod. IV	805-870
Ty-Wrap 100*2,5MM	832-203
PCB for Tube Unit	971-160

CRT Driver (901-417)

CAPACITORS

C 1	C Ceramic 10n0 -20+80% 63V	213-020
C 2	C Ceramic 10n0 -20+80% 63V	213-020
C 3	C Ceramic 100n 20% 50V	213-400
C 4	C Tantalum 4u7 20% 25V	267-004
C 5	C Ceramic 1n00 -20+80% 63V	213-013
C 6	C Ceramic 100n 20% 50V	213-400
C 7	Electrolytic 220/40, 2000h/85°, R:10*20, RM2	261-084
C 8	MKT, 0.47/63/10, R:5*11*13, RM4	241-038
C 9	MKT, 3.3/63/10, R:8.5*18*26, RM9	241-053
C 10	C Polycarbonate 10n 10% 1600V 150PPM	242-010
C 11	Electrolytic 100/100, 2000h/85°,	261-024
C 12	Electrolytic 100/100, 2000h/85°,	261-024
C 13	Electrolytic 100/63, 2000h/85°, R:10*12, RM2	261-083
C 14	Electrolytic 100/25, 2000h/85°, R:6.3*11, RM2	261-073
C 15	Electrolytic 100/25, 2000h/85°, R:6.3*11, RM2	261-073
C 16	MKT, 10/63/10, A:14.5*31.5	241-028
C 17	MKT, 1/63/10, R:6*12*18, RM6	241-027
C 18	MKT, 0.68/63/10, R:5*11*18, RM6	241-030
C 19	C Polyst 4n64 1% 63V	243-301
C 20	MKT, 0.22/100/10, R:4*9*13, RM4	241-032
C 21	C Tantalum 4u7 20% 25V	267-004
C 22	C Ceramic 270p 2% 100V N750	213-213
C 23	C Ceramic 82p0 2% 100V NP0	213-124
C 24	C Polycarbonate 10n 10% 1600V 150PPM	242-010
C 25	MKT, 3.3/63/10, R:8.5*18*26, RM9	241-053
C 26	C Ceramic 100n 20% 50V	213-400
C 27	C Ceramic 100n 20% 50V	213-400
C 28	MKT, 0.1/100/10, R:4*9*13, RM4	241-025
C 29	MKT, 0.1/100/10, R:4*9*13, RM4	241-025
C 30	MKT, 0.1/100/10, R:4*9*13, RM4	241-025
C 31	C Tantal 2u2 20% 35V	267-007
C 32	Electrolytic 1000/35, 2000h/85°, R:16*25, RM2	261-082
C 33	MKT, 0.47/63/10, R:5*11*13, RM4	241-038
C 34	MKT, 0.01/400/10, R:4*9*13, RM4	241-020
C 35	Electrolytic 100/25, 2000h/85°, R:6.3*11, RM2	261-073
C 36	Electrolytic 1000/35, 2000h/85°, R:16*25, RM2	261-082
C 37	C Tantalum 10u 20% 16V	267-000
C 38	C Ceramic 100n 20% 50V	213-400
C 39	C Ceramic 100n 20% 50V	213-400
C 40	C Ceramic 270p 2% 100V N750	213-213
C 41	C Polyst 10n0 1% 63V	243-302

DIODES

CR 1	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 2	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 3	Diode BYV27-200V 2A SOT-57 Fast Recovery	350-437
CR 4	Diode BYV96D SI 800V 750mA DO14	350-430
CR 5	Diode BYV96D SI 800V 750mA DO14	350-430
CR 6	Diode BYV96D SI 800V 750mA DO14	350-430

CR 7	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 8	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 9	Diode BYV96D SI 800V 750mA DO14	350-430
CR 10	Diode BAV10 Si Vr-60V If-600mA	350-022

CONNECTORS

J 1	5 Pin Connector Male mod II W. Lock	805-895
J 2	12 Pin Connector Male mod II W. Lock	805-902
J 3	6 Pin Connector Male mod II W. Lock	805-896
J 4	4 Pin Connector Male mod II W. Lock	805-901
J 5	5 Pin Connector Male mod II W. Lock	805-895
J 6	5 Pin Connector Male mod II W. Lock	805-895

CHOKES

L 1	Linearity Corrector at 4042/46	910-145

TRANSISTORS

Q 1	Transistor BC640 SI NPN 80V 1,5A 1W TO-92	360-227
Q 2	Transistor BC557B pnp	360-160
Q 3	Transistor BC557B pnp	360-160
Q 4	Transistor BC547B npn	360-159
Q 5	Transistor BC547B npn	360-159
Q 6	Transistor BU806 SI NPN 200V 8A 60W TO-220	360-229
Q 7	Transistor BC547B npn	360-159
Q 8	Transistor BC547B npn	360-159
Q 9	Transistor BC547B npn	360-159
Q 10	Transistor BC547B npn	360-159

INTEGRATED ANALOG CIRCUITS

QA 1	IC TDA2593 hor sync comb	364-491
QA 2	IC TDA2653A Vertical deflection circuit	364-503
QA 3	IC 78MO5UC Voltage regulator 5V/1A	364-180

INTEGRATED DIGITAL CIRCUITS

QD 1	IC SN74S04N Hex Inverters	364-085
QD 2	IC 74LS04 hex inverters	364-219
QD 3	IC HEF4528B Dual monostable multivibrator	364-249

RESISTORS

R 1	R Metal Film 576E 1% 0.5W TC50	113-576
R 2	R Metal Film 1K00 1% 0.5W TC50	114-100
R 4	R Cermet Trimpot 100E 20% 0.5W TC150	182-004
R 5	R Metal Film 127K 1% 0.5W TC50	116-127
R 6	R var 10K 20% 0.5w	182-008
R 7	R Metal Film 75E 1% 0.5W TC50	140-926
R 8	R Carbon Film 5K6 5% 0.2W	106-456
R 9	R Metal Film 51K1 1% 0.5W TC50	115-511
R 10	R Carbon Film 6K8 5% 0.2W	106-468

R 11	R Carbon 10K 5% 0.2w	106-510
R 12	R Metal Film 102K 1% 0.5W TC50	116-102
R 13	R Carbon Film 6K8 5% 0.2W	106-468
R 14	R Carbon 10K 5% 0.2w	106-510
R 18	R Carbon Film 1K 5% 0.2W	106-410
R 19	R Carbon Film 10E 5% 0,2W	106-210
R 20	R Carbon Film 120E 5% 0.2W	106-312
R 21	R Cermet Trimpot 47K 20% 0.5W TC150	182-010
R 22	R Carbon Film 120K 5% 0.2W	106-612
R 23	R Metal Film 12K1 1% 0.5W TC50	115-121
R 24	R Carbon Film 82K 5% 0.2W	106-582
R 25	R Carbon Film 1K2 5% 0.2W	106-412
R 26	R Carbon Film 3K3 5% 0.2W	106-433
R 27	R Carbon Film 2M2 5% 0.5W	100-722
R 28	R Carbon Film 2K2 5% 0.2W	106-422
R 29	R Carbon Film 180K 5% 0.2W	106-618
R 30	R Carbon Film 27E 5% 0.2W	106-227
R 31	R Cermet Trimpot 47K 20% 0.5W TC150	182-010
R 32	R Carbon Film 56K 5% 0.2W	106-556
R 33	R Carbon Film 330E 5% 0.2W	106-333
R 34	R Carbon Film 470E 5% 0.2W	106-347
R 35	R Carbon Film 1M5 5% 0.5W	100-715
R 36	R Carbon Film 22K 5% 0.2W	106-522
R 37	R Cermet Trimpot 220K 20% 0.5W TC150	182-011
R 38	R Carbon Film 82K 5% 0.2W	106-582
R 39	R Carbon Film 3K3 5% 0.2W	106-433
R 40	R Carbon Film 56K 5% 0.2W	106-556
R 41	R Carbon Film 18K 5% 0.2W	106-518
R 42	R Carbon Film 4K7 5% 0.2W	106-447
R 43	R Carbon Film 22K 5% 0.2W	106-522
R 44	R Carbon Film 3E3 5% 0.2W	106-133
R 45	R Carbon Film 820E 5% 0,2w	106-382
R 46	R Carbon Film 1E5 5% 0.2W	106-115
R 47	R Carbon Film 120E 5% 0.2W	106-312
R 48	R Cermet Trimpot 47K 20% 0.5W TC150	182-010
R 49	R Carbon Film 39K 5% 0.2W	106-539
R 50	R Carbon Film 68K 5% 0.2W	106-568
R 51	R Carbon Film 270E 5% 0.2W	106-327
R 52	R Carbon Film 4K7 5% 0.2W	106-447
R 53	R Carbon Film 18K 5% 0.2W	106-518
R 54	R Metal Film 6E8 5% 1W TC250	121-212
R 55	R Carbon Film 220K 5% 0.2W	106-622
R 56	R Carbon Film 1K 5% 0.2W	106-410
R 57	R Carbon Film 1K 5% 0.2W	106-410
R 58	R Carbon Film 15K 5% 0.2W	106-515
R 59	R Carbon Film 1K5 5% 0.2W	106-415
R 60	R Carbon Film 820E 5% 0,2w	106-382
R 61	R Carbon Film 2K2 5% 0.2W	106-422
R 62	R Carbon Film 2K7 5% 0.2W	106-427
R 63	R Carbon Film 8K2 5% 0.2W	106-482
R 64	R Carbon Film 1K2 5% 0.2W	106-412
R 65	R Carbon Film 1K2 5% 0.2W	106-412
R 66	R Carbon 150E 5% 0.2W	106-315
R 67	R Carbon Film 470E 5% 0.2W	106-347

R 68	R Carbon Film 220E 5% 0.2W	106-322
R 69	R Carbon Film 100E 5% 0.2W	106-310
R 70	R Carbon Film 220E 5% 0.2W	106-322
R 71	R Carbon 10K 5% 0.2w	106-510
R 72	R Carbon Film 6K8 5% 0.2W	106-468
R 73	R Metal Film 205K 1% 0.5W TC50	116-205
R 74	R Carbon 1M 5% 0.2w	106-710
R 75	R Carbon 1M 5% 0.2w	106-710
R 76	R Carbon Film 27K 5% 0.2W	106-527
R 77	R Carbon Film 12K 5% 0.2W	106-512
R 78	R Carbon Film 470K 5% 0.2W	106-647
R 79	R Carbon Film 220K 5% 0.2W	106-622
R 80	R Carbon Film 330E 5% 0.2W	106-333
R 81	R Metal film 47K0 5% 0.2W TC250	107-547
R 82	R Metal film 39K0 5% 0.2W TC250	107-539
R 83	R Metal film 1K00 5% 0.2W TC250	107-410
R 84	R Metal film 1K00 5% 0.2W TC250	107-410

MISCELLANEOUS

	Screw pozidriv panhead M3x8	008-308
	Nut hexagon M3	031-302
	Washer |3.2/7x1	042-307
	Lock washer D3,2/5,5x0,45	046-405
	EHT Cable Ass'y 3111 100 32250	617-831
	Female Plug	805-718
	Wire Wrap Terminal	805-727
	Mounting Acc. for TO-220	816-163
	Insulation Bushing F. TO-220	816-214
	Heat Sink for TO-220 Case - FK216/SA-CB	816-250
	PCB for CRT Driver	971-163
TR 1	Line Output Transformer AT2140/16	770-690

Analog Frontend (901-421)

CAPACITORS

C 1	MKT, 4x u33 Select 100V,	241-077
C 2	MKT, 4x u33 Select 100V,	241-077
C 3	MKT, 4x u33 Select 100V,	241-077
C 4	MKT, 4x u33 Select 100V,	241-077
C 5	C Ceramic 1p2 +-P25 100V P100	213-102
C 6	C Ceramic 1p2 +-P25 100V P100	213-102
C 7	C Ceramic 1p2 +-P25 100V P100	213-102
C 8	C Ceramic 1p2 +-P25 100V P100	213-102
C 9	C Tantalum 10u 20% 16V	267-000
C 10	C Tantalum 10u 20% 16V	267-000
C 11	C Tantalum 10u 20% 16V	267-000
C 12	C Tantalum 10u 20% 16V	267-000
C 13	C Tantal 4x 68uF Select 16V	267-021
C 14	C Tantal 4x 68uF Select 16V	267-021
C 15	C Tantal 4x 68uF Select 16V	267-021
C 16	C Tantal 4x 68uF Select 16V	267-021
C 17	C Ceramic 10p 2% 100V NP0	213-113
C 18	C Ceramic 10p 2% 100V NP0	213-113
C 19	C Tantalum 10u 20% 16V	267-000
C 20	C Tantalum 10u 20% 16V	267-000
C 21	C Ceramic 10p 2% 100V NP0	213-113
C 22	C Polyst 10n0 1% 63V	243-302
C 23	C Polyst 10n0 1% 63V	243-302
C 24	C Polyst 10n0 1% 63V	243-302
C 25	C Polyst 10n0 1% 63V	243-302
C 26	C Polyst 10n0 1% 63V	243-302
C 27	C Polyst 10n0 1% 63V	243-302
C 28	C Polyst 10n0 1% 63V	243-302
C 29	C Polyst 10n0 1% 63V	243-302
C 30	C Polyst 10n0 1% 63V	243-302
C 31	C Polyst 10n0 1% 63V	243-302
C 32	C Ceramic 100n 20% 50V	213-401
C 33	C Ceramic 10p 2% 100V NP0	213-113
C 34	C Tantalum 22u 20% 16V	267-019
C 35	C Ceramic 10p 2% 100V NP0	213-113
C 36	C Ceramic 100n 20% 50V	213-401
C 37	C Ceramic 100n 20% 50V	213-401
C 38	C Tantalum 22u 20% 16V	267-019
C 39	C Ceramic 22n -20+80% 63V	213-028
C 40	Electrolytic 47/25, 2000h/85°, R:5*11, RM2	261-085
C 41	Electrolytic 47/25, 2000h/85°, R:5*11, RM2	261-085
C 42	Electrolytic 47/25, 2000h/85°, R:5*11, RM2	261-085
C 44	C Ceramic 100n 20% 50V	213-401
C 45	C Ceramic 100n 20% 50V	213-400
C 46	C Ceramic 100n 20% 50V	213-400
C 47	C Ceramic 100n 20% 50V	213-401
C 49	Electrolytic 47/25, 2000h/85°, R:5*11, RM2	261-085
C 50	C Ceramic 100n 20% 50V	213-400
C 51	C Ceramic 100n 20% 50V	213-400
C 52	Electrolytic 47/25, 2000h/85°, R:5*11, RM2	261-085

C 53	C Ceramic 100n 20% 50V	213-400
C 54	C Ceramic 100n 20% 50V	213-400
C 55	C Ceramic 100n 20% 50V	213-400
C 56	C Ceramic 100n 20% 50V	213-400
C 57	Electrolytic 47/25, 2000h/85°, R:5*11, RM2	261-085
C 58	C Ceramic 100n 20% 50V	213-400
C 59	C Ceramic 100n 20% 50V	213-400
C 60	C Ceramic 100n 20% 50V	213-400
C 61	C Ceramic 100n 20% 50V	213-400
C 62	C Ceramic 5p6 +-P25 100V NPO	213-110
C 63	C Ceramic 10p 2% 100V NP0	213-113
C 64	C Ceramic 5p6 +-P25 100V NPO	213-110
C 65	C Ceramic 5p6 +-P25 100V NPO	213-110
C 66	MKT, 0.22/100/10, R:4*9*13, RM4	241-032
C 67	MKT, 0.68/63/10, R:5*11*18, RM6	241-030
C 68	C Ceramic 100n 20% 50V	213-400
C 69	C Ceramic 100n 20% 50V	213-400
C 70	C Ceramic 100n 20% 50V	213-400
C 71	C Ceramic 100n 20% 50V	213-400
C 72	C Tantalum 10u 20% 16V	267-000
C 73	C Solid alu 4u7 20% 25V	265-000
C 76	C Tantalum 10u 20% 16V	267-000
C 77	C Solid alu 4u7 20% 25V	265-000
C 78	C Ceramic 100n 20% 50V	213-400
C 79	C Ceramic 100n 20% 50V	213-400
C 80	C Ceramic 100n 20% 50V	213-400
C 81	C Ceramic 100n 20% 50V	213-400
C 82	C Ceramic 100p 2% 100V NP0	213-125
C 83	MKT, 1/63/10, R:6*12*18, RM6	241-027
C 85	MKT, 0.1/100/10, R:4*9*13, RM4	241-025
C 86	C electrolytic 10u0 25V	261-081
C 87	C electrolytic 10u0 25V	261-081
C 90	C Ceramic 10n -20+80% 63V	213-027
C 91	C Ceramic 10n -20+80% 63V	213-027
C 92	C Ceramic 10n -20+80% 63V	213-027
C 96	C electrolytic 10u0 25V	261-081
C 97	C Ceramic 100n 20% 50V	213-400
C 102	C Ceramic 100n 20% 50V	213-400
C 103	C Ceramic 100n 20% 50V	213-400
C 104	Electrolytic 47/25, 2000h/85°, R:5*11, RM2	261-085
C 105	Electrolytic 47/25, 2000h/85°, R:5*11, RM2	261-085
C 106	Electrolytic 47/25, 2000h/85°, R:5*11, RM2	261-085
C 107	Electrolytic 47/25, 2000h/85°, R:5*11, RM2	261-085
C 108	C Ceramic 100n 20% 50V	213-400
C 109	C Ceramic 100n 20% 50V	213-400
C 110	C Ceramic 100n 20% 50V	213-400
C 111	C Ceramic 100n 20% 50V	213-400
C 112	C Ceramic 82p0 2% 100V NP0	213-124
C 113	C Ceramic 100p 2% 100V NP0	213-125
C 114	C Ceramic 220p 2% 100V N750	213-129
C 115	C Ceramic 220p 2% 100V N750	213-129
C 117	C Ceramic 22p0 2% 100V NP0	213-206
C 118	C Ceramic 22p0 2% 100V NP0	213-206
C 119	C Ceramic 22p0 2% 100V NP0	213-206

C 120	C Ceramic 15p0 2% 100V NP0	213-216
C 121	C Ceramic 15p0 2% 100V NP0	213-216
C 122	C Ceramic 22p0 2% 100V NP0	213-206
C 123	C Ceramic 22p0 2% 100V NP0	213-206
C 124	C Ceramic 100n 20% 50V	213-401
C 125	C Ceramic 100n 20% 50V	213-401
C 126	C Ceramic 100n 20% 50V	213-401
C 127	C Ceramic 100n 20% 50V	213-401
C 128	C Ceramic 10p0 2% 100V NP0	213-205
C 129	C Ceramic 100n 20% 50V	213-401
C 130	C Ceramic 22n0 -20+80% 63V	213-011

DIODES

CR 1	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 2	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 3	Diode zener BZX79-C10V 0.4W	350-657
CR 4	Diode zener BZX79-C10V 0.4W	350-657
CR 5	Diode zener BZX79-C10V 0.4W	350-657
CR 6	Diode zener BZX79-C10V 0.4W	350-657
CR 7	Diode 1N3595 SI 100V 100mA	350-415
CR 8	Diode 1N3595 SI 100V 100mA	350-415
CR 9	Diode 1N3595 SI 100V 100mA	350-415
CR 10	Diode 1N3595 SI 100V 100mA	350-415
CR 11	Diode 1N3595 SI 100V 100mA	350-415
CR 12	Diode 1N3595 SI 100V 100mA	350-415
CR 13	Diode 1N3595 SI 100V 100mA	350-415
CR 14	Diode 1N3595 SI 100V 100mA	350-415
CR 15	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 16	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 17	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 18	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 19	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 20	Diode zener BZX79-C5V6 0.4W	350-629
CR 21	LED 3mm red	350-043
CR 22	Diode zener BZX79-C4V3 0.4W	350-639
CR 23	Diode zener BZX79-C4V3 0.4W	350-639
CR 25	Diode zener BZX79-C5V6 0.4W	350-629
CR 26	Diode zener BZX79-C5V6 0.4W	350-629
CR 27	Diode BAV45 Si Vr-20V If-50mA	350-432
CR 28	Diode BAV45 Si Vr-20V If-50mA	350-432
CR 29	Diode BAV45 Si Vr-20V If-50mA	350-432
CR 30	Diode BAV45 Si Vr-20V If-50mA	350-432

CONNECTORS

J 1	16 Pin Dil Socket	816-133
J 2	16 Pin Dil Socket	816-133
J 3	16 Pin Dil Socket	816-133
J 4	16 Pin Dil Socket	816-133

RELAYS & JUMPERS

K 1	Relay Double Throw 4,5V	570-082
K 2	Relay Double Throw 4,5V	570-082

TRANSISTORS

Q 1	Transistor J109-18 n Fet	360-188
Q 2	Transistor J109-18 n Fet	360-188
Q 3	Transistor FET J106 N 25V	360-261
Q 4	Transistor FET J106 N 25V	360-261
Q 5	Transistor BC547B npn	360-159
Q 6	Transistor BC547B npn	360-159
Q 7	Transistor BC547B npn	360-159
Q 8	Transistor BC557B pnp	360-160
Q 9	Transistor BC557B pnp	360-160
Q 10	Transistor BC557B pnp	360-160
Q 11	Transistor J109-18 n Fet	360-188
Q 12	Transistor BC547B npn	360-159
Q 13	Transistor BC557B pnp	360-160
Q 14	Transistor J109-18 n Fet	360-188
Q 15	Transistor J109-18 n Fet	360-188
Q 16	Transistor BC547B npn	360-159
Q 17	Transistor BC547B npn	360-159
Q 18	Transistor BC557B pnp	360-160
Q 19	Transistor BC557B pnp	360-160
Q 20	Transistor JFet-N J112, TO92	360-114
Q 21	Transistor JFet-N J112, TO92	360-114
Q 22	Transistor JFet-N J112, TO92	360-114
Q 23	Transistor JFet-N J112, TO92	360-114
Q 24	Transistor JFet-N J112, TO92	360-114
Q 25	Transistor JFet-N J112, TO92	360-114
Q 26	Transistor JFet-N J112, TO92	360-114
Q 27	Transistor JFet-N J112, TO92	360-114
Q 28	Transistor BC547B npn	360-159
Q 29	Transistor BC547B npn	360-159
Q 30	Transistor BC547B npn	360-159
Q 31	Transistor BC547B npn	360-159
Q 32	Transistor BC547B npn	360-159
Q 33	Transistor BC547B npn	360-159
Q 34	Transistor BC547B npn	360-159
Q 35	Transistor BC557B pnp	360-160
Q 36	Transistor BC557B pnp	360-160
Q 37	Transistor BC557B pnp	360-160
Q 38	Transistor BC557B pnp	360-160
Q 39	Transistor BC557B pnp	360-160
Q 40	Transistor BC557B pnp	360-160
Q 41	Transistor BC557B pnp	360-160
Q 42	Transistor J109-18 n Fet	360-188
Q 43	Transistor JFet-N J111, TO92	360-116
Q 44	Transistor JFet-N J111, TO92	360-116
Q 45	Transistor J109-18 n Fet	360-188
Q 46	Transistor J109-18 n Fet	360-188
Q 47	Transistor J109-18 n Fet	360-188

Q 48	Transistor J109-18 n Fet	360-188
Q 49	Transistor JFet-N J111, TO92	360-116
Q 51	Transistor BC547B npn	360-159
Q 52	Transistor BC547B npn	360-159
Q 53	Transistor BC547B npn	360-159
Q 54	Transistor BC547B npn	360-159
Q 55	Transistor BC557B pnp	360-160
Q 56	Transistor BC557B pnp	360-160
Q 57	Transistor BC557B pnp	360-160
Q 58	Transistor BC557B pnp	360-160
Q 59	Transistor BC557B pnp	360-160
Q 60	Transistor PN3686-J35Z JFET	360-216
Q 61	Transistor PN3686-J35Z JFET	360-216
Q 62	Transistor PN3686-J35Z JFET	360-216
Q 63	Transistor PN3686-J35Z JFET	360-216
Q 64	Transistor BC547B npn	360-159
Q 65	Transistor BC547B npn	360-159
Q 66	Transistor BC547B npn	360-159
Q 67	Transistor BC547B npn	360-159
Q 68	Transistor BSR50 npn	360-201
Q 69	Transistor BSR50 npn	360-201
Q 70	Transistor BC557B pnp	360-160
Q 71	Transistor J109-18 n Fet	360-188
Q 72	Transistor PN4416 Jfet UHF	360-108
Q 73	Transistor JFet-N J112, TO92	360-114
Q 74	Transistor BC557B pnp	360-160

INTEGRATED ANALOG CIRCUITS

QA 1	IC 5534A op amp	364-639
QA 2	IC 5534A op amp	364-639
QA 3	IC 5534A op amp	364-639
QA 4	IC 5534A op amp	364-639
QA 5	IC 5534A op amp	364-639
QA 6	IC 5534A op amp	364-639
QA 7	IC 5534A op amp	364-639
QA 8	IC NE5532A Dual OP-Amp low noise	364-640
QA 9	IC NE5532A Dual OP-Amp low noise	364-640
QA 10	IC NE5532A Dual OP-Amp low noise	364-640
QA 11	IC NE5532A Dual OP-Amp low noise	364-640
QA 16	IC 5534A op amp	364-639
QA 17	IC LF356 op amp	364-203
QA 18	IC LF356 op amp	364-203
QA 19	IC LF356 op amp	364-203
QA 20	IC LF356 op amp	364-203
QA 21	IC TL084 quad op amp	364-276
QA 22	IC TL084 quad op amp	364-276
QA 23	IC LM311N comparator	364-024
QA 24	IC LM311N comparator	364-024
QA 25	IC LF356 op amp	364-203
QA 26	IC HA5320 Sample hold amp	364-691
QA 27	IC ADC84KG-12 12-bit A/D converter	364-414

INTEGRATED DIGITAL CIRCUITS

QD 1	IC SN74LS138N 1-of-8 decoder/demultiplexer	364-308
QD 2	IC HEF4724BP 8-bit adessable latch	364-412
QD 3	IC HEF4724BP 8-bit adessable latch	364-412
QD 4	IC SN74LS139N Dual 1 of-4 decoder/demultiplexer	364-376
QD 5	IC SN74LS05N HEX inverters (open collector)	364-214
QD 6	IC 74LS00 quad NAND gate	364-213
QD 7	IC SN74HCT368N Hex Bus Drivers	364-669
QD 8	IC SN74HCT368N Hex Bus Drivers	364-669
QD 10	IC SN74LS139N Dual 1 of-4 decoder/demultiplexer	364-376

RESISTORS

R 1	R Metal Film 294K 0.1% 0.2W TC25	140-984
R 2	R Metal Film 294K 0.1% 0.2W TC25	140-984
R 3	R Metal Film 294K 0.1% 0.2W TC25	140-984
R 4	R Metal Film 294K 0.1% 0.2W TC25	140-984
R 5	R Metal Film 32K4 0.1% 0.2W TC25	141-005
R 6	R Metal Film 32K4 0.1% 0.2W TC25	141-005
R 7	R Metal Film 32K4 0.1% 0.2W TC25	141-005
R 8	R Metal Film 32K4 0.1% 0.2W TC25	141-005
R 9	R Carbon Film 68E 5% 0.2W	106-268
R 10	R Carbon Film 68E 5% 0.2W	106-268
R 11	R Cermet Trimpot 470E 20% 0.5W TC70	182-302
R 12	R Cermet Trimpot 470E 20% 0.5W TC70	182-302
R 13	R Metal Film 267E 1% 0.5W TC50	113-267
R 14	R Metal Film 267E 1% 0.5W TC50	113-267
R 15	R Carbon Film 1K8 5% 0.2W	106-418
R 16	R Carbon Film 1K8 5% 0.2W	106-418
R 17	R Carbon Film 1K8 5% 0.2W	106-418
R 18	R Carbon Film 1K8 5% 0.2W	106-418
R 19	R Carbon Film 4K7 5% 0.2W	106-447
R 20	R Carbon Film 4K7 5% 0.2W	106-447
R 21	R Carbon Film 4K7 5% 0.2W	106-447
R 22	R Carbon Film 4K7 5% 0.2W	106-447
R 23	R Carbon Film 5K6 5% 0.2W	106-456
R 24	R Carbon Film 5K6 5% 0.2W	106-456
R 25	R Metal film 12K0 5% 0.2W TC250	107-512
R 26	R Metal film 12K0 5% 0.2W TC250	107-512
R 27	R Metal film 12K0 5% 0.2W TC250	107-512
R 28	R Metal film 12K0 5% 0.2W TC250	107-512
R 29	R Metal film 1K00 5% 0.2W TC250	107-410
R 30	R Metal film 1K00 5% 0.2W TC250	107-410
R 31	R Metal film 1K00 5% 0.2W TC250	107-410
R 32	R Metal film 1K00 5% 0.2W TC250	107-410
R 33	R Metal film 12K0 5% 0.2W TC250	107-512
R 34	R Metal film 12K0 5% 0.2W TC250	107-512
R 35	R Metal film 12K0 5% 0.2W TC250	107-512
R 36	R Metal film 12K0 5% 0.2W TC250	107-512
R 37	R Carbon Film 33K 5% 0.2W	106-533
R 38	R Carbon Film 33K 5% 0.2W	106-533
R 39	R Carbon Film 15K 5% 0.2W	106-515
R 40	R Carbon Film 15K 5% 0.2W	106-515

R 41	R Carbon Film 56K 5% 0.2W	106-556
R 42	R Carbon Film 56K 5% 0.2W	106-556
R 43	R Carbon 10K 5% 0.2w	106-510
R 44	R Carbon 10K 5% 0.2w	106-510
R 45	R Carbon Film 100K 5% 0.2W	106-610
R 46	R Carbon Film 100E 5% 0.2W	106-310
R 47	R Carbon Film 100E 5% 0.2W	106-310
R 48	R Carbon Film 100E 5% 0.2W	106-310
R 49	R Metal Film 19K1 0.1% 0.2W TC25	140-983
R 50	R Metal Film 2K 0.1% 1/8W TC50	140-495
R 51	R Metal Film 118E 1% 0.5W TC50	113-118
R 52	R Carbon 10K 5% 0.2w	106-510
R 53	R Carbon Film 15K 5% 0.2W	106-515
R 54	R Carbon Film 56K 5% 0.2W	106-556
R 55	R Carbon 10K 5% 0.2w	106-510
R 56	R Metal Film 49K9 1% 0.5W TC50	115-499
R 57	R Metal Film 475E 1% 0.5W TC50	113-475
R 58	R Metal Film 27E4 1% 0.5W TC50	112-274
R 59	R Metal Film 1K00 1% 0.5W TC50	140-477
R 60	R Metal Film 1K00 1% 0.5W TC50	140-477
R 61	R Metal Film 1K18 1% 0.5W TC50	114-118
R 62	R Metal film 22E0 5% 0.2W TC250	107-222
R 63	R Metal film 22E0 5% 0.2W TC250	107-222
R 64	R Metal Film 976E 1% 0.5W TC50	113-976
R 65	R Metal Film 147E 1% 0.5W TC50	113-147
R 66	R Metal Film 1K00 1% 0.5W TC50	140-477
R 67	R Metal Film 1K00 1% 0.5W TC50	140-477
R 68	R Metal Film 1K21 1% 0.5W TC50	114-121
R 69	R Metal Film 909E 1% 0.5W TC50	113-909
R 70	R Metal Film 196E 1% 0.5W TC50	113-196
R 71	R Metal Film 1K00 1% 0.5W TC50	140-477
R 72	R Metal Film 1K00 1% 0.5W TC50	140-477
R 73	R Metal Film 1K27 1% 0.5W TC50	114-127
R 74	R Metal Film 909E 1% 0.5W TC50	113-909
R 75	R Metal Film 100E 1% 0.5W TC50	113-100
R 76	R Metal Film 1K00 1% 0.5W TC50	140-477
R 77	R Metal Film 1K00 1% 0.5W TC50	140-477
R 78	R Metal Film 1K33 1% 0.5W TC50	114-133
R 79	R Metal Film 422E 1% 0.5W TC50	113-422
R 80	R Metal Film 51K1 1% 0.5W TC50	115-511
R 81	R Carbon Film 27K 5% 0.2W	106-527
R 82	R Metal Film 4K75 1% 0.5W TC50	114-475
R 83	R Cermet Trimpot 470E 20% 0.75W TC70	182-318
R 84	R Carbon Film 33K 5% 0.2W	106-533
R 85	R Carbon Film 15K 5% 0.2W	106-515
R 86	R Carbon Film 56K 5% 0.2W	106-556
R 87	R Carbon Film 5K6 5% 0.2W	106-456
R 88	R Carbon Film 33K 5% 0.2W	106-533
R 89	R Carbon Film 33K 5% 0.2W	106-533
R 90	R Carbon Film 5K6 5% 0.2W	106-456
R 91	R Carbon Film 15K 5% 0.2W	106-515
R 92	R Carbon Film 15K 5% 0.2W	106-515
R 93	R Carbon Film 56K 5% 0.2W	106-556
R 94	R Carbon Film 56K 5% 0.2W	106-556

R 95	R Carbon Film 5K6 5% 0.2W	106-456
R 96	R Carbon Film 5K6 5% 0.2W	106-456
R 97	R Carbon Film 100K 5% 0.2W	106-610
R 98	R Carbon Film 33E 5% 0.2W	106-233
R 99	R Carbon Film 33E 5% 0.2W	106-233
R 100	R Carbon Film 2M2 5% 0.2W	106-722
R 101	R Metal Film 8K66 0.1% 0.2W TC25	140-982
R 102	R Metal film 3K92 0.1% 0.25w TC25	141-004
R 103	R Carbon Film 47E 5% 0.2W	106-247
R 104	R Metal film 4k99 0.1% 0.25w TC25	140-981
R 105	R Metal Film 499K 1% 0.5W TC50	116-499
R 106	R Metal film 20K0 0.5% 0.25w TC25	140-473
R 107	R Metal Film 432K 1% 0.5W TC50	116-432
R 108	R Metal Film 8K66 0.1% 0.2W TC25	140-982
R 109	R Metal film 4k99 0.1% 0.25w TC25	140-981
R 110	R Carbon 1M 5% 0.2w	106-710
R 111	R Carbon Film 560K 5% 0.2W	106-656
R 112	R Metal Film 3K30 0.1% 0.1W TC25	141-203
R 113	R Metal Film 8K66 0.1% 0.2W TC25	140-982
R 114	R Metal film 3K92 0.1% 0.25w TC25	141-004
R 115	R Carbon Film 47E 5% 0.2W	106-247
R 116	R Carbon Film 100E 5% 0.2W	106-310
R 117	R Metal Film 8K66 0.1% 0.2W TC25	140-982
R 118	R Metal film 3K92 0.1% 0.25w TC25	141-004
R 119	R Carbon Film 47E 5% 0.2W	106-247
R 120	R thick film Sil 8x47K	146-005
R 127	R thick film Sil 8x10K	146-003
R 128	R Metal film 1K00 5% 0.2W TC250	107-410
R 129	R Cermet Trimpot 4K7 20% 0.75W TC70	182-319
R 130	R Metal film 12K0 5% 0.2W TC250	107-512
R 131	R Metal film 12K0 5% 0.2W TC250	107-512
R 132	R Metal film 12K0 5% 0.2W TC250	107-512
R 133	R Metal film 12K0 5% 0.2W TC250	107-512
R 134	R Carbon Film 56K 5% 0.2W	106-556
R 135	R Carbon Film 56K 5% 0.2W	106-556
R 136	R Carbon Film 56K 5% 0.2W	106-556
R 137	R Carbon Film 56K 5% 0.2W	106-556
R 138	R Carbon Film 56K 5% 0.2W	106-556
R 139	R Carbon Film 56K 5% 0.2W	106-556
R 140	R Carbon Film 56K 5% 0.2W	106-556
R 141	R Carbon 10K 5% 0.2w	106-510
R 142	R Carbon Film 5K6 5% 0.2W	106-456
R 143	R Carbon Film 5K6 5% 0.2W	106-456
R 144	R Carbon Film 5K6 5% 0.2W	106-456
R 145	R Carbon Film 5K6 5% 0.2W	106-456
R 146	R Carbon 10K 5% 0.2w	106-510
R 147	R Carbon 10K 5% 0.2w	106-510
R 148	R Carbon Film 5K6 5% 0.2W	106-456
R 149	R Carbon Film 150K 5% 0.2W	106-615
R 150	R Metal film 1K00 5% 0.2W TC250	107-410
R 151	R Carbon Film 1K 5% 0.2W	106-410
R 152	R Carbon Film 1K 5% 0.2W	106-410
R 153	R Metal film 1K00 5% 0.2W TC250	107-410
R 154	R Metal film 330K 5% 0.2W TC250	107-633

R 155	R Carbon Film 330K 5% 0.2W	106-633
R 156	R Cermet Trimpot 10K 20% 0.75W TC70	182-320
R 157	R Cermet Trimpot 10K 20% 0.75W TC70	182-320
R 158	R Carbon Film 100E 5% 0.2W	106-310
R 159	R Metal film 100E 5% 0.2W TC250	107-310
R 160	R Carbon Film 100K 5% 0.2W	106-610
R 161	R Metal film 100K 5% 0.2W TC250	107-610
R 162	R Carbon Film 47E 5% 0.2W	106-247
R 163	R Carbon Film 47E 5% 0.2W	106-247
R 164	R Metal film 330K 5% 0.2W TC250	107-633
R 165	R Carbon Film 330K 5% 0.2W	106-633
R 166	R Metal film 1K00 5% 0.2W TC250	107-410
R 167	R Carbon Film 1K 5% 0.2W	106-410
R 168	R Carbon Film 33K 5% 0.2W	106-533
R 169	R Carbon Film 12K 5% 0.2W	106-512
R 170	R Carbon Film 33K 5% 0.2W	106-533
R 171	R Carbon Film 33K 5% 0.2W	106-533
R 172	R Carbon Film 33K 5% 0.2W	106-533
R 173	R Carbon Film 15K 5% 0.2W	106-515
R 175	R Carbon Film 15K 5% 0.2W	106-515
R 176	R Carbon Film 15K 5% 0.2W	106-515
R 177	R Carbon Film 15K 5% 0.2W	106-515
R 178	R Carbon Film 56K 5% 0.2W	106-556
R 179	R Carbon 1M 5% 0.2w	106-710
R 180	R Carbon Film 56K 5% 0.2W	106-556
R 181	R Carbon Film 56K 5% 0.2W	106-556
R 182	R Carbon Film 56K 5% 0.2W	106-556
R 183	R Carbon Film 2K7 5% 0.2W	106-427
R 184	R Carbon Film 5K6 5% 0.2W	106-456
R 185	R Carbon 10K 5% 0.2w	106-510
R 186	R Carbon Film 5K6 5% 0.2W	106-456
R 187	R Carbon Film 5K6 5% 0.2W	106-456
R 188	R Carbon Film 5K6 5% 0.2W	106-456
R 189	R Carbon Film 22E 5% 0.2W	106-222
R 190	R Carbon Film 100K 5% 0.2W	106-610
R 191	R Carbon Film 1K 5% 0.2W	106-410
R 192	R Metal film 470K 5% 0.2W TC250	107-647
R 193	R Cermet Trimpot 10K 20% 0.75W TC70	182-320
R 194	R Carbon Film 1K 5% 0.2W	106-410
R 195	R Carbon Film 100E 5% 0.2W	106-310
R 196	R Metal film 560K 5% 0.2W TC250	107-656
R 197	R Metal film 560K 5% 0.2W TC250	107-656
R 198	R Cermet Trimpot 10K 20% 0.75W TC70	182-320
R 199	R Carbon Film 1K 5% 0.2W	106-410
R 200	R Metal film 4k99 0.1% 0.25w TC25	140-981
R 201	R Metal film 4k99 0.1% 0.25w TC25	140-981
R 202	R Carbon 10K 5% 0.2w	106-510
R 203	R Carbon Film 100K 5% 0.2W	106-610
R 204	R Carbon Film 47E 5% 0.2W	106-247
R 206	R Cermet Trimpot 22K 20% 0.3W TC70	182-303
R 207	R Metal Film 14K0 1% 0.5W TC50	115-140
R 208	R Cermet Trimpot 470E 20% 0.75W TC70	182-318
R 209	R Metal Film 2K15 1% 0.5W TC50	114-215
R 211	R Carbon Film 560K 5% 0.2W	106-656

R 212	R Carbon Film 1K8 5% 0.2W	106-418
R 213	R Carbon Film 5K6 5% 0.2W	106-456
R 214	R Carbon Film 5K6 5% 0.2W	106-456
R 215	R Carbon Film 4K7 5% 0.2W	106-447
R 216	R Carbon Film 330E 5% 0.2W	106-333
R 217	R Carbon Film 1K 5% 0.2W	106-410
R 218	R Carbon 10K 5% 0.2w	106-510
R 219	R Carbon 10K 5% 0.2w	106-510
R 220	R Carbon Film 27K 5% 0.2W	106-527
R 221	R Carbon Film 27K 5% 0.2W	106-527
R 222	R Metal film 1K00 5% 0.2W TC250	107-410
R 223	R Metal film 1K00 5% 0.2W TC250	107-410
R 224	R Metal film 47E0 5% 0.2W TC250	107-247
R 225	R Metal film 47E0 5% 0.2W TC250	107-247
R 228	R Metal Film 4K99 1% 0.5W TC50	114-499
R 231	R Cermet Trimpot 470E 20% 0.5W TC70	182-302
R 232	R Cermet Trimpot 470E 20% 0.75W TC70	182-318
R 233	R Cermet Trimpot 470E 20% 0.5W TC70	182-302
R 234	R Cermet Trimpot 470E 20% 0.75W TC70	182-318
R 235	R Metal Film 4K75 1% 0.5W TC50	114-475
R 236	R Metal Film 4K75 1% 0.5W TC50	114-475
R 237	R Metal Film 4K75 1% 0.5W TC50	114-475
R 238	R Metal Film 4K75 1% 0.5W TC50	114-475
R 239	R Metal Film 4K99 1% 0.5W TC50	114-499
R 240	R Metal Film 4K99 1% 0.5W TC50	114-499
R 241	R Metal Film 4K99 1% 0.5W TC50	114-499
R 242	R Metal Film 4K99 1% 0.5W TC50	114-499
R 243	R Carbon Film 22E 5% 0.2W	106-222
R 244	R Carbon Film 22E 5% 0.2W	106-222
R 245	R Carbon Film 22E 5% 0.2W	106-222
R 246	R Carbon Film 22E 5% 0.2W	106-222
R 247	R Carbon Film 100E 5% 0.2W	106-310
R 248	R Carbon Film 100E 5% 0.2W	106-310
R 249	R Carbon Film 6K8 5% 0.2W	106-468
R 250	R Carbon Film 3K9 5% 0,2W	106-439
R 251	R Carbon Film 6K8 5% 0.2W	106-468
R 252	R Carbon Film 6K8 5% 0.2W	106-468
R 253	R Carbon Film 100K 5% 0.2W	106-610
R 254	R Carbon Film 100K 5% 0.2W	106-610
R 255	R Metal film 22K0 5% 0.2W TC250	107-522
R 256	R Metal film 22K0 5% 0.2W TC250	107-522
R 257	R Cermet Trimpot 100K 20% 0.75W TC70	182-321
R 258	R Cermet Trimpot 100K 20% 0.75W TC70	182-321
R 261	R Carbon Film 56K 5% 0.2W	106-556
R 262	R Carbon Film 33M 10% 1/8W 140PPM	109-021
R 263	R Carbon Film 2K7 5% 0.2W	106-427
R 264	R Metal film 10K0 5% 0.2W TC250	107-510
R 265	R Metal film 33E0 5% 0.2W TC250	107-233
R 266	R Metal film 33E0 5% 0.2W TC250	107-233
R 267	R Metal film 47E0 5% 0.2W TC250	107-247

MISCELLANEOUS

tubular rivet 02.5x0.25x7	060-270
Solder sleeve	062-625
Coax Cable 50E	616-064
Wire Electrical Tinned 0.5mm	648-050
Wire Electrical Tinned 0.5mm	648-050
Teflon Sleeving 0O 8X10 Clear	691-803
Sleeving Heat Shrinkable Black 1/8" RNF 100	692-006
Female Plug	805-718
Wire Wrap Terminal	805-727
14 Pin Dil Socket	816-131
Dual-in-Line Socket 16 Pin Sil	816-210
Board Extractor	857-017
Conducter Rail C1	931-036
PCB Analog Frontend	971-167
Adhesive Mark. Label 1	992-001
Adhesive marking label 2	992-002
Adhesive marking label 3	992-003

Arithmetical Unit (901-527)

CAPACITORS

C 4	C Ceramic 100n 20% 50V	213-400
C 5	C Ceramic 100n 20% 50V	213-400
C 6	C Ceramic 100n 20% 50V	213-400
C 7	C Ceramic 100n 20% 50V	213-400
C 8	C Ceramic 100n 20% 50V	213-400
C 9	C Ceramic 100n 20% 50V	213-400
C 10	C Ceramic 100n 20% 50V	213-400
C 11	C Ceramic 100n 20% 50V	213-400
C 12	C Ceramic 100n 20% 50V	213-400
C 13	C Ceramic 100n 20% 50V	213-400
C 15	C Ceramic 100n 20% 50V	213-400
C 16	C Ceramic 100n 20% 50V	213-400
C 17	C Ceramic 100n 20% 50V	213-400
C 19	C Ceramic 100n 20% 50V	213-400
C 20	C solid AL 10u 20% 16V	265-008
C 21	C solid AL 10u 20% 16V	265-008
C 22	C solid AL 10u 20% 16V	265-008
C 23	C solid AL 10u 20% 16V	265-008
C 24	C solid AL 10u 20% 16V	265-008
C 25	C Ceramic 100n 20% 50V	213-400
C 26	C Ceramic 100n 20% 50V	213-400
C 27	C Ceramic 100n 20% 50V	213-400
C 28	C Ceramic 100n 20% 50V	213-400
C 29	C Ceramic 100n 20% 50V	213-400
C 30	C Ceramic 100n 20% 50V	213-400
C 31	C Ceramic 100n 20% 50V	213-400
C 32	C Ceramic 100n 20% 50V	213-400
C 34	C Ceramic 100n 20% 50V	213-400
C 35	C Ceramic 100n 20% 50V	213-400
C 36	C Ceramic 100n 20% 50V	213-400
C 37	C Ceramic 100n 20% 50V	213-400
C 38	C Ceramic 100n 20% 50V	213-400
C 39	C Ceramic 100n 20% 50V	213-400
C 40	C Ceramic 100n 20% 50V	213-400
C 41	C Ceramic 100n 20% 50V	213-400
C 42	C Ceramic 100n 20% 50V	213-400
C 43	C Ceramic 100n 20% 50V	213-400
C 45	C Ceramic 100n 20% 50V	213-400
C 46	C Ceramic 100n 20% 50V	213-400
C 47	C solid AL 10u 20% 16V	265-008
C 48	C solid AL 10u 20% 16V	265-008

CONNECTORS

J 2	Connector Socket for 14-Pin	816-218

CHOKES

L 1	COIL 15MHz	731-203
L 2	COIL 15MHz	731-203

INTEGRATED DIGITAL CIRCUITS

QD 1	IC 74LS08 quad AND gate	364-270
QD 2	IC 74LS08 quad AND gate	364-270
QD 3	IC 74LS08 quad AND gate	364-270
QD 4	IC 74LS08 quad AND gate	364-270
QD 5	IC 74LS00 quad NAND gate	364-213
QD 6	IC SN74S00N Quadruple 2-Input Nand Gates	364-082
QD 7	IC SN74LS03 Quad 2-input Nand gate open collector	364-329
QD 8	IC SN74LS03 Quad 2-input Nand gate open collector	364-329
QD 9	IC 74LS00 quad NAND gate	364-213
QD 10	IC SN74LS27N Triple 3-input NOR gate	364-299
QD 11	IC 74LS10 tripl NAND gate	364-300
QD 12	IC 74LS20 dual NAND gate	364-402
QD 13	IC 74LS11 tripl AND gate	364-406
QD 15	IC 74LS04 hex inverters	364-219
QD 16	IC 4049 hex inv buffer	364-224
QD 17	IC 74LS04 hex inverters	364-219
QD 18	IC SN74LS245 Octal bus transceiver	364-332
QD 19	IC SN74LS245 Octal bus transceiver	364-332
QD 20	IC SN74LS138N 1-of-8 decoder/demultiplexer	364-308
QD 21	IC SN74LS259 8-bit adressable latch	364-397
QD 22	IC HEF40097BP 3-state HEX non-inverting buffers	364-264
QD 23	IC HEF40097BP 3-state HEX non-inverting buffers	364-264
QD 24	IC HEF40097BP 3-state HEX non-inverting buffers	364-264
QD 25	IC HEF40097BP 3-state HEX non-inverting buffers	364-264
QD 26	IC HEF4029BP Synchronous up/down counter	364-269
QD 27	IC HEF4029BP Synchronous up/down counter	364-269
QD 28	IC HEF4029BP Synchronous up/down counter	364-269
QD 29	IC 74LS244 oct buffer	364-321
QD 30	IC 74LS244 oct buffer	364-321
QD 31	IC HEF40097BP 3-state HEX non-inverting buffers	364-264
QD 32	IC 4027 dual JK ff	364-237
QD 33	IC SN74LS138N 1-of-8 decoder/demultiplexer	364-308
QD 35	IC 74LS244 oct buffer	364-321
QD 36	IC 74LS244 oct buffer	364-321
QD 37	IC 2114-Static RAM	364-377
QD 38	IC 2114-Static RAM	364-377
QD 39	IC 2114-Static RAM	364-377
QD 40	IC 2114-Static RAM	364-377
QD 41	RE201 Arithmetical Unit QD41	368-302
QD 42	RE201 Arithmetical Unit QD42	368-303
QD 43	IC HEF4040BP 12-stage binary counter	364-260
QD 44	IC HEF40097BP 3-state HEX non-inverting buffers	364-264
QD 45	IC SN74LS367N HEX buffer/driver 3-state	364-400
QD 46	IC AM25LS22N 8-bit shift register	364-413
QD 47	IC AM25LS22N 8-bit shift register	364-413
QD 48	IC AM25LS22N 8-bit shift register	364-413
QD 49	IC AM25LS22N 8-bit shift register	364-413

QD 50	IC AM25LS22N 8-bit shift register	364-413
QD 51	IC AM25LS22N 8-bit shift register	364-413
QD 52	IC AM25LS22N 8-bit shift register	364-413
QD 53	IC AM25LS22N 8-bit shift register	364-413
QD 54	IC SN74LS384N 8-bit two's-complement multipliers	367-008
QD 55	IC SN74LS384N 8-bit two's-complement multipliers	367-008
QD 56	IC SN74LS384N 8-bit two's-complement multipliers	367-008
QD 57	IC SN74LS384N 8-bit two's-complement multipliers	367-008
QD 58	IC SN74LS384N 8-bit two's-complement multipliers	367-008
QD 59	IC SN74LS384N 8-bit two's-complement multipliers	367-008
QD 60	IC SN74LS384N 8-bit two's-complement multipliers	367-008
QD 61	IC SN74LS384N 8-bit two's-complement multipliers	367-008
QD 62	IC 74LS74 dual D ff	364-185
QD 63	IC SN74LS138N 1-of-8 decoder/demultiplexer	364-308
QD 64	IC SN74LS138N 1-of-8 decoder/demultiplexer	364-308
QD 65	IC 74LS374 oct D ff	364-303
QD 66	RE201 901-527 PROM 256x8 Program	368-099
QD 67	IC 74LS157 quad 2-1 MUX	364-407
QD 68	IC AM25LS15 Quad serial adder/subtractor	364-417
QD 69	IC AM25LS15 Quad serial adder/subtractor	364-417
QD 70	IC 74LS174 hex D ff	364-271
QD 71	IC 74LS266 quad XNOR gate	364-416
QD 72	IC 74S74 dual D ff	364-094
QD 73	IC 74LS163 bin counter	364-408
QD 74	IC 74LS163 bin counter	364-408
QD 75	IC 74LS163 bin counter	364-408
QD 76	IC 74LS163 bin counter	364-408
QD 77	IC SN74LS112N Dual J-K edge-triggered flip-flop	364-405
QD 78	IC 74LS74 dual D ff	364-185
QD 79	Crystal Oscillator 14.08 MHz 20ppm	910-148

RESISTORS

R 1	R thick film Sil 8x47K	146-005
R 2	R thick film Sil 8x47K	146-005
R 3	R Metal film 1K00 5% 0.2W TC250	107-410
R 4	R Metal film 1K00 5% 0.2W TC250	107-410
R 5	R Metal film 10K0 5% 0.2W TC250	107-510
R 6	R Metal film 10K0 5% 0.2W TC250	107-510
R 7	R Metal film 1K00 5% 0.2W TC250	107-410
R 8	R Metal film 1K00 5% 0.2W TC250	107-410
R 9	R Metal film 10K0 5% 0.2W TC250	107-510
R 10	R Metal film 10K0 5% 0.2W TC250	107-510
R 11	R Metal film 1K00 5% 0.2W TC250	107-410
R 12	R Metal film 10K0 5% 0.2W TC250	107-510
R 15	R Metal film 1K00 5% 0.2W TC250	107-410
R 16	R Metal film 10K0 5% 0.2W TC250	107-510

MISCELLANEOUS

tubular rivet 02.5x0.25x7	060-270
Female Plug	805-718
Wire Wrap Terminal	805-727
16 Pin Dil Socket	816-133
24 Pin Dil Socket	816-134
18 Pin DIL Socket	816-183
20 Pin DIL Socket	816-184
Solder Terminal 0.1 O2	823-303
Board Extractor	857-017
Conducter Rail C1	931-036
PCB Arithmetical Unit	971-217

Static CPU (901-788)

BATTERIES

BT 1	Battery Nickel-Cadmium 2,4W	431-004

CAPACITORS

C 1	C Ceramic 10n -20+80% 63V	213-027
C 2	C Ceramic 82p0 2% 100V NP0	213-124
C 3	C Solid alu 4u7 20% 25V	265-000
C 4	C solid AL 33u 20% 10V	265-005
C 5	C Ceramic 100n 20% 50V	213-400
C 6	C Ceramic 100n 20% 50V	213-400
C 7	C solid AL 33u 20% 10V	265-005
C 8	C solid AL 33u 20% 10V	265-005
C 9	C solid AL 10u 20% 16V	265-008
C 10	C Ceramic 100n 20% 50V	213-400
C 14	C Ceramic 100n 20% 50V	213-400
C 15	C Ceramic 100n 20% 50V	213-400
C 16	C Ceramic 100n 20% 50V	213-400
C 17	C Ceramic 100n 20% 50V	213-400
C 18	C Ceramic 100n 20% 50V	213-400
C 19	C solid AL 10u 20% 16V	265-008
C 20	C Ceramic 100n 20% 50V	213-400
C 21	C Ceramic 100n 20% 50V	213-400
C 22	C Ceramic 100n 20% 50V	213-400
C 23	C Ceramic 100n 20% 50V	213-400
C 27	C Ceramic 100n 20% 50V	213-400
C 28	C Ceramic 100n 20% 50V	213-400
C 29	C Ceramic 100n 20% 50V	213-400
C 30	C Ceramic 100n 20% 50V	213-400
C 31	C Ceramic 100n 20% 50V	213-400
C 32	C Ceramic 100n 20% 50V	213-400
C 33	C Ceramic 100n 20% 50V	213-400
C 34	C Ceramic 100n 20% 50V	213-400
C 35	C Ceramic 100n 20% 50V	213-400
C 36	C solid AL 33u 20% 10V	265-005
C 37	C solid AL 33u 20% 10V	265-005

DIODES

CR 1	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 2	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 3	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 4	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 5	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 6	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 7	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 8	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 9	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 10	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 12	Diode Schottky BAT41 S 150V 250mA	350-061
CR 13	Diode BAV10 Si Vr-60V If-600mA	350-022

CR 14	Diode zener BZX79-C3V6 0.4W	350-626

CONNECTORS

J 2	16 Pin Dil Socket	816-133

RELAYS & JUMPERS

K 1	16 Pin Dil Socket	816-133
K 2	16 Pin Dil Socket	816-133
K 3	2-pol amp connector	805-951
K 4	3 Pin AMP mod II Terminal List, Straight	805-894

CHOKES

L 1	COIL 15MHz	731-203
L 2	COIL 15MHz	731-203
L 3	Choke HF Mini 2u2 10% 1A 0. 25ohm	703-011

TRANSISTORS

Q 1	Transistor 2N3904 pnp	360-064
Q 2	Transistor BC327-25 SI PNP 45V 1A 800mW TO-92	360-224

INTEGRATED DIGITAL CIRCUITS

QD 1	IC TMS9995NL CPU	364-496
QD 2	IC 74LS244 oct buffer	364-321
QD 3	IC 74LS244 oct buffer	364-321
QD 4	IC 74LS244 oct buffer	364-321
QD 5	IC SN74LS245 Octal bus transceiver	364-332
QD 6	IC SN74LS138N 1-of-8 decoder/demultiplexer	364-308
QD 7	IC 74HCT00 quad NAND gate	364-684
QD 8	IC SN74LS156N Dual 2-line to 4-line decoder	364-349
QD 9	IC 74HCT11 triple 3-input and gate	364-683
QD 10	IC 74LS74 dual D ff	364-185
QD 11	IC 74LS74 dual D ff	364-185
QD 12	IC 74LS74 dual D ff	364-185
QD 13	IC SN74LS259 8-bit adressable latch	364-397
QD 14	IC TMS9902ANL	364-516
QD 15	IC 74LS00 quad NAND gate	364-213
QD 16	IC 74LS00 quad NAND gate	364-213
QD 17	IC 74HCT132 P nand schmit	364-697
QD 18	RE201 901-788 QD18	369-307
QD 19	IC SN74LS03 Quad 2-input Nand gate open collector	364-329
QD 20	IC 74LS32 quad OR gate	364-301
QD 21	IC 74LS32 quad OR gate	364-301
QD 22	IC 74LS04 hex inverters	364-219
QD 23	IC 74LS04 hex inverters	364-219
QD 24	IC 74S260 dual NOR gate	364-498
QD 25	IC 74LS30 8-input nand gate	364-384
QD 26	IC HEF40244 Octal buffer with 3-state	364-497
QD 27	IC HEF40244 Octal buffer with 3-state	364-497
QD 28	IC SN74LS259 8-bit adressable latch	364-397

QD 29	IC HEF4724BP 8-bit adessable latch	364-412
QD 30	IC HEF4512BP 8-input multiplexer	364-279
QD 31	IC SN74LS138N 1-of-8 decoder/demultiplexer	364-308
QD 32	IC HEF4068P 8-input Nand gate	364-236
QD 33	IC 74LS74 dual D ff	364-185
QD 34	RE201 901-788 QD34 VER 1.0	368-337
QD 35	RE201 901-788 QD35 VER 1.0	368-338
QD 36	IC TC5565PL-15 8KX8 CMOS RAM	364-612
QD 37	IC TC5565PL-15 8KX8 CMOS RAM	364-612

RESISTORS

R 1	R thick film Sil 8x10K	146-003
R 2	R trick film Sil 8x18K	146-008
R 3	R trick film Sil 8x18K	146-008
R 4	R trick film Sil 8x18K	146-008
R 5	R thick film Sil 8x47K	146-005
R 6	R thick film Sil 8x47K	146-005
R 7	R trick film Sil 8x390E	146-009
R 8	R thick film Sil 8x10K	146-003
R 10	R Metal film 1K00 5% 0.2W TC250	107-410
R 11	R Metal film 390E 5% 0.2W TC250	107-339
R 12	R Metal film 4K70 5% 0.2W TC250	107-447
R 13	R Metal film 1K00 5% 0.2W TC250	107-410
R 14	R Metal film 18K0 5% 0.2W TC250	107-518
R 15	R Metal film 150E 5% 0.2W TC250	107-315
R 16	R Metal film 3K30 5% 0.2W TC250	107-433
R 17	R Metal film 470E 5% 0.2W TC250	107-347
R 20	R Metal film 10K0 5% 0.2W TC250	107-510
R 21	R Metal film 1K00 5% 0.2W TC250	107-410
R 22	R Metal film 1K00 5% 0.2W TC250	107-410
R 23	R Metal film 270E 5% 0.2W TC250	107-327

TESTPOINTS

TP 1	4 Pin Connector Male mod II W. Lock	805-901
TP 2	4 Pin Connector Male mod II W. Lock	805-901

CRYSTALS

Y 1	Crystal 12MHZ	910-144

MISCELLANEOUS

tubular rivet 02.5x0.25x7	060-270
Female Plug	805-718
16 Pin Dil Socket	816-133
40 pin DIL Socket	816-179
18 Pin DIL Socket	816-183
20 Pin DIL Socket	816-184
16 Pin Programmable Plug	816-187
28 Pin DIL Socket	816-251
Solder Terminal 0.1 O2	823-303
Board Extractor	857-017

Conducter Rail C1	931-036
PCB RE201 Static CPU Ver.2	971-350

Main CPU (901-789)

CAPACITORS

C 1	C solid AL 33u 20% 10V	265-005
C 2	C solid AL 33u 20% 10V	265-005
C 3	C solid AL 33u 20% 10V	265-005
C 4	C solid AL 33u 20% 10V	265-005
C 5	C solid AL 33u 20% 10V	265-005
C 6	C solid AL 33u 20% 10V	265-005
C 7	C solid AL 33u 20% 10V	265-005
C 8	C solid AL 33u 20% 10V	265-005
C 9	C Ceramic 12p0 p25 100V NPO	213-227
C 10	C Ceramic 12p0 p25 100V NPO	213-227
C 11	C Ceramic 100n 20% 50V	213-400
C 12	C Ceramic 100n 20% 50V	213-400
C 13	C Ceramic 100n 20% 50V	213-400
C 14	C Ceramic 100n 20% 50V	213-400
C 15	C Ceramic 100n 20% 50V	213-400
C 16	C Ceramic 100n 20% 50V	213-400
C 17	C Ceramic 100n 20% 50V	213-400
C 18	C Ceramic 100n 20% 50V	213-400
C 19	C Ceramic 100n 20% 50V	213-400
C 20	C Ceramic 100n 20% 50V	213-400
C 21	C Ceramic 100n 20% 50V	213-400
C 22	C Ceramic 100n 20% 50V	213-400
C 23	C Ceramic 100n 20% 50V	213-400
C 24	C Ceramic 100n 20% 50V	213-400
C 25	C Ceramic 100n 20% 50V	213-400
C 26	C Ceramic 100n 20% 50V	213-400
C 27	C Ceramic 100n 20% 50V	213-400
C 28	C Ceramic 100n 20% 50V	213-400
C 29	C Ceramic 100n 20% 50V	213-400
C 30	C Ceramic 100n 20% 50V	213-400
C 31	C Ceramic 100n 20% 50V	213-400
C 32	C Ceramic 100n 20% 50V	213-400
C 33	C Ceramic 100n 20% 50V	213-400

DIODES

CR 1	Diode BAV10 Si Vr-60V If-600mA	350-022
CR 2	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 3	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 4	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 5	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 6	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 7	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 8	Diode Right Angle Led-Indicator HP-HLMP5000	350-803
CR 9	Diode Right Angle Led-Indicator HP-HLMP5000	350-803

CONNECTORS

J 2	DIN 41651 header f. pcb 26 pol	805-961

RELAYS & JUMPERS

JP 4	2-pol amp connector	805-951

CHOKES

L 1	COIL 15MHz	731-203
L 2	COIL 15MHz	731-203

TRANSISTORS

Q 1	Transistor VP0106N3 Power Mos P-CH	360-244
Q 2	Transistor VN0106N3 Power Mos N-CH	360-245

INTEGRATED DIGITAL CIRCUITS

QD 1	IC TMS9995NL CPU	364-496
QD 2	IC TMS9914ANL P-VER.Gen.Pur Interface bus	364-454
QD 3	IC 82C59 Interrupt controller	364-710
QD 4	RE201 901-422 QD4 Eprom 27C256-150	368-341
QD 5	RE201 901-422 QD5 Eprom 27C256-150	368-342
QD 8	IC 55257/51256 CMOS RAM 32KX8	364-759
QD 9	RE201 901-422 QD9 Pal 16L8	369-309
QD 10	RE201 901-422 QD10 PAL 12L6	369-310
QD 11	RE201 901-422 QD11 Pal 16L8	369-311
QD 12	IC TC5565PL-15 8KX8 CMOS RAM	364-612
QD 13	RE201 901-422 QD13 Eprom 2764-3	368-343
QD 14	IC 68A45 CRT Controller	364-723
QD 15	IC SN75160A Octal IEEE-488 TR	364-576
QD 16	IC SN75161N Octal bus transceivers	364-455
QD 17	IC SN74ALS08 Quad 2-Input AND Gate	364-719
QD 18	IC SN74ALS32 Quad 2-Input OR Gate	364-720
QD 19	IC SN74ALS32 Quad 2-Input OR Gate	364-720
QD 20	IC SN74ALS74 Dual D-Type Flip-Flop	364-722
QD 21	IC SN74ALS245A Octal Bus Transceiver (3-State)	364-721
QD 22	IC 74ALS163 Synchron 4-Bit Counter	364-717
QD 23	IC SN74HCT259 8-bit Addressable Latch	364-715
QD 24	IC SN74HCT259 8-bit Addressable Latch	364-715
QD 25	IC 74HCT245 oct bus tx/rx	364-667
QD 26	IC 74HCT245 oct bus tx/rx	364-667
QD 27	IC 74HCT646 Octal Bus Transciver/Register 3-state	364-742
QD 28	IC 74HCT646 Octal Bus Transciver/Register 3-state	364-742
QD 31	IC 74HCT574P octal d ff	364-716
QD 32	IC 74HCT574P octal d ff	364-716
QD 33	IC 74HCT245 oct bus tx/rx	364-667
QD 34	IC 74HCT245 oct bus tx/rx	364-667
QD 35	IC 74HCT245 oct bus tx/rx	364-667
QD 36	IC 74HCT157 quad 2-input	364-713
QD 37	IC CD74HCT138 3-to-8 line dec.	364-570
QD 38	IC SN74HCT139 Dual 2-to-4 Line Decod./Demultiplex.	364-712

QD 39	IC 74HCT166 8bit shift re	364-714
QD 40	IC 74HCT166 8bit shift re	364-714
QD 41	IC 74HCT157 quad 2-input	364-713
QD 42	IC 74HCT74 dual D ff	364-686
QD 43	IC 74HCT74 dual D ff	364-686
QD 44	IC 74HCT74 dual D ff	364-686
QD 45	IC 74HCT74 dual D ff	364-686
QD 46	IC 74HCT74 dual D ff	364-686
QD 47	IC 74HCT74 dual D ff	364-686
QD 48	IC 74HCT74 dual D ff	364-686
QD 49	IC 74HCT08 quad AND gate	364-711
QD 50	IC 74HCT08 quad AND gate	364-711
QD 51	IC 74HCT04 HEX inv	364-700
QD 52	IC 74HCT04 HEX inv	364-700
QD 53	IC 74HCT04 HEX inv	364-700
QD 54	IC 74HCT00 quad NAND gate	364-684
QD 56	IC 74HCT132 P nand schmit	364-697
QD 57	IC 74LS125 quad buffer	364-575
QD 58	IC 74LS125 quad buffer	364-575
QD 59	IC 4078 8-input NOR gate	364-268

RESISTORS

R 1	R trick film Sil 8x18K	146-008
R 2	R trick film Sil 8x18K	146-008
R 3	R trick film Sil 8x18K	146-008
R 4	R Metal film 18K0 5% 0.2W TC250	107-518
R 5	R Metal film 18K0 5% 0.2W TC250	107-518
R 6	R trick film Sil 8x390E	146-009
R 7	R Metal film 100E 5% 0.2W TC250	107-310
R 8	R trick film Sil 8x18K	146-008
R 9	R Metal film 18K0 5% 0.2W TC250	107-518
R 10	R Metal film 18K0 5% 0.2W TC250	107-518
R 11	R Metal film 18K0 5% 0.2W TC250	107-518
R 12	R Metal film 18K0 5% 0.2W TC250	107-518
R 13	R Metal film 18K0 5% 0.2W TC250	107-518
R 14	R Metal film 18K0 5% 0.2W TC250	107-518
R 15	R Metal film 18K0 5% 0.2W TC250	107-518
R 16	R Metal film 18K0 5% 0.2W TC250	107-518
R 17	R Metal film 10K0 5% 0.2W TC250	107-510
R 18	R Metal film 1K00 5% 0.2W TC250	107-410

CRYSTALS

Y 1	QUARTZ CRYSTAL 10MHz +-50ppm	910-198

MISCELLANEOUS

	tubular rivet 02.5x0.25x7	060-270
	40 pin DIL Socket	816-179
	20 Pin DIL Socket	816-184
	28 Pin DIL Socket	816-251
	Solder Terminal 0.1 O2	823-303
	Board Extractor	857-017

Conducter Rail C1	931-036
PCB RE201 Main CPU Ver.2	971-352

Digital Motherboard (901-790)

CAPACITORS

C 1	C Tantal 68u 20% 16V	267-015
C 2	C Ceramic 100n 20% 50V	213-400
C 3	C Ceramic 100n 20% 50V	213-400
C 4	C Ceramic 100n 20% 50V	213-400
C 5	C Ceramic 100n 20% 50V	213-400
C 6	C Ceramic 100n 20% 50V	213-400
C 7	C Ceramic 100n 20% 50V	213-400
C 8	C electrolytic 10u0 25V	261-081
C 13	C electrolytic 10u0 25V	261-081
C 14	C electrolytic 10u0 25V	261-081
C 19	C electrolytic 10u0 25V	261-081
C 20	C Ceramic 100n 20% 50V	213-400
C 21	C Ceramic 100n 20% 50V	213-400
C 22	C Ceramic 100n 20% 50V	213-400
C 23	C Ceramic 100n 20% 50V	213-400
C 24	C Ceramic 100n 20% 50V	213-400
C 25	C Ceramic 100n 20% 50V	213-400
C 26	C Ceramic 100n 20% 50V	213-400

DIODES

CR 1	Diode BAV20 Si Vr-150V If-250mA	350-023
CR 2	Diode BAV20 Si Vr-150V If-250mA	350-023
CR 3	Diode zener BZX79-C12V 0.4W	350-605
CR 4	Diode zener BZX79-C12V 0.4W	350-605

CONNECTORS

J 1	Terminal strip 8-pol vinkel MOD II	805-851
J 2	6 Pin AMP mod II Terminal List, Angled	805-914
J 3	9 Pin AMP mod II Terminal List, Straight	805-903
J 4	14 Pin Dil Socket	816-131
J 5	4 Pin AMP mod. I Terminal List, Straight	805-917
J 6	5 Pin Connector Male mod II W. Lock	805-895
J 7	Bus Connector	805-790
J 9	Bus Connector	805-790
J 11	Bus Connector	805-790
J 13	Bus Connector	805-790
J 16	3 Pin AMP mod II Terminal List, Straight	805-894

RELAYS & JUMPERS

K 1	Wire Wrap Terminal	805-727
K 2	Wire Wrap Terminal	805-727
K 3	Wire Wrap Terminal	805-727

CHOKES

L 1	Choke HF Mini 6u8H 10%	703-035

TRANSISTORS

Q 1	Transistor HCPL2730 Dual Optocoupler	360-219

INTEGRATED DIGITAL CIRCUITS

QD 1	IC TMS9902ANL	364-516
QD 2	IC SN74LS139N Dual 1 of-4 decoder/demultiplexer	364-376
QD 3	IC 74LS04 hex inverters	364-219
QD 4	IC TMS9902ANL	364-516
QD 5	IC SN74LS138N 1-of-8 decoder/demultiplexer	364-308
QD 6	IC HEF4724BP 8-bit adessable latch	364-412
QD 7	IC 74LS74 dual D ff	364-185
QD 8	IC 74LS174 hex D ff	364-271
QD 9	IC 74LS174 hex D ff	364-271
QD 10	IC 75188 quad line driver	364-502
QD 11	IC SN74LS05N HEX inverters (open collector)	364-214

RESISTORS

R 1	R trick film Sil 8x1K	146-010
R 2	R Metal film 1K00 5% 0.2W TC250	107-410
R 3	R Metal film 1K00 5% 0.2W TC250	107-410
R 4	R Metal film 1K20 5% 0.2W TC250	107-412
R 5	R Metal film 1K20 5% 0.2W TC250	107-412
R 6	R Metal film 3K30 5% 0.2W TC250	107-433
R 8	R thick film Sil 8x10K	146-003
R 9	R thick film Sil 8x10K	146-003
R 10	R thick film Sil 8x10K	146-003
R 11	R thick film Sil 8x10K	146-003
R 12	R thick film Sil 8x10K	146-003
R 13	R thick film Sil 8x10K	146-003
R 14	R thick film Sil 8x10K	146-003
R 15	R thick film Sil 8x10K	146-003
R 16	R Metal film 47K0 5% 0.2W TC250	107-547
R 17	R Metal film 47K0 5% 0.2W TC250	107-547
R 18	R Metal film 47K0 5% 0.2W TC250	107-547
R 19	R Carbon 83E 5% 0.2W	106-282
R 20	R Carbon 83E 5% 0.2W	106-282

MISCELLANEOUS

***** Unknown text *****	
Tubular Rivet 2.5X10	060-310
Spacer 3.5/6-1.5	065-672
Polarizing Key for EMZ Conn.	805-306
Female Plug	805-718
8 Pin Dil Socket	816-132
18 Pin DIL Socket	816-183
PCB RE201 Digatal Motherboard Ver.2	971-351

Mains Input and Power Supply Filters (985-211)

FANS

B 1	Fan Toyo 115 V	580-154
B 2	Fan Toyo 115 V	580-154

CAPACITORS

C 1	C Ceramic 1n -20%+50%	215-500
C 2	C Ceramic 1n -20%+50%	215-500
C 3	MKT, 0.1/100/10, R:4*9*13, RM4	241-025
C 4	MKT, 0.1/100/10, R:4*9*13, RM4	241-025
C 5	C Tantal 68u 20% 16V	267-015
C 6	C Ceramic u1 -20%+80% 12V	213-017

CHOKES

L 1	Choke HF Coil 6uH 3A	703-043

SWITCHES

S 1	Main Switch, 2 pole	500-202
S 2	Slide Switch Line CSA	500-111

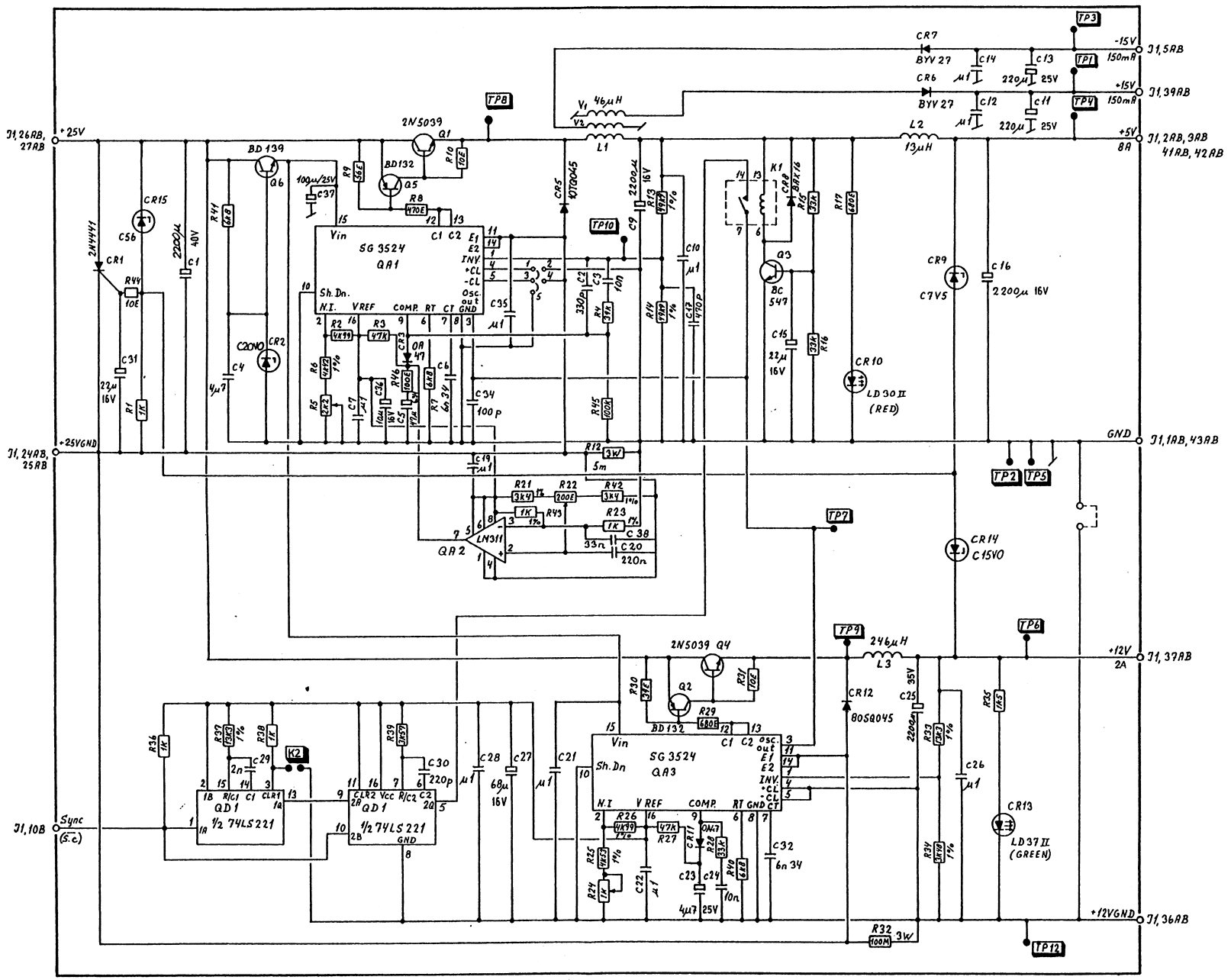
MISCELLANEOUS

T1 *	Transformer	770-696

PI-Filters (985-217)

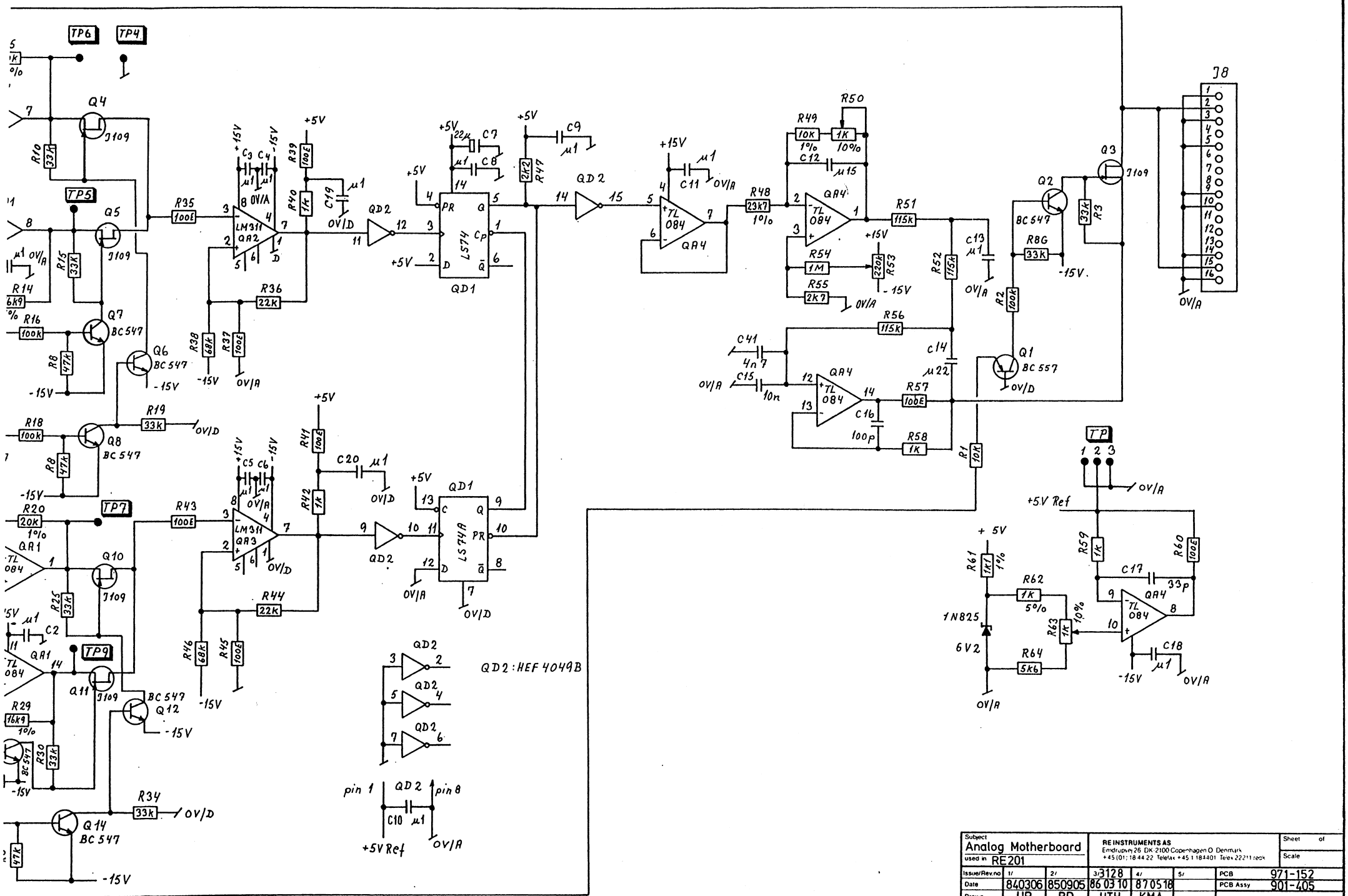
FILTERS

FL 1	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 2	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 3	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 4	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 5	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 6	C Pi-Filter Ceramic 2x100p 250V	216-004
FL 7	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 8	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 9	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 10	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 11	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 12	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 13	C Pi-Filter Ceramic 2x1n5 250V	216-001
FL 14	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 15	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 16	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 17	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 18	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 19	C Pi-Filter Ceramic 2x1n5 250V	216-001
FL 20	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 21	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 22	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 23	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 24	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 25	Pi-filter, 2 x 1.5 nF 250 V	910-032
FL 26	Pi-filter, 2 x 1.5 nF 250 V	910-032



Subject: SMPS used in RE201			RE INSTRUMENTS AS Emdrupvej 26 DK-2100 Copenhagen O Denmark +45 (01) 18 44 22 Telefax +45 1 184401 Telex 22211 redk			Sheet of	
						Scale :	
Issue/Rev.no	1/	2/	3/	4/	5/	PCB	970-921
Date	840306	850709	850904			PCB Assy	901-022
Drawn	UP	TD	BD			Schematic Drawing	985-107
App.			NE				

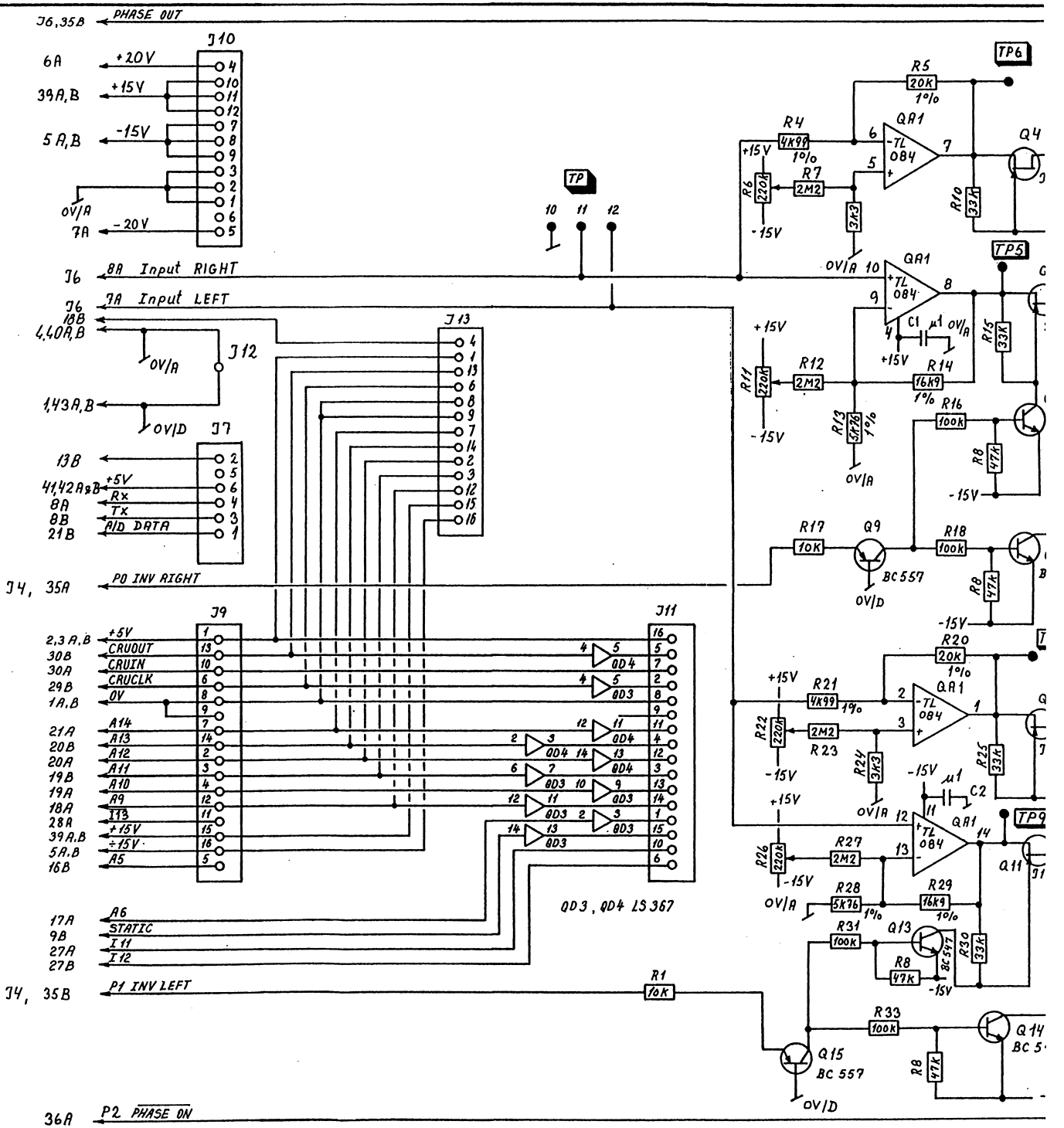
RE•INSTRUMENTS AS
901-022
ISS.8
S8
GND
TP1
K1
K2
L1
L2
L3
Q1
Q2
Q3
Q4
Q5
Q6
CR5
CR10
CR13
CR12
CR2
CR3
CR4
CR6
CR7
CR8
CR9
CR11
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
C35
C36
C37
C38
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
R45
R46
A1
A2
A3
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
D32
D33
D34
D35
D36
D37
D38
D39
D40
D41
D42
D43
D44
D45
D46
D47
D48
D49
D50
D51
D52
D53
D54
D55
D56
D57
D58
D59
D60
D61
D62
D63
D64
D65
D66
D67
D68
D69
D70
D71
D72
D73
D74
D75
D76
D77
D78
D79
D80
D81
D82
D83
D84
D85
D86
D87
D88
D89
D90
D91
D92
D93
D94
D95
D96
D97
D98
D99
D100
D101
D102
D103
D104
D105
D106
D107
D108
D109
D110
D111
D112
D113
D114
D115
D116
D117
D118
D119
D120
D121
D122
D123
D124
D125
D126
D127
D128
D129
D130
D131
D132
D133
D134
D135
D136
D137
D138
D139
D140
D141
D142
D143
D144
D145
D146
D147
D148
D149
D150
D151
D152
D153
D154
D155
D156
D157
D158
D159
D160
D161
D162
D163
D164
D165
D166
D167
D168
D169
D170
D171
D172
D173
D174
D175
D176
D177
D178
D179
D180
D181
D182
D183
D184
D185
D186
D187
D188
D189
D190
D191
D192
D193
D194
D195
D196
D197
D198
D199
D200
D201
D202
D203
D204
D205
D206
D207
D208
D209
D210
D211
D212
D213
D214
D215
D216
D217
D218
D219
D220
D221
D222
D223
D224
D225
D226
D227
D228
D229
D230
D231
D232
D233
D234
D235
D236
D237
D238
D239
D240
D241
D242
D243
D244
D245
D246
D247
D248
D249
D250
D251
D252
D253
D254
D255
D256
D257
D258
D259
D260
D261
D262
D263
D264
D265
D266
D267
D268
D269
D270
D271
D272
D273
D274
D275
D276
D277
D278
D279
D280
D281
D282
D283
D284
D285
D286
D287
D288
D289
D290
D291
D292
D293
D294
D295
D296
D297
D298
D299
D300
D301
D302
D303
D304
D305
D306
D307
D308
D309
D310
D311
D312
D313
D314
D315
D316
D317
D318
D319
D320
D321
D322
D323
D324
D325
D326
D327
D328
D329
D330
D331
D332
D333
D334
D335
D336
D337
D338
D339
D340
D341
D342
D343
D344
D345
D346
D347
D348
D349
D350
D351
D352
D353
D354
D355
D356
D357
D358
D359
D360
D361
D362
D363
D364
D365
D366
D367
D368
D369
D370
D371
D372
D373
D374
D375
D376
D377
D378
D379
D380
D381
D382
D383
D384
D385
D386
D387
D388
D389
D390
D391
D392
D393
D394
D395
D396
D397
D398
D399
D400
D401
D402
D403
D404
D405
D406
D407
D408
D409
D410
D411
D412
D413
D414
D415
D416
D417
D418
D419
D420
D421
D422
D423
D424
D425
D426
D427
D428
D429
D430
D431
D432
D433
D434
D435
D436
D437
D438
D439
D440
D441
D442
D443
D444
D445
D446
D447
D448
D449
D450
D451
D452
D453
D454
D455
D456
D457
D458
D459
D460
D461
D462
D463
D464
D465
D466
D467
D468
D469
D470
D471
D472
D473
D474
D475
D476
D477
D478
D479
D480
D481
D482
D483
D484
D485
D486
D487
D488
D489
D490
D491
D492
D493
D494
D495
D496
D497
D498
D499
D500
D501
D502
D503
D504
D505
D506
D507
D508
D509
D510
D511
D512
D513
D514
D515
D516
D517
D518
D519
D520
D521
D522
D523
D524
D525
D526
D527
D528
D529
D530
D531
D532
D533
D534
D535
D536
D537
D538
D539
D540
D541
D542
D543
D544
D545
D546
D547
D548
D549
D550
D551
D552
D553
D554
D555
D556
D557
D558
D559
D560
D561
D562
D563
D564
D565
D566
D567
D568
D569
D570
D571
D572
D573
D574
D575
D576
D577
D578
D579
D580
D581
D582
D583
D584
D585
D586
D587
D588
D589
D590
D591
D592
D593
D594
D595
D596
D597
D598
D599
D600
D601
D602
D603
D604
D605
D606
D607
D608
D609
D610
D611
D612
D613
D614
D615
D616
D617
D618
D619
D620
D621
D622
D623
D624
D625
D626
D627
D628
D629
D630
D631
D632
D633
D634
D635
D636
D637
D638
D639
D640
D641
D642
D643
D644
D645
D646
D647
D648
D649
D650
D651
D652
D653
D654
D655
D656
D657
D658
D659
D660
D661
D662
D663
D664
D665
D666
D667
D668
D669
D670
D671
D672
D673
D674
D675
D676
D677
D678
D679
D680
D681
D682
D683
D684
D685
D686
D687
D688
D689
D690
D691
D692
D693
D694
D695
D696
D697
D698
D699
D700
D701
D702
D703
D704
D705
D706
D707
D708
D709
D710
D711
D712
D713
D714
D715
D716
D717
D718
D719
D720
D721
D722
D723
D724
D725
D726
D727
D728
D729
D730
D731
D732
D733
D734
D735
D736
D737
D738
D739
D740
D741
D742
D743
D744
D745
D746
D747
D748
D749
D750
D751
D752
D753
D754
D755
D756
D757
D758
D759
D760
D761
D762
D763
D764
D765
D766
D767
D768
D769
D770
D771
D772
D773
D774
D775
D776
D777
D778
D779
D780
D781
D782
D783
D784
D785
D786
D787
D788
D789
D790
D791
D792
D793
D794
D795
D796
D797
D798
D799
D800
D801
D802
D803
D804
D805
D806
D807
D808
D809
D810
D811
D812
D813
D814
D815
D816
D817
D818
D819
D820
D821
D822
D823
D824
D825
D826
D827
D828
D829
D830
D831
D832
D833
D834
D835
D836
D837
D838
D839
D840
D841
D842
D843
D844
D845
D846
D847
D848
D849
D850
D851
D852
D853
D854
D855
D856
D857
D858
D859
D860
D861
D862
D863
D864
D865
D866
D867
D868
D869
D870
D871
D872
D873
D874
D875
D876
D877
D878
D879
D880
D881
D882
D883
D884
D885
D886
D887
D888
D889
D890
D891
D892
D893
D894
D895
D896
D897
D898
D899
D900
D901
D902
D903
D904
D905
D906
D907
D908
D909
D910
D911
D912
D913
D914
D915
D916
D917
D918
D919
D920
D921
D922
D923
D924
D925
D926
D927
D928
D929
D930
D931
D932
D933
D934
D935
D936
D937
D938
D939
D940
D941
D942
D943
D944
D945
D946
D947
D948
D949
D950
D951
D952
D953
D954
D955
D956
D957
D958
D959
D960
D961
D962
D963
D964
D965
D966
D967
D968
D969
D970
D971
D972
D973
D974
D975
D976
D977
D978
D979
D980
D981
D982
D983
D984
D985
D986
D987
D988
D989
D990
D991
D992
D993
D994
D995
D996
D997
D998
D999
D1000



Subject: Analog Motherboard used in RE201			RE INSTRUMENTS AS Emdrupvej 26 DK-2100 Copenhagen O Denmark +45 (01) 18 44 22 Telefax +45 1 184401 Telex 22211 reck				Sheet of
Issue/Rev.no	1/	2/	3/3128	4/	5/	PCB	971-152
Date	840306	850905	860310	870518		PCB Assy	901-405
Drawn	UP	BD	UTH	KMA		Schematic Drawing	985-100
App.		NE	ME				

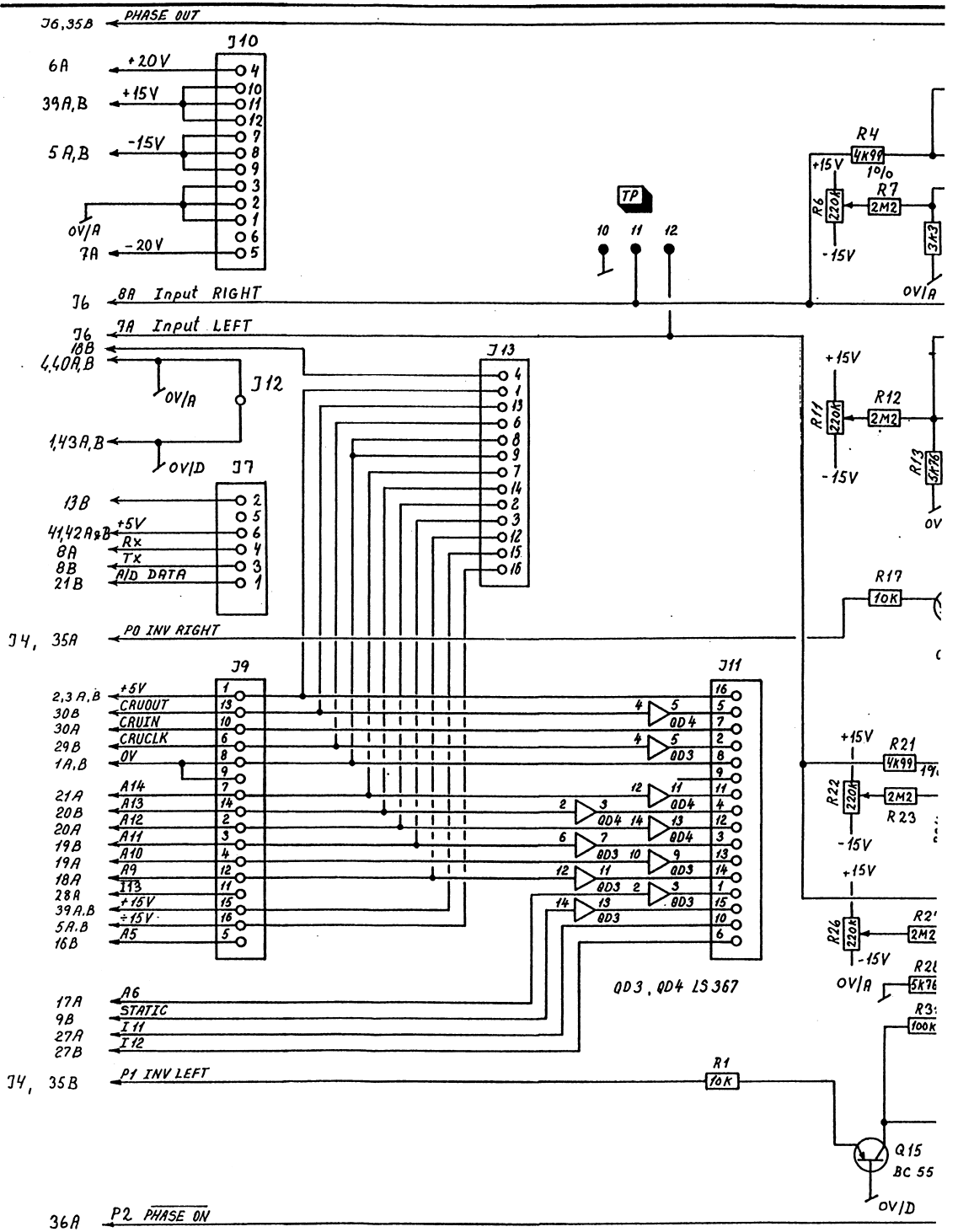
IT SIDE			B SOLDER SIDE			
		DESCRIPTION	PIN	MNEM		DESCRIPTION
		DIGITAL GROUND	1B	GND		DIGITAL GROUND
		+5VDC	2B	+5V		+5VDC
		+5VDC	3B	+5V		+5VDC
		ANALOG GROUND	4B	GNDA		ANALOG GROUND
		-15VDC	5B	-15V		-15VDC
	+	+20VDC	6B			
2)	+	-20VDC	7B	READY		READY
3)	*	SERIAL RECEIVER	8B	TX	*	SERIAL TRANSMIT
TOUT	+	SYSTEM RESET	9B	STATIC	*	
HOLDA	+		10B	SC		START CONVERSION
	+		11B	CLKOUT	*	
	+		12B	MEMEN	+	MEMORY ENABLE
	+		13B		*	
		MOST SIGN ADR BIT	14B	A1		
			15B	A3		
			16B	A5		
			17B	A7		
		NB A8 OTHER SIDE	18B	A8		NB A9 OTHER SIDE
			19B	A11		
			20B	A13		
			21B	A15&CRUOUT	+	1)
	*	RESET IN	22B	I2	*	
	*	INT1	23B	I4	*	INT4&EC
	*		24B	I6	*	
	*		25B	I8	*	
	*		26B	I10	*	
	*	KEYBOARD	27B	I12	*	EXT. KEYBOARD
		W&F PRESENT	28B	I14	+	OPTION PRESENT
		OVERLOAD	29B	CRUCLK		
IN			30B	CRUOUT&A15		
	+	MOST SIGN D BIT	31B	D1	+	
	+		32B	D3	+	
	+		33B	D5	+	
	+		34B	D7	+	
	+	INV RIGHT	35B	P1	4) +	INV LEFT
	+	PHASE ON	36B	P3	+	
	*		37B	P5	+	
	*		38B	VBAT	+	BAT. BACK-UP
V		+15VDC	39B	+15V		+15VDC
A		ANALOG GROUND	40B	GNDA		ANALOG GROUND
		+5VDC	41B	+5V		+5VDC
		+5VDC	42B	+5V		+5VDC
		DIGITAL GROUND	43B	GND		DIGITAL GROUND

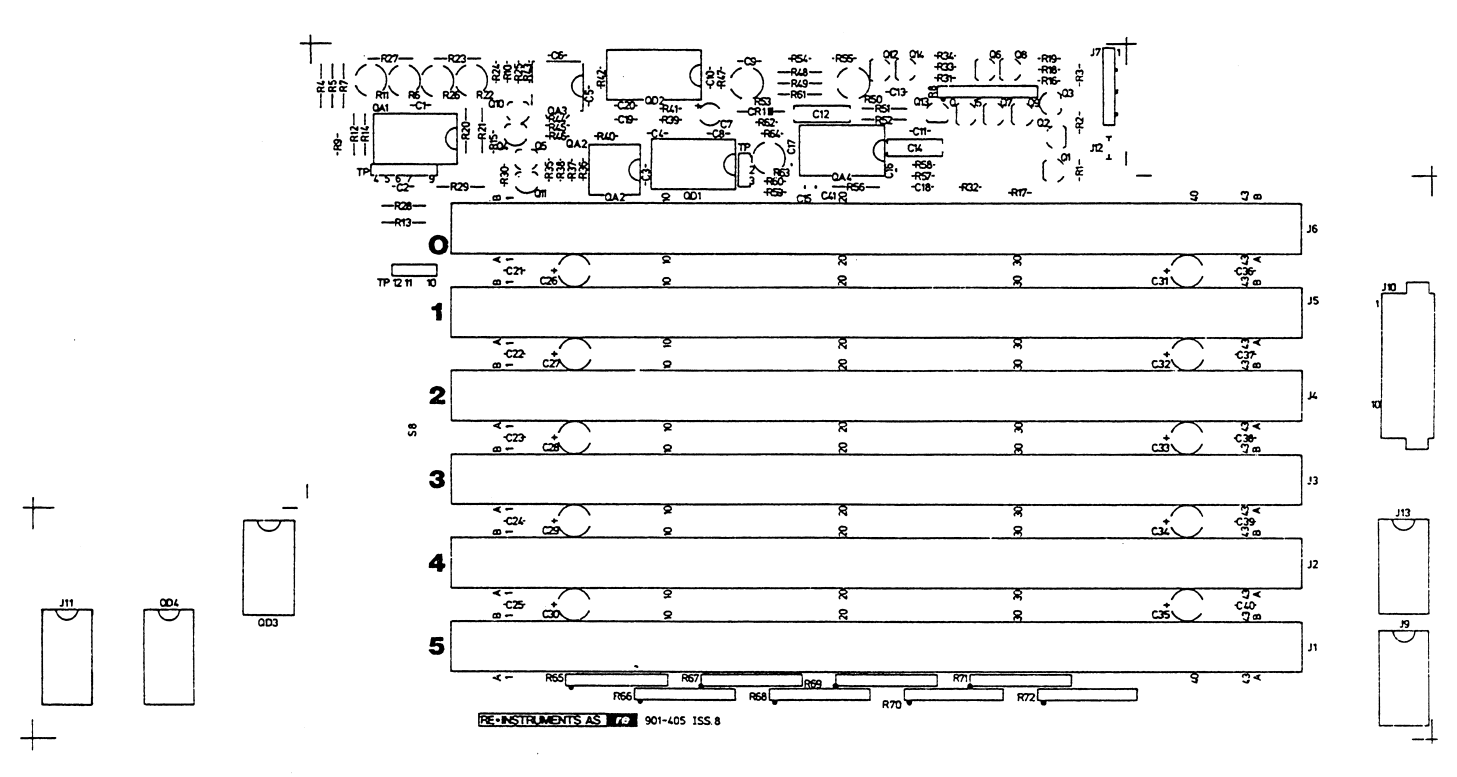
+ : NOT CONNECTED TO SLOT 0
* : NOT CONNECTED TO SLOTS 0 AND 1
1): SERIAL DATA FROM A/D CONVERTER IN SLOT 0
2): OUTPUT FROM LEFT CHANNEL TO PHASE DETECTOR IN SLOT 0
3): OUTPUT FROM RIGHT CHANNEL TO PHASE DETECTOR IN SLOT 0
4): OUTPUT FROM PHASE DETECTOR TO SLOT 0

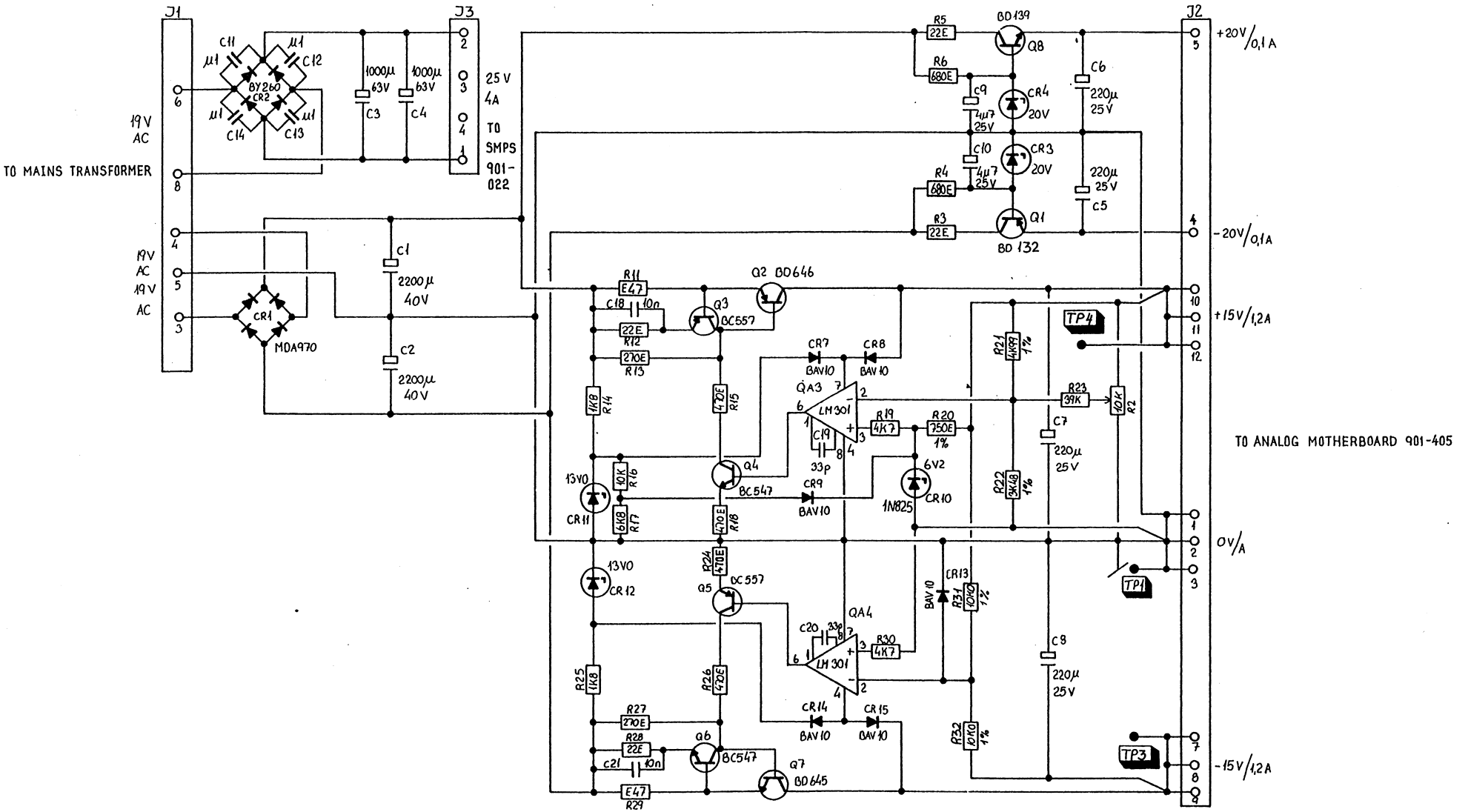


A COMPONENT SIDE				B SOLDER SIDE			
PIN	MNEM		DESCRIPTION	PIN	MNEM		DESCRIPTION
1A	GND		DIGITAL GROUND	1B	GND		DIGITAL GROUND
2A	+5V		+5VDC	2B	+5V		+5VDC
3A	+5V		+5VDC	3B	+5V		+5VDC
4A	GNDA		ANALOG GROUND	4B	GNDA		ANALOG GROUND
5A	-15V		-15VDC	5B	-15V		-15VDC
6A	+20V	+	+20VDC	6B			
7A	-20V 2)	+	-20VDC	7B	READY		READY
8A	RX 3)	*	SERIAL RECEIVER	8B	TX	*	SERIAL TRANSMIT
9A	RESETOUT	+	SYSTEM RESET	9B	STATIC	*	
10A	IAQ&HOLDA	+		10B	SC		START CONVERSION
11A	HOLD	+		11B	CLKOUT	*	
12A	WE	+		12B	MEMEN	+	MEMORY ENABLE
13A	DBIN	+		13B		*	
14A	A0		MOST SIGN ADR BIT	14B	A1		
15A	A2			15B	A3		
16A	A4			16B	A5		
17A	A6			17B	A7		
18A	A9		NB A8 OTHER SIDE	18B	A8		NB A9 OTHER SIDE
19A	A10			19B	A11		
20A	A12			20B	A13		
21A	A14			21B	A15&CRUOUT	+	1)
22A	I1	*	RESET IN	22B	I2	*	
23A	I3	*	INT1	23B	I4	*	INT4&EC
24A	I5	*		24B	I6	*	
25A	I7	*		25B	I8	*	
26A	I9	*		26B	I10	*	
27A	I11	*	KEYBOARD	27B	I12	*	EXT. KEYBOARD
28A	I13		W&F PRESENT	28B	I14	+	OPTION PRESENT
29A	I15		OVERLOAD	29B	CRUCLK		
30A	CRUIN			30B	CRUOUT&A15		
31A	D0	+	MOST SIGN D BIT	31B	D1	+	
32A	D2	+		32B	D3	+	
33A	D4	+		33B	D5	+	
34A	D6	+		34B	D7	+	
35A	P0	+	INV RIGHT	35B	P1 4)	+	INV LEFT
36A	P2	+	PHASE ON	36B	P3	+	
37A	P4	*		37B	P5	+	
38A	P6	*		38B	VBAT	+	BAT. BACK-UP
39A	+15V		+15VDC	39B	+15V		+15VDC
40A	GNDA		ANALOG GROUND	40B	GNDA		ANALOG GROUND
41A	+5V		+5VDC	41B	+5V		+5VDC
42A	+5V		+5VDC	42B	+5V		+5VDC
43A	GND		DIGITAL GROUND	43B	GND		DIGITAL GROUND

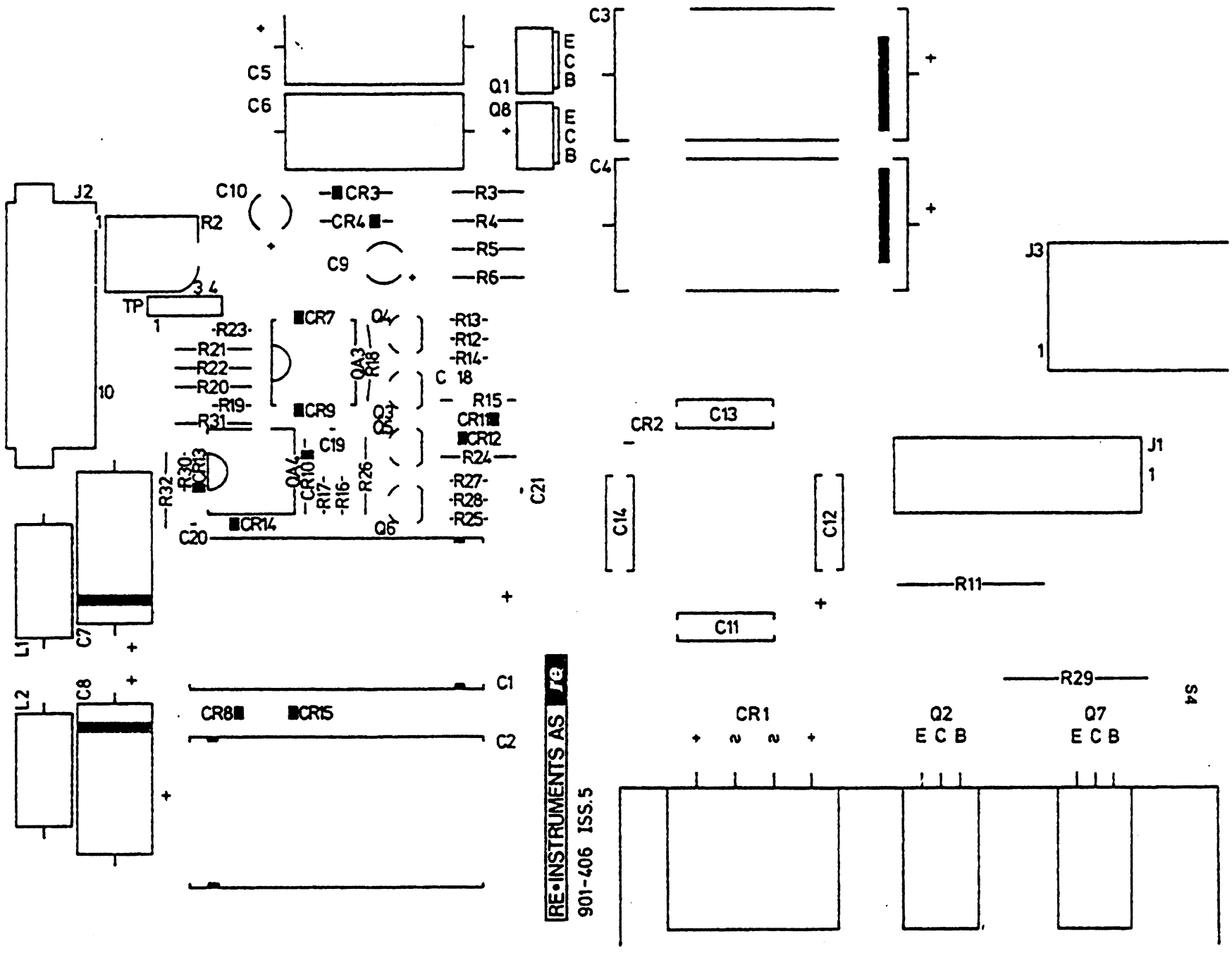
\+ : NOT CONNECTED TO SLOT 0
* : NOT CONNECTED TO SLOTS 0 AND 1
1): SERIAL DATA FROM A/D CONVERTER IN SLOT 0
2): OUTPUT FROM LEFT CHANNEL TO PHASE DETECTOR IN SLOT 0
3): OUTPUT FROM RIGHT CHANNEL TO PHASE DETECTOR IN SLOT 0
4): OUTPUT FROM PHASE DETECTOR TO SLOT 0

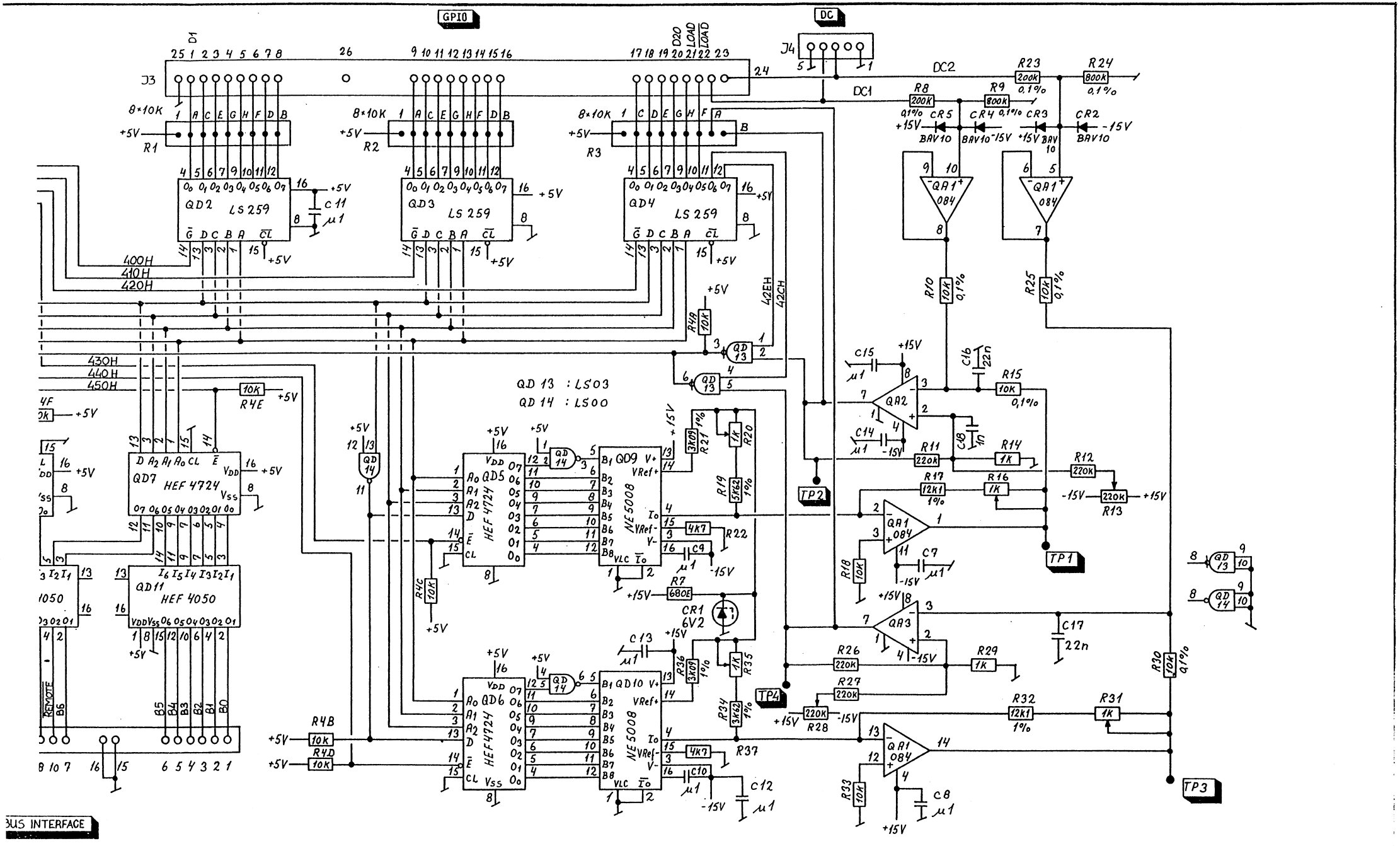



0
1
2
3
4
5
J6
J5
J4
J3
J2
J1
J10
J13
J9
J11
QD4
QD3
S8
TP
QA1
QA2
QD1
QD2
QA4
C12
C14
R65
R66
R67
R68
R69
R70
R71
R72
RE-INSTRUMENTS AS
901-405 ISS.8

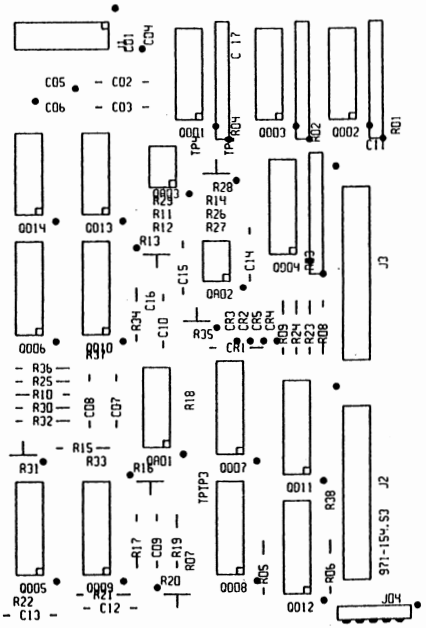


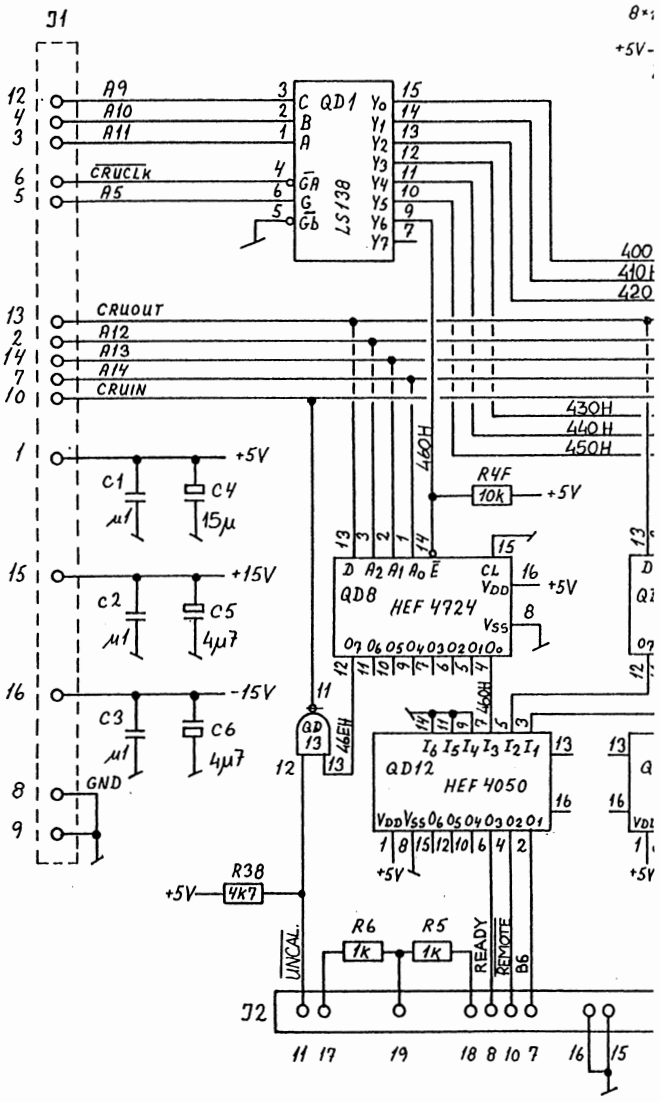
Subject: Linear Power Supply used in RE201			RE INSTRUMENTS AS Emdrupvej 26 DK 2100 Copenhagen O Denmark +45 (01) 18 44 22 Telefax +45 1 184401 Telex 22211 reds				Sheet of
Issue/Rev no	1/	2/	3/	4/	5/3017	PCB	971-153
Date	840306	850102	850710	850905	860206	PCB Assy	901-406
Drawn	UP	TD	TD	BD	UTH	Schematic Drawing	985-101
App.				NE	NE		

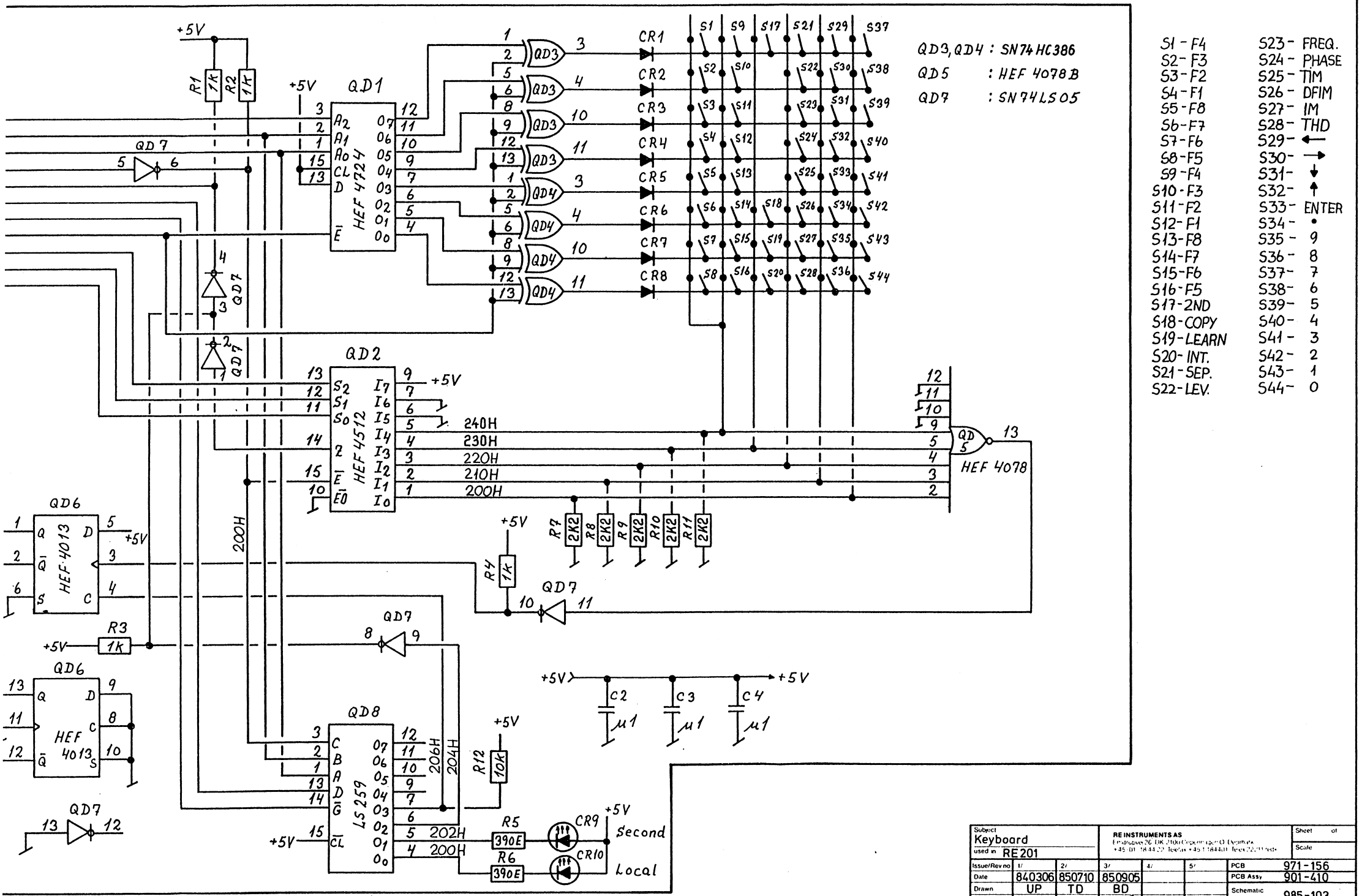

C5
C6
Q1
Q8
C3
C4
J2
C10
CR3
CR4
R2
R3
R4
R5
R6
C9
TP
J3
CR7
Q4
R23
R21
R22
R20
R19
R31
R13
R12
R14
C 18
R15
CR11
CR12
R24
CR9
C19
CR13
R30
R32
CR10
R17
R16
R26
R27
R28
R25
CR14
Q6
C20
C21
CR2
C13
J1
C14
C12
R11
C11
L1
C7
L2
C8
C1
C2
CR8
CR15
R29
CR1
Q2
E C B
Q7
E C B
S4
RE•INSTRUMENTS AS
901-406 ISS.5



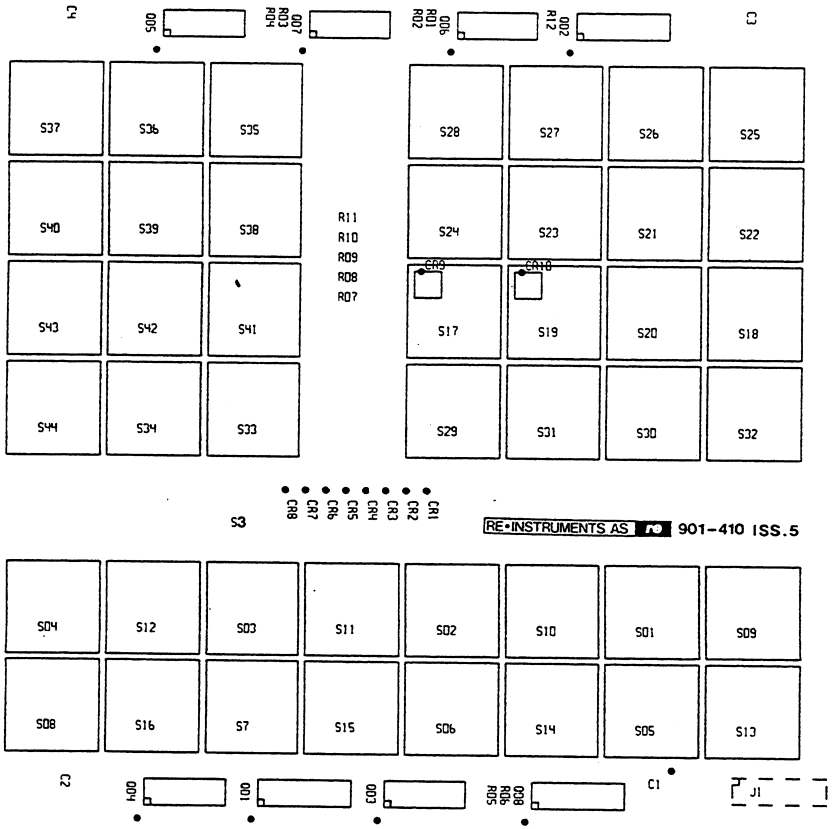
Subject: I/O & Mem.Bus Interface, used in RE201	RE INSTRUMENTS AS, Emdrupvej 26, DK-2100 Copenhagen O, Denmark, +45 (01) 18 44 22, Telefax +45 1 184401, Telex 22211 reins					Sheet of	
						Scale	
Issue/Rev.no	1/	2/	3/	4/	5/	PCB	971-154
Date	840306	850708	850905			PCB Assy	901-407
Drawn	UP	TD	BD			Schematic Drawing	985-102
App			NE				

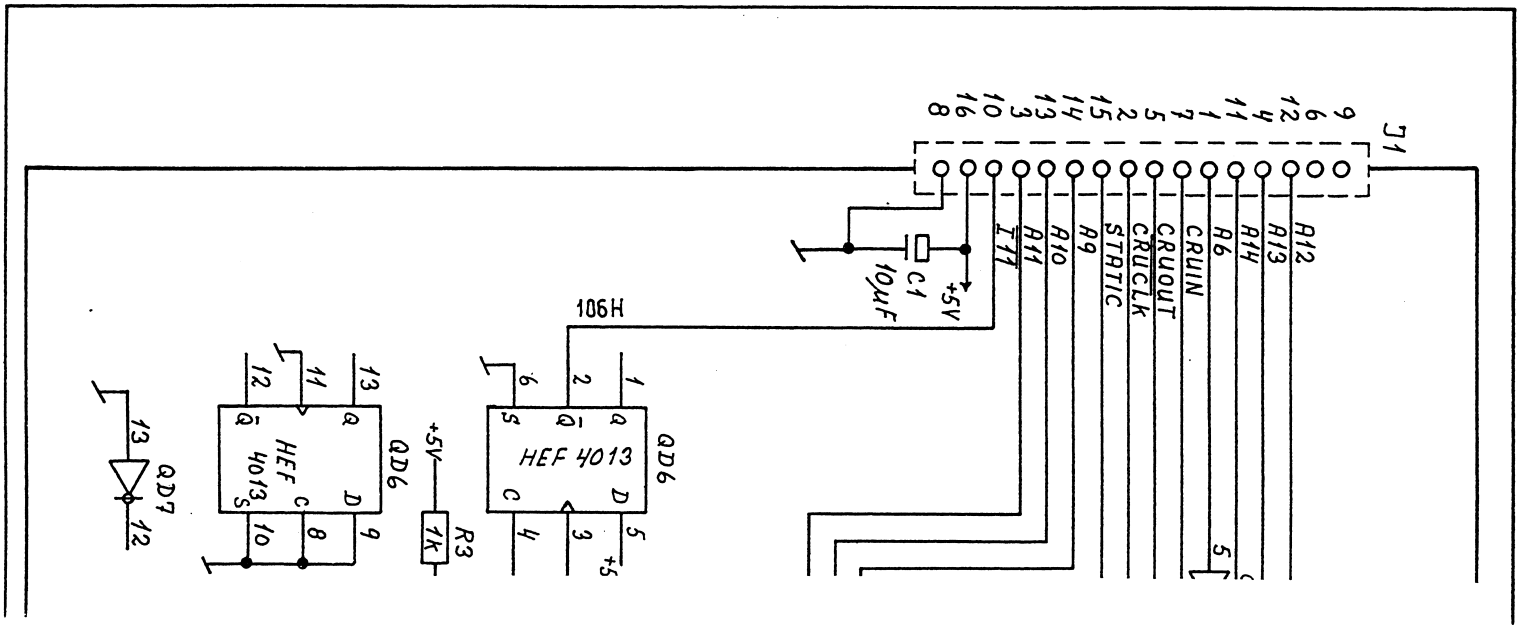


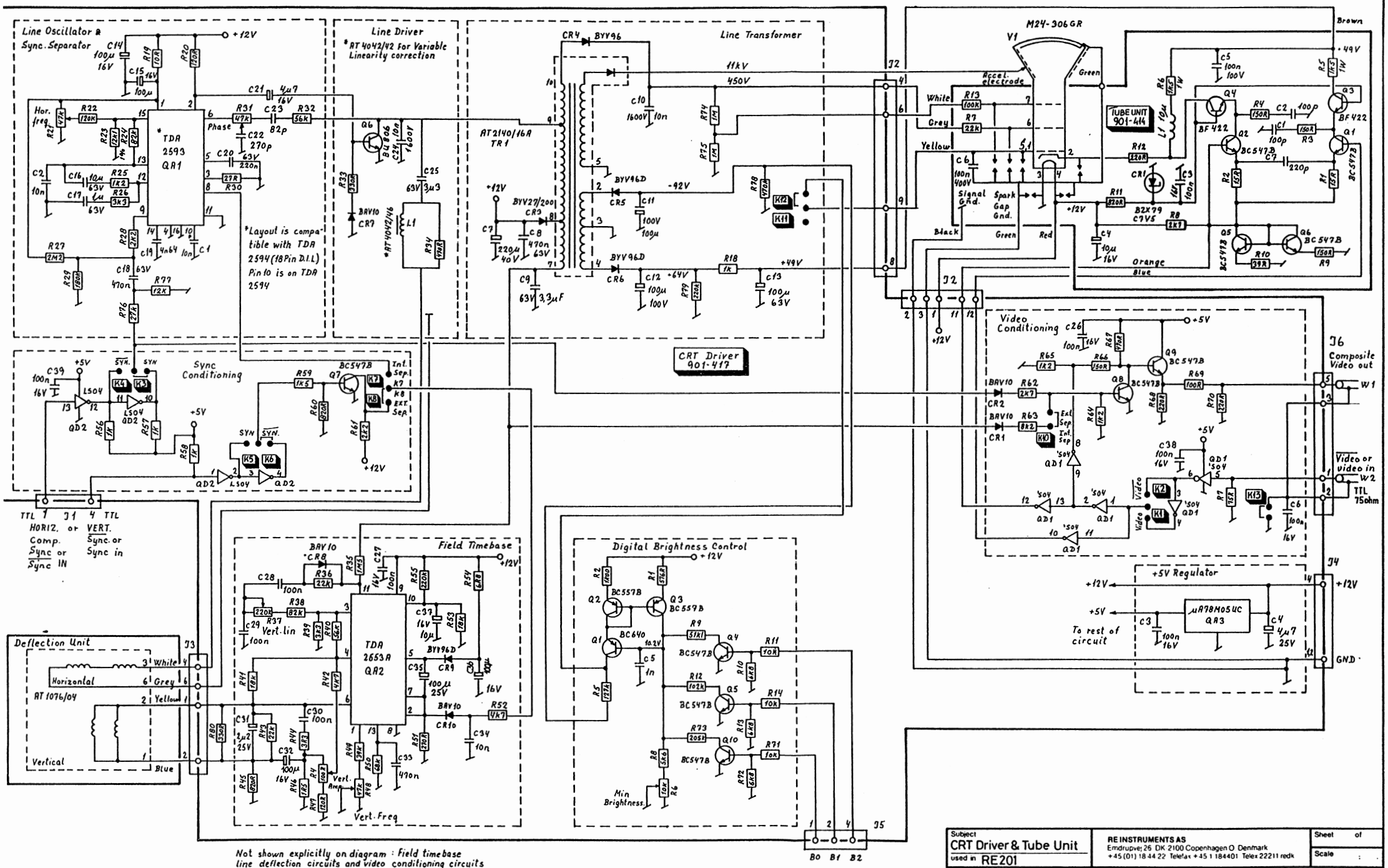

J1
A9
A10
A11
CRUCLK
A5
CRUOUT
A12
A13
A14
CRUIN
GND
QD1
LS138
QD8
HEF 4724
QD12
HEF 4050
+5V
+15V
-15V
C1
C2
C3
C4
C5
C6
R38
4K7
R4F
10k
R6
R5
1K
UNCAL.
READY
REMOTE
B6
J2
460H
430H
440H
450H
MEMORY BUS INTERFACE



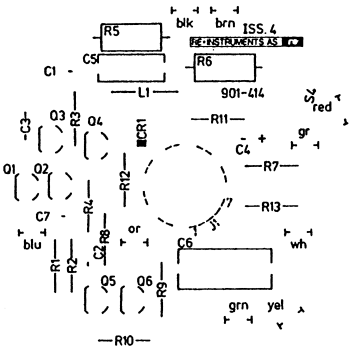
Subject: Keyboard			RE INSTRUMENTS AS			Sheet of	
used in: RE 201						Scale	
Issue/Rev no	1/	2/	3/	4/	5/	PCB	971-156
Date	840306	850710	850905			PCB Assy	901-410
Drawn	UP	TD	BD			Schematic Drawing	985-103
App			NG				

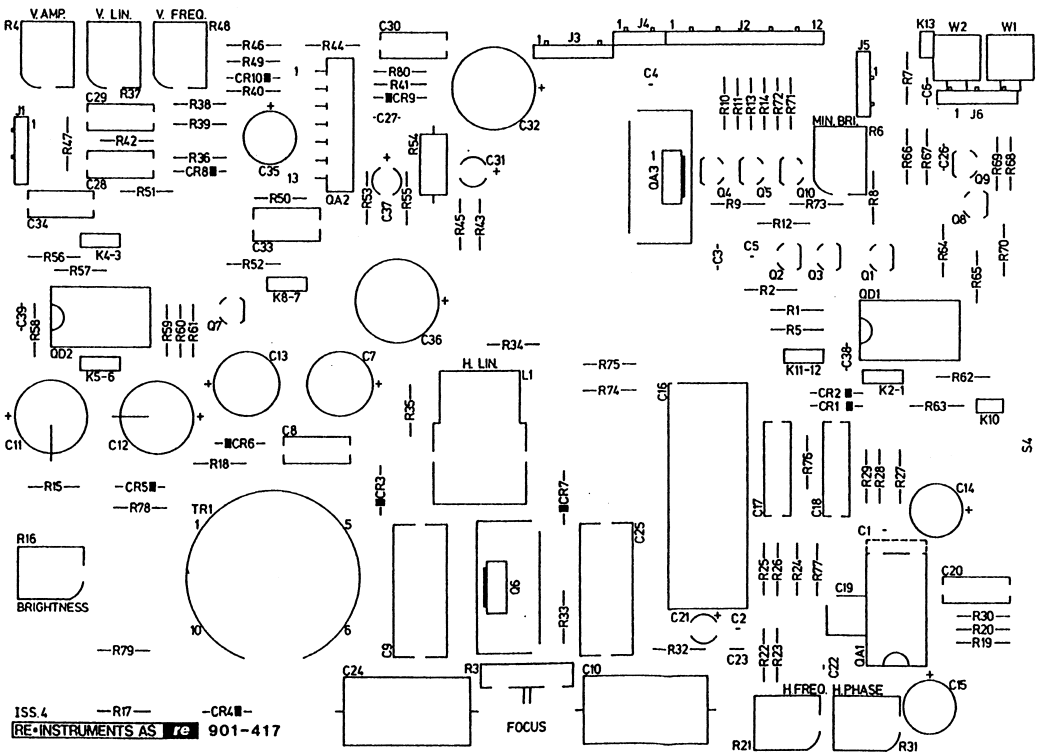

C4
C3
C2
C1
J1
S3
RE•INSTRUMENTS AS
901-410 ISS.5

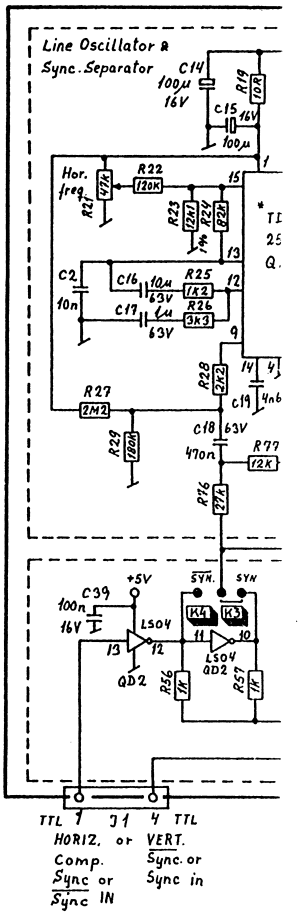

J1
A12
A13
A14
A6
CRUIN
CRUOUT
CRUCLK
STATIC
A9
A10
A11
IT7
+5V
C1
10µF
106H
HEF 4013
QD6
QD7
R3
1k
+5V

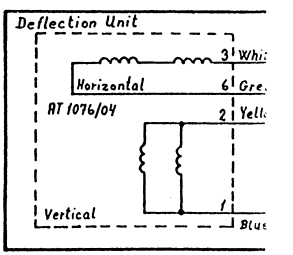


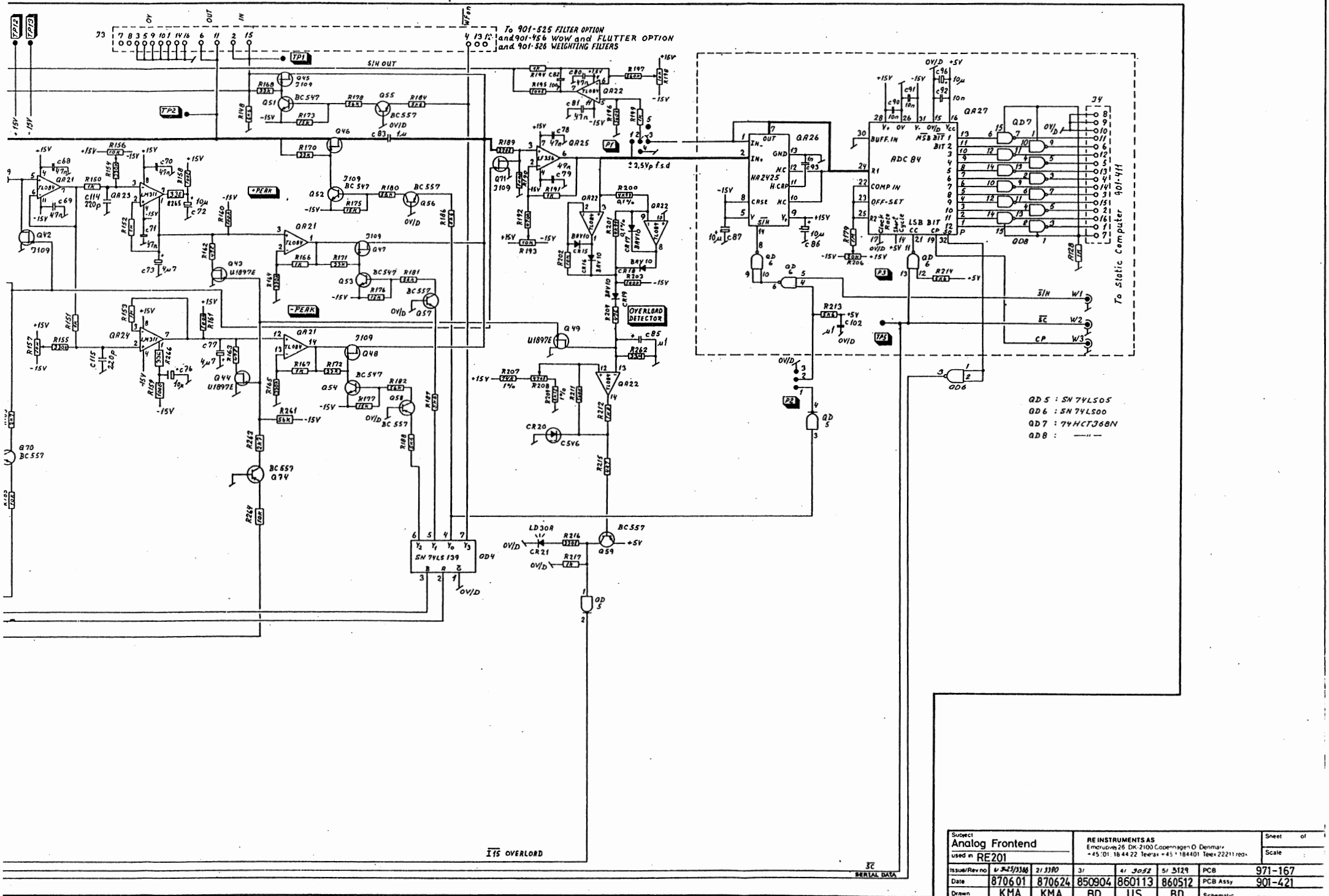
Subject: CRT Driver & Tube Unit used in RE201	RE INSTRUMENTS AS Emdrupvej 26 DK 2100 Copenhagen O Denmark +45 (01) 18 44 22 Telefax +45 1 184401 Telex 22211 redk					Sheet of	
Issue/Rev.no	1/	2/	3/	4/	5/	PCB	971-160.971-163
Date	840306	850711	850904			PCB Assy	901-414 901-417
Drawn	UP	TD	BD			Schematic Drawing	985-106
App.			NE			Scale	: .


blk
brn
ISS. 4
RE•INSTRUMENTS AS
R5
R6
901-414
L1
C1
C5
red
gr
or
wh
blu
grn
yel
R10

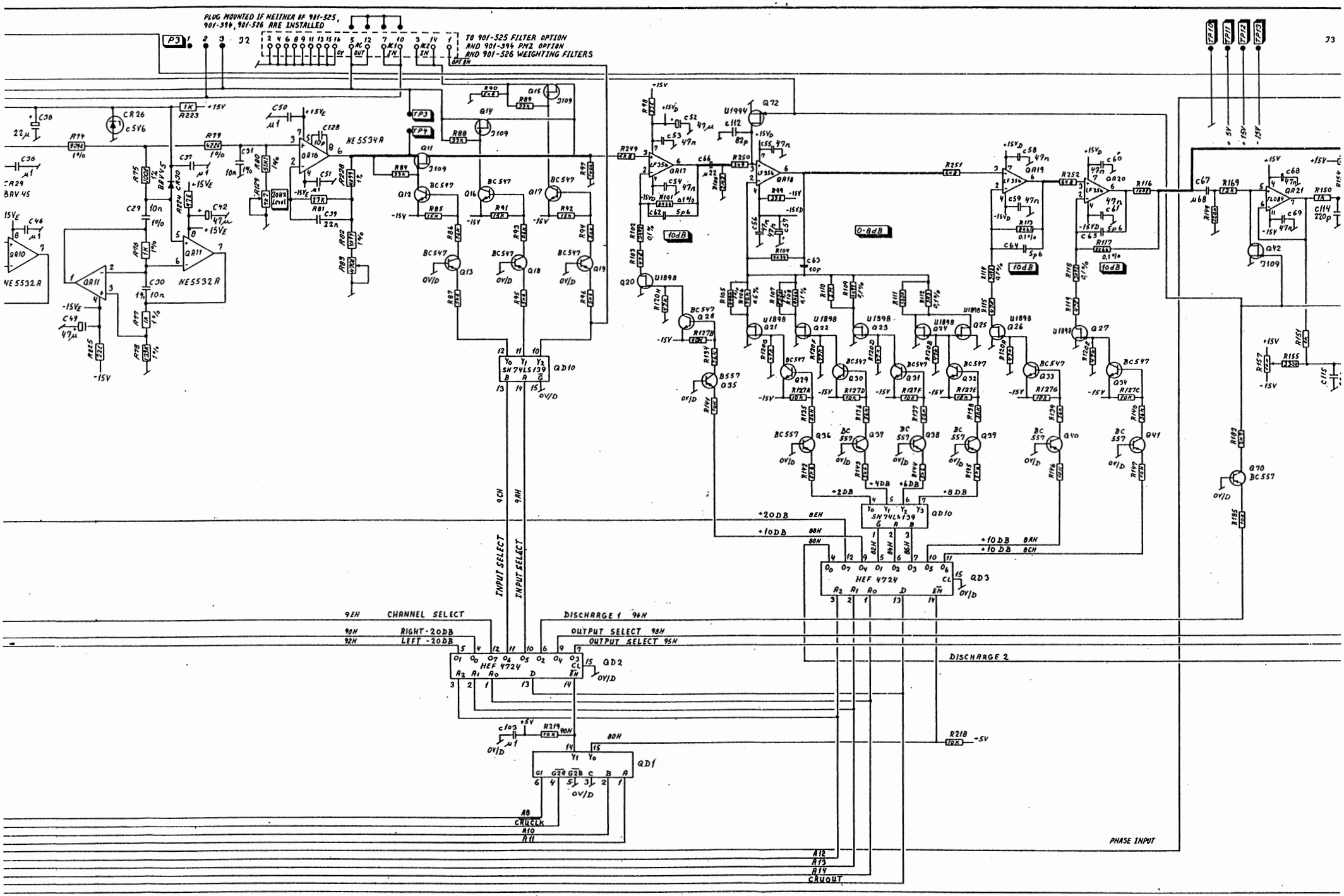

V. AMP.
V. LIN.
V. FREQ.
H. LIN.
BRIGHTNESS
FOCUS
H.FREQ.
H.PHASE
MIN. BRI.
TR1
L1
ISS.4
RE•INSTRUMENTS AS
901-417

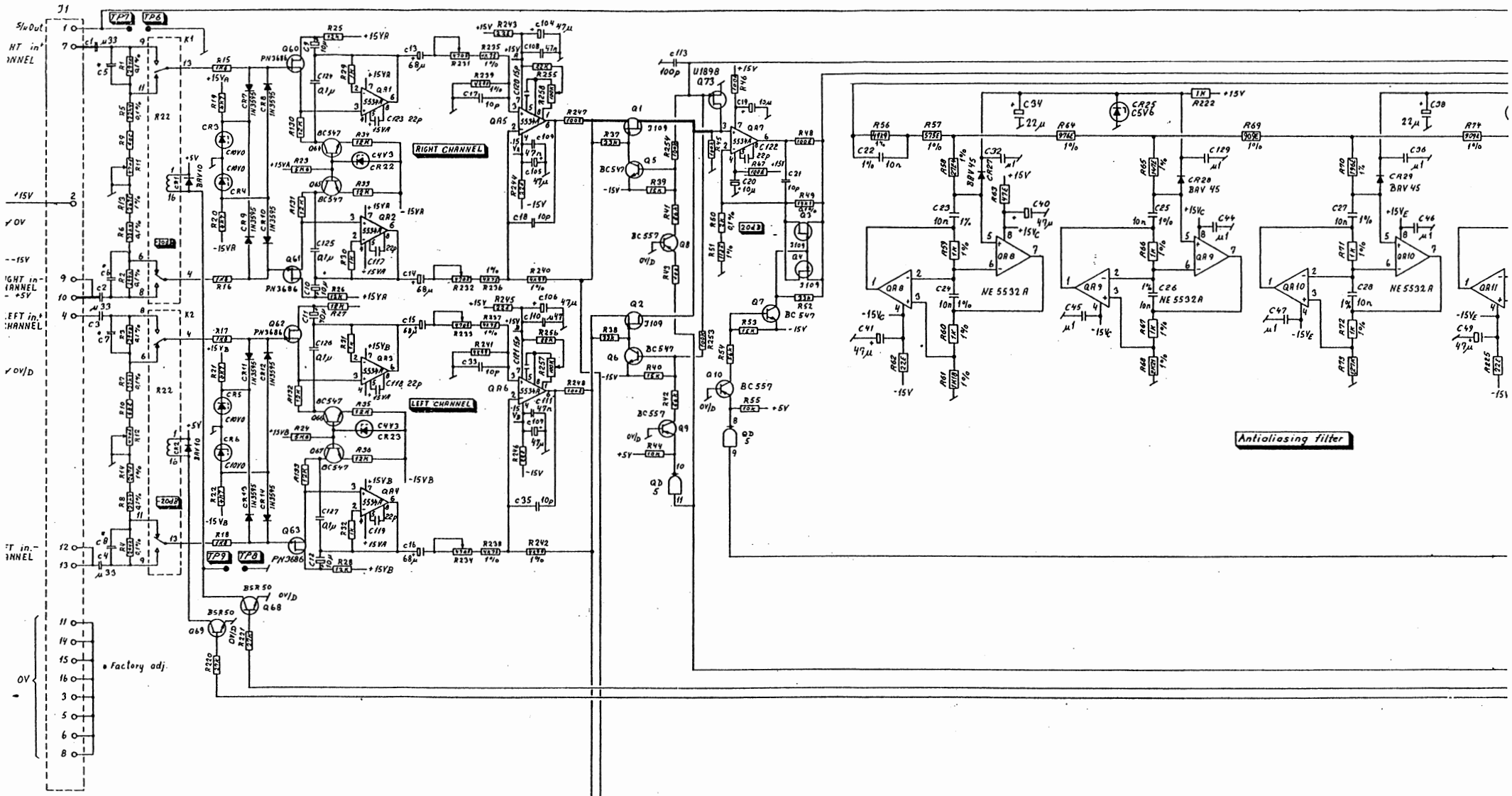

Line Oscillator &
Sync. Separator
Hor. freq.
+5V
SYN.
LS04
TTL
HORIZ. or Comp. Sync or Sync IN
VERT. Sync or Sync in

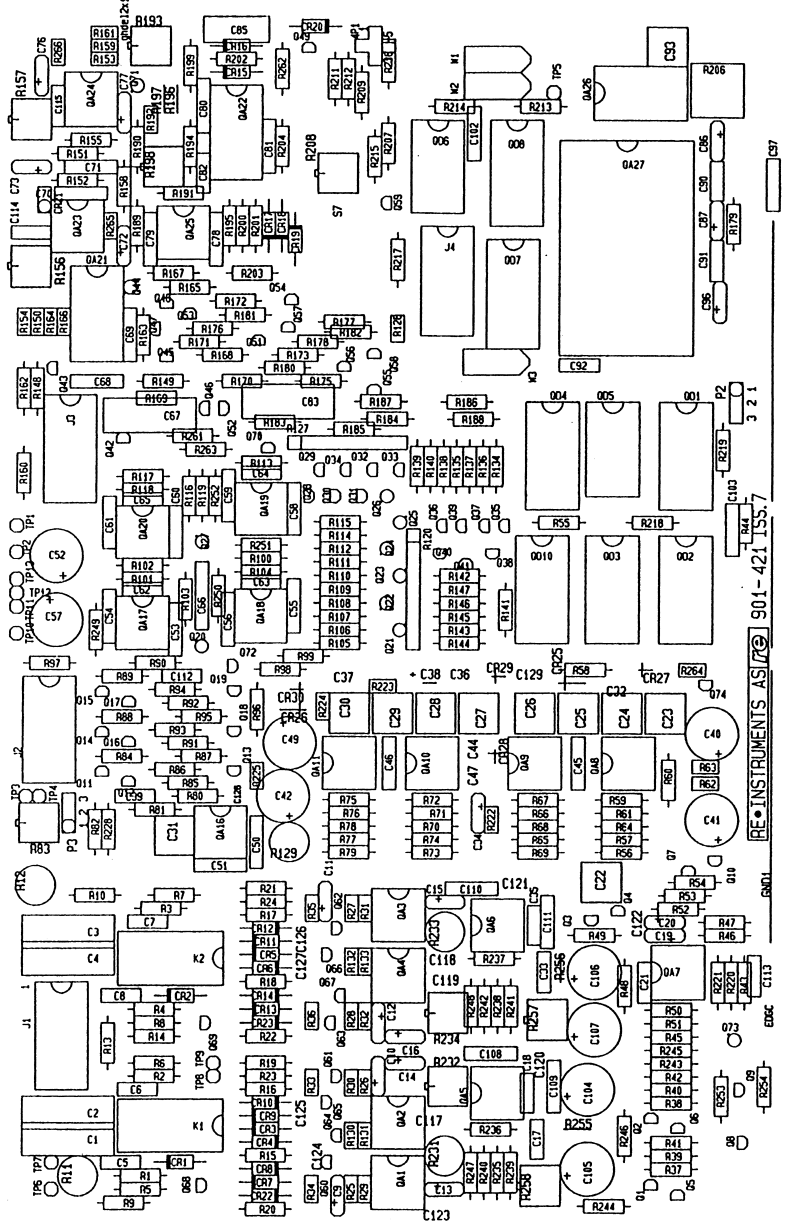

Deflection Unit
Horizontal
AT 1076/04
Vertical

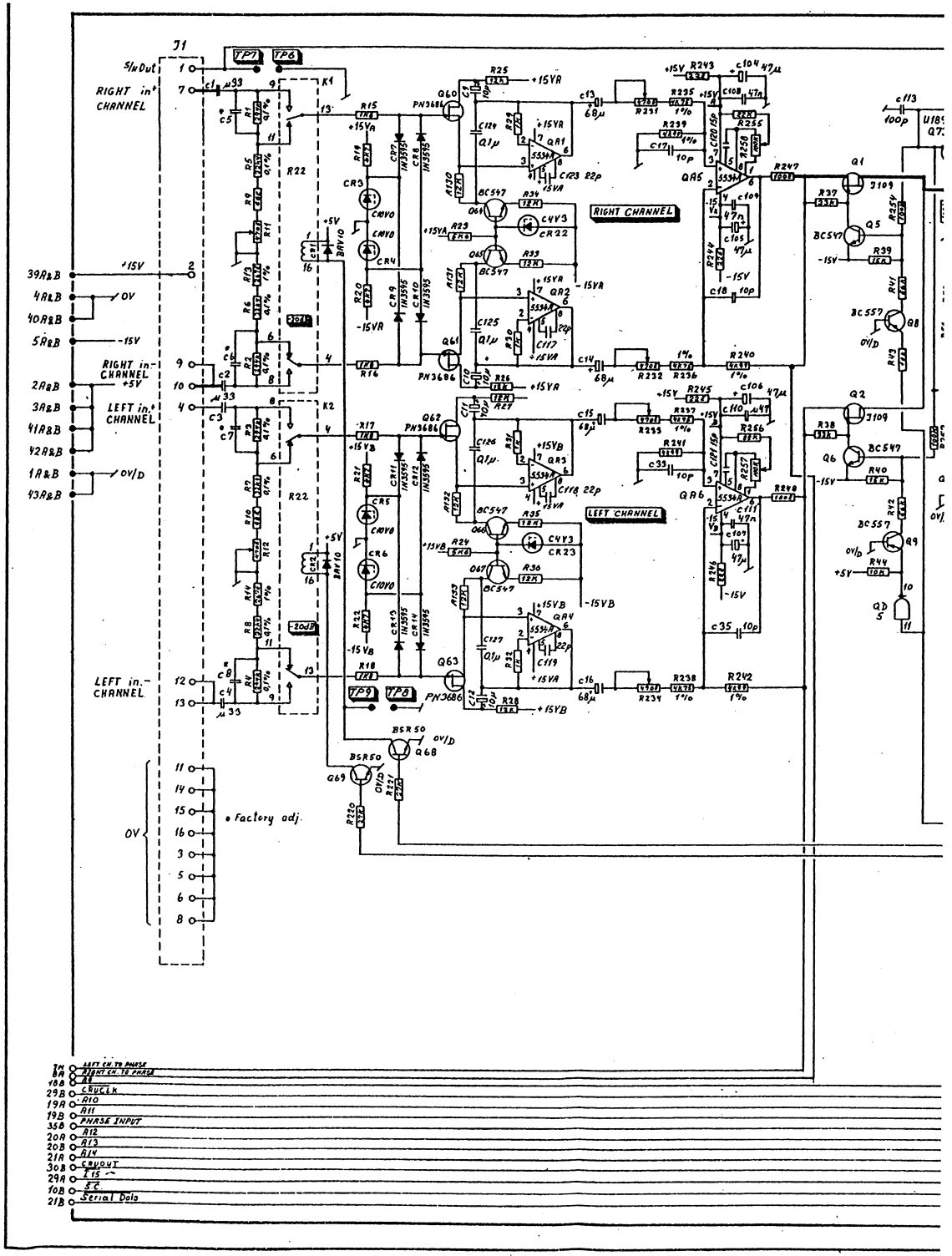


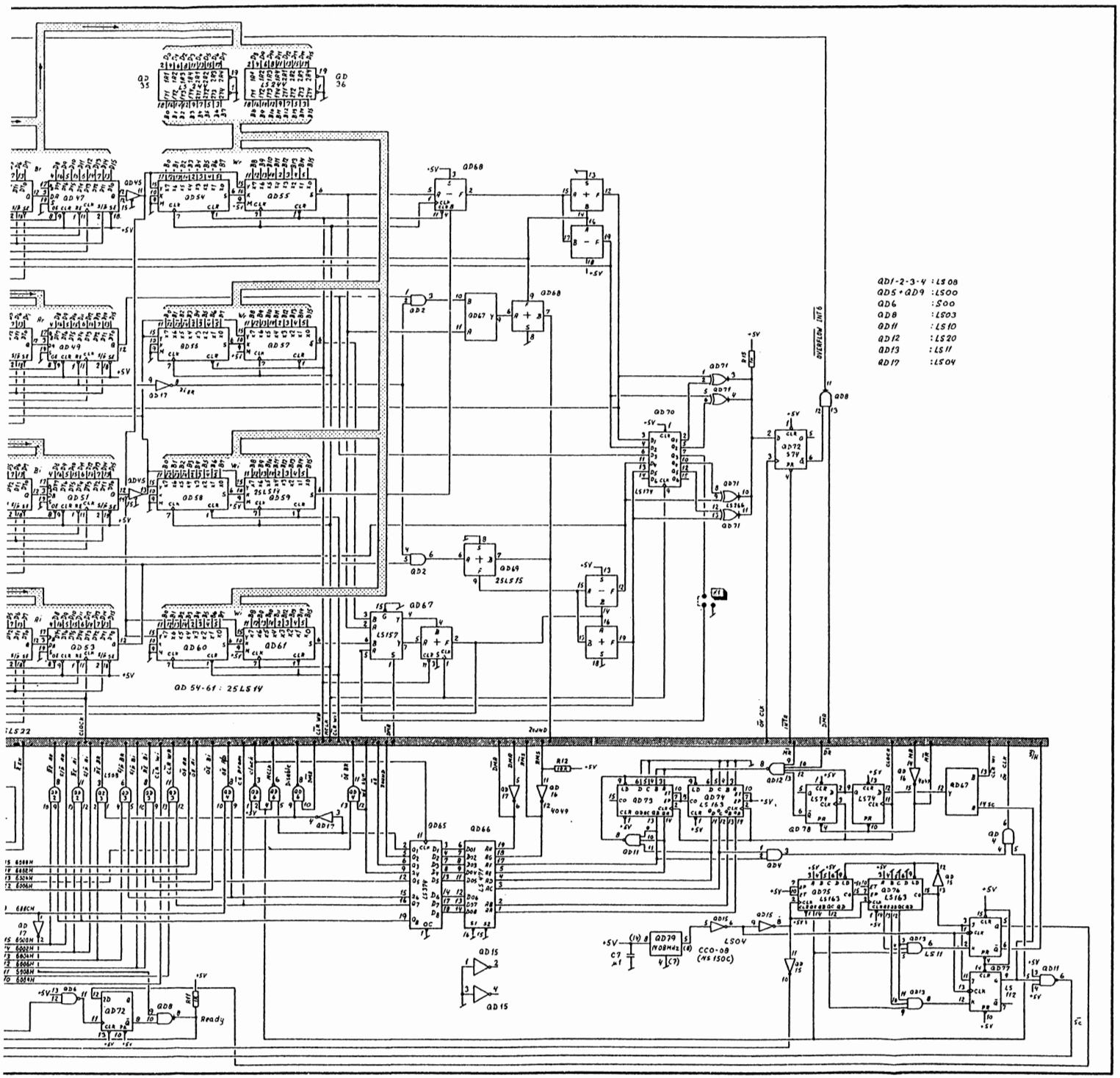
Subject: Analog Frontend, used in RE201	RE INSTRUMENTS AS, Emdrupvej 26 DK-2100 Copenhagen O Denmark, +45 01 18 44 22 Telex +45 1 184401 Telex 22211 reins					Sheet of	
Issue/Rev no	6/ 3425/3386	2/ 3390	3/	4/ 3052	5/ 3129	PCB	971-167
Date	870601	870624	850904	860113	860512	PCB Assy	901-421
Drawn	KMA	KMA	BD	US	BD	Schematic Drawing	985-099
App			NE	WR	NE		


PLUG MOUNTED IF NEITHER OF 901-525, 901-394, 901-526 ARE INSTALLED
TO 901-525 FILTER OPTION AND 901-394 PMZ OPTION AND 901-526 WEIGHTING FILTERS
P3
NE 5534 A
NE 5532 A
SN 74LS 139
HEF 4724
10dB
0-8dB
INPUT SELECT
9CH
9AH
9EH CHANNEL SELECT
90H RIGHT -20DB
92H LEFT -20DB
OUTPUT SELECT 98H
OUTPUT SELECT 95H
DISCHARGE 1 96H
DISCHARGE 2
+20DB 8EH
+10DB 88H
+10DB 8AH
+10DB 8CH
+2DB
+4DB
+6DB
+8DB
80H
A8 CRUCLK
A10
A11
A12
A13
A14 CRUOUT
PHASE INPUT
0V/D
-15V
+15V
+5V

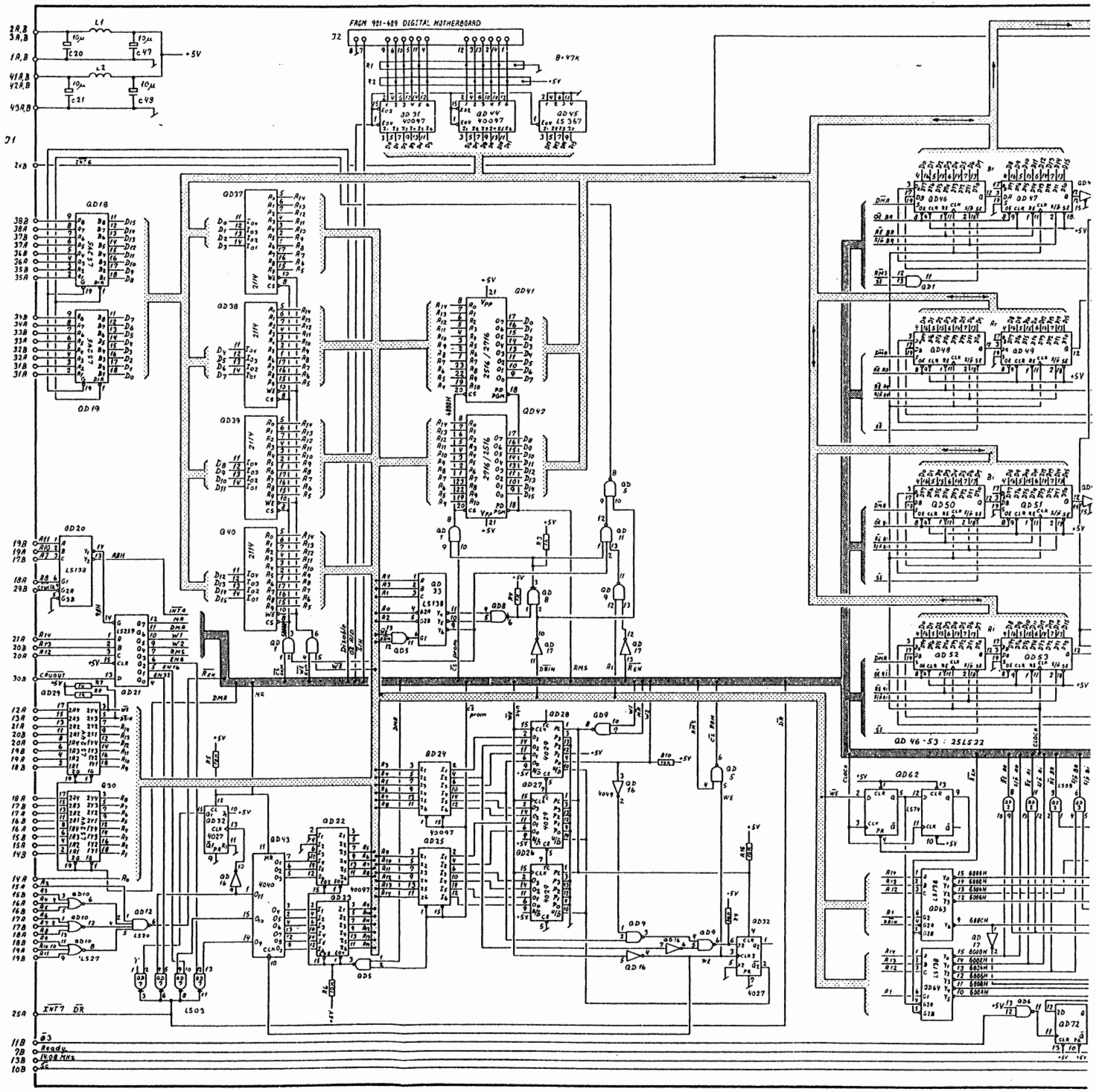

RIGHT CHANNEL
LEFT CHANNEL
Antialiasing filter
NE 5532 A
* Factory adj.

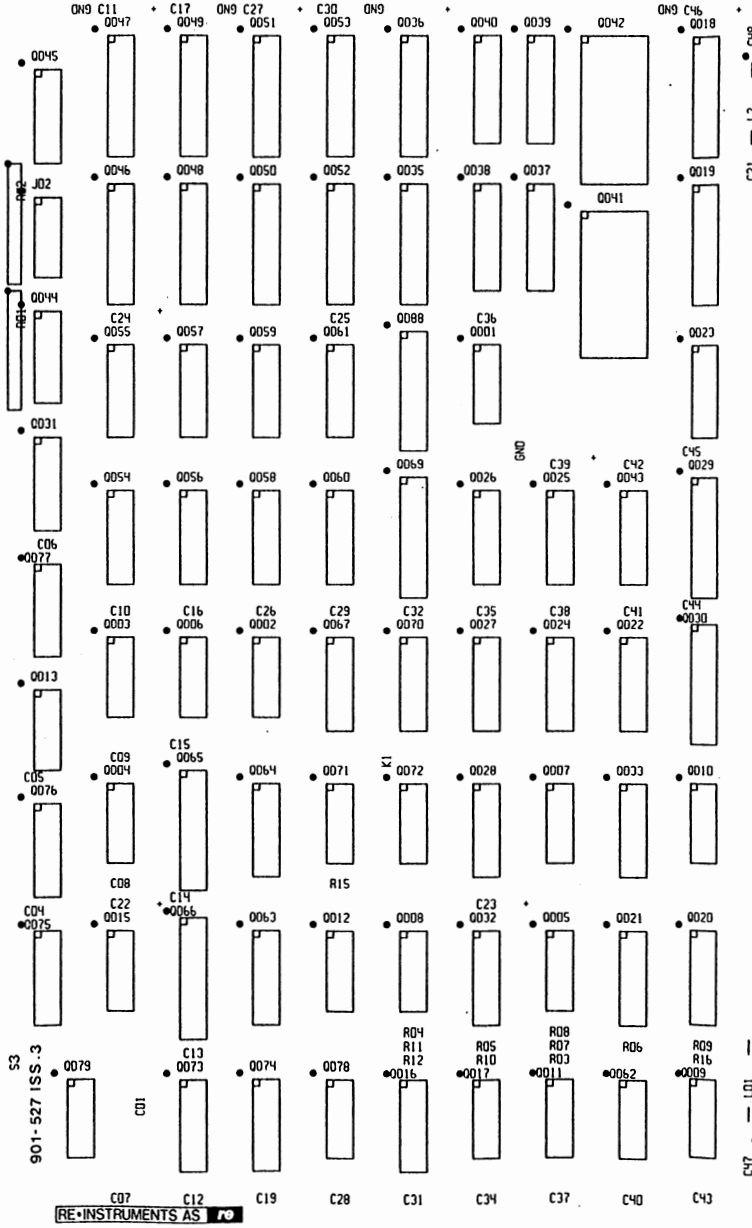


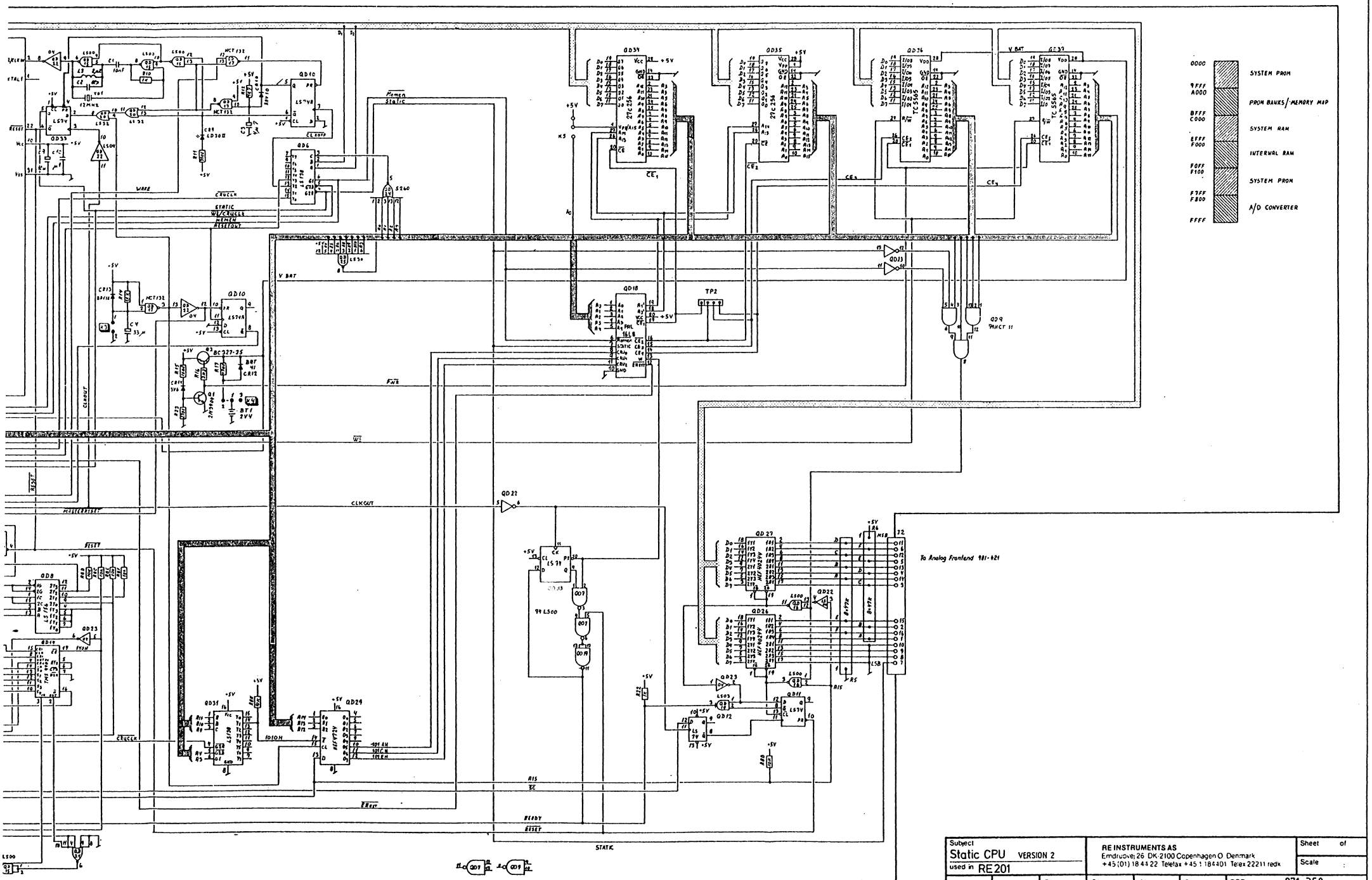

RIGHT in+ CHANNEL
RIGHT in- CHANNEL
LEFT in+ CHANNEL
LEFT in.- CHANNEL
RIGHT CHANNEL
LEFT CHANNEL
* Factory adj.
LEFT CH TO PHASE
RIGHT CH TO PHASE
CLOCK
PHASE INPUT
CHOUT
Serial Data



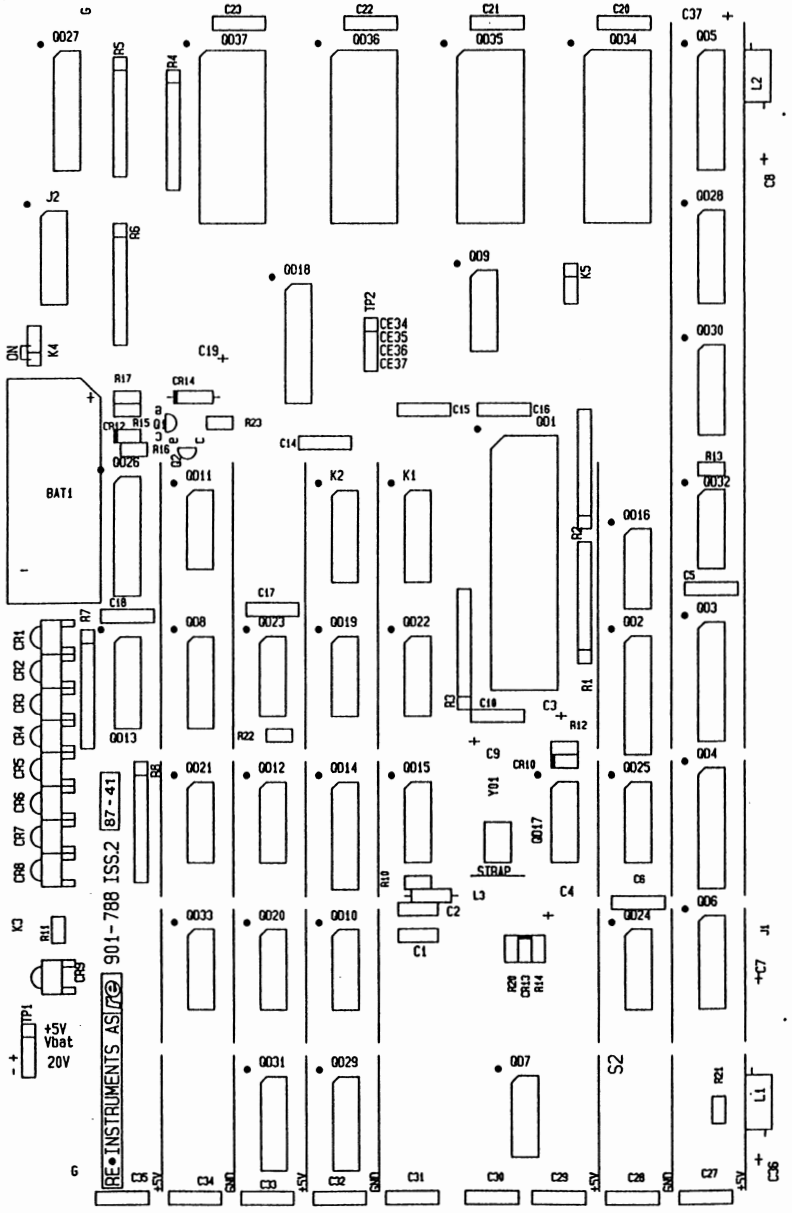
Subject: Arithmetical Unit			RE INSTRUMENTS AS Emdrupvej 26 DK 2100 Copenhagen O Denmark +45 (01) 18 44 22 Telefax +45 1 184401 Telex 22211 redk			Sheet of	
used in RE201						Scale :	
Issue/Rev.no	1/	2/	3/	4/	5/	PCB	971-217
Date	830711	840306	850904			PCB Assy	901-527
Drawn	UP	UP	BD			Schematic Drawing	985-109
App.			NE				

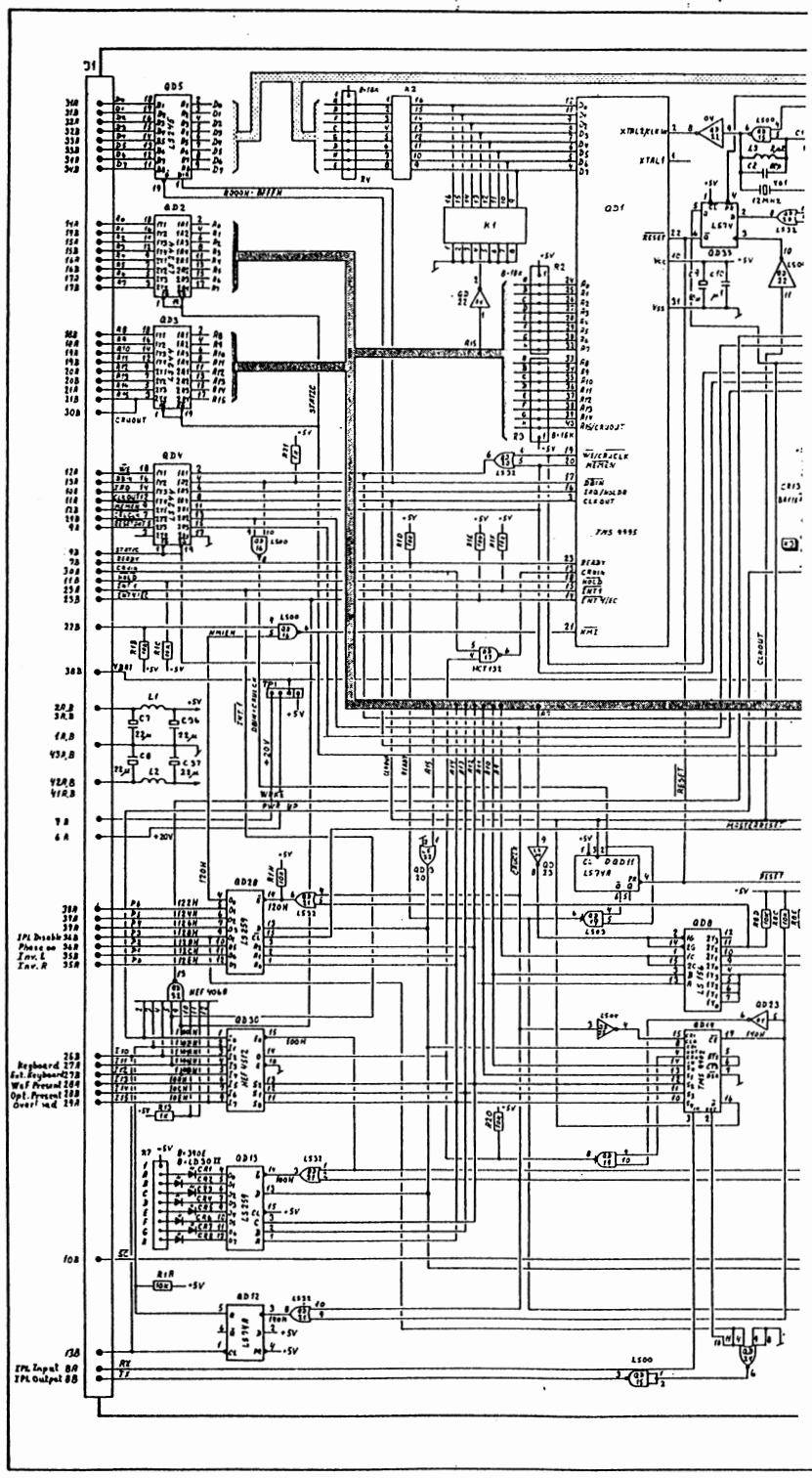

FROM 931-689 DIGITAL MOTHERBOARD
+5V
8-47K
QD 31
QD 44
QD 45
QD 18
QD 19
QD 37
QD 38
QD 39
QD 40
QD 41
QD 42
QD 20
LS138
QD 29
QD 21
QD 30
QD 24
QD 25
QD 28
QD 27
QD 26
QD 22
QD 23
QD 43
4040
QD 12
QD 10
QD 11
LS20
LS27
LS03
QD 32
4027
QD 62
LS74
QD 63
2D69
QD 72
QD 4
QD 5
QD 6
QD 7
QD 8
QD 9
QD 16
QD 17
QD 33
QD 48
QD 49
QD 50
QD 51
QD 52
QD 53
QD V6-53 : 25LS22
INT7
INT6
DMA
WT
W2
RMS
EN33
EN16
ABH
DR
Ready
8MHz
CLOCK

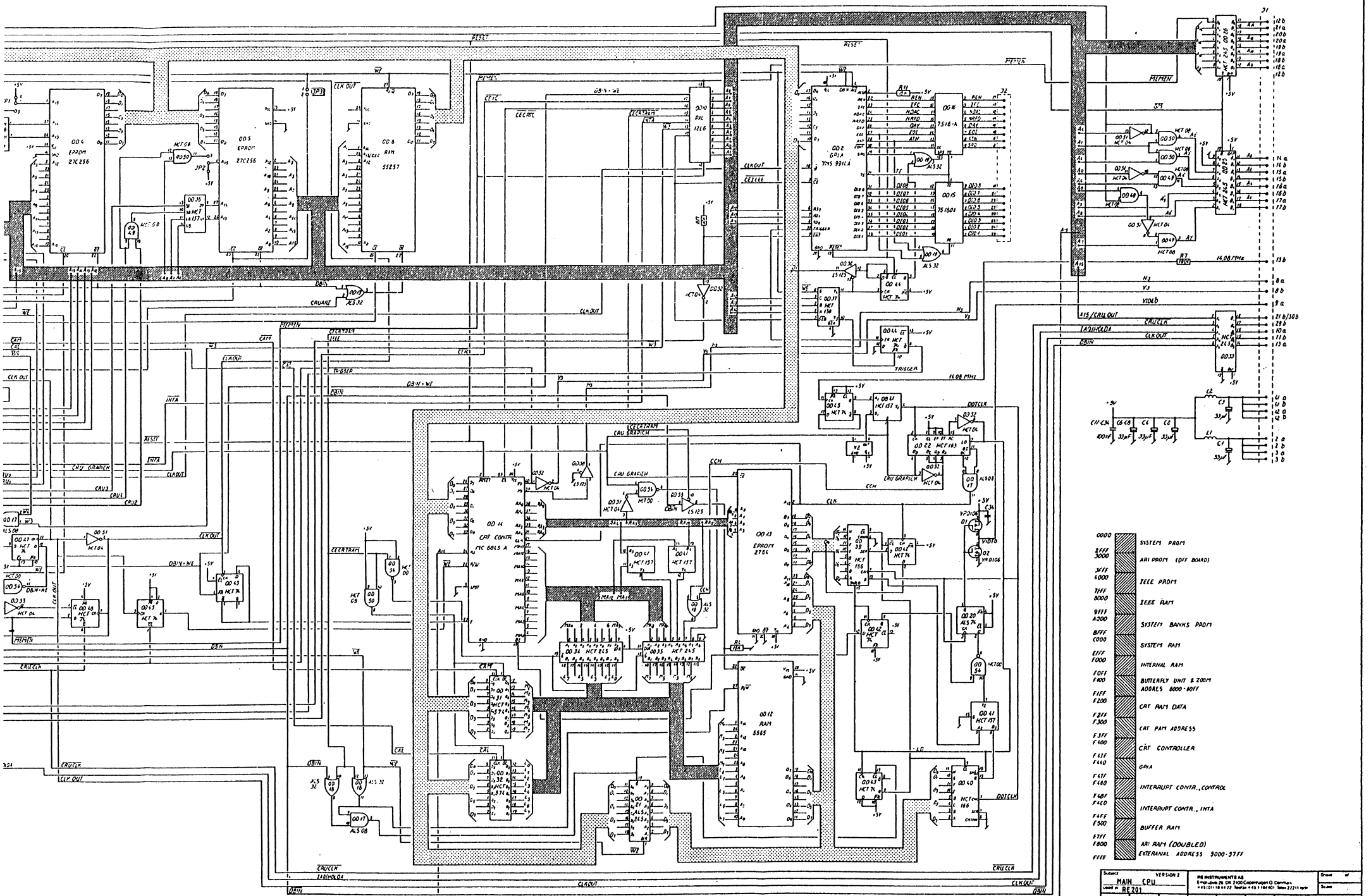

ON9 C11
Q047
C17
Q049
ON9 C27
Q051
C30
Q053
ON9
Q036
Q040
Q039
Q042
ON9 C46
Q018
C48
L2
C21
Q045
J02
A03
Q046
Q048
Q050
Q052
Q035
Q038
Q037
Q041
Q019
A01
Q044
C24
Q055
Q057
Q059
C25
Q061
Q088
C36
Q001
Q023
Q031
Q054
Q056
Q058
Q060
Q069
Q026
GND
C39
Q025
C42
Q043
C45
Q029
C06
Q077
C10
Q003
C16
Q006
C26
Q002
C29
Q067
C32
Q070
C35
Q027
C38
Q024
C41
Q022
C44
Q030
Q013
C09
Q004
C15
Q065
Q064
Q071
K1
Q072
Q028
Q007
Q033
Q010
C05
Q076
C08
R15
C04
Q075
C22
Q015
C14
Q066
Q063
Q012
Q008
C23
Q032
Q005
Q021
Q020
C20
S3
901-527 ISS.3
Q079
C13
Q073
Q074
Q078
R04
R11
R12
Q016
R05
R10
Q017
R08
R07
R03
Q011
R06
Q062
R09
R16
Q009
C47
L01
C01
C07
C12
C19
C28
C31
C34
C37
C40
C43
RE•INSTRUMENTS AS no

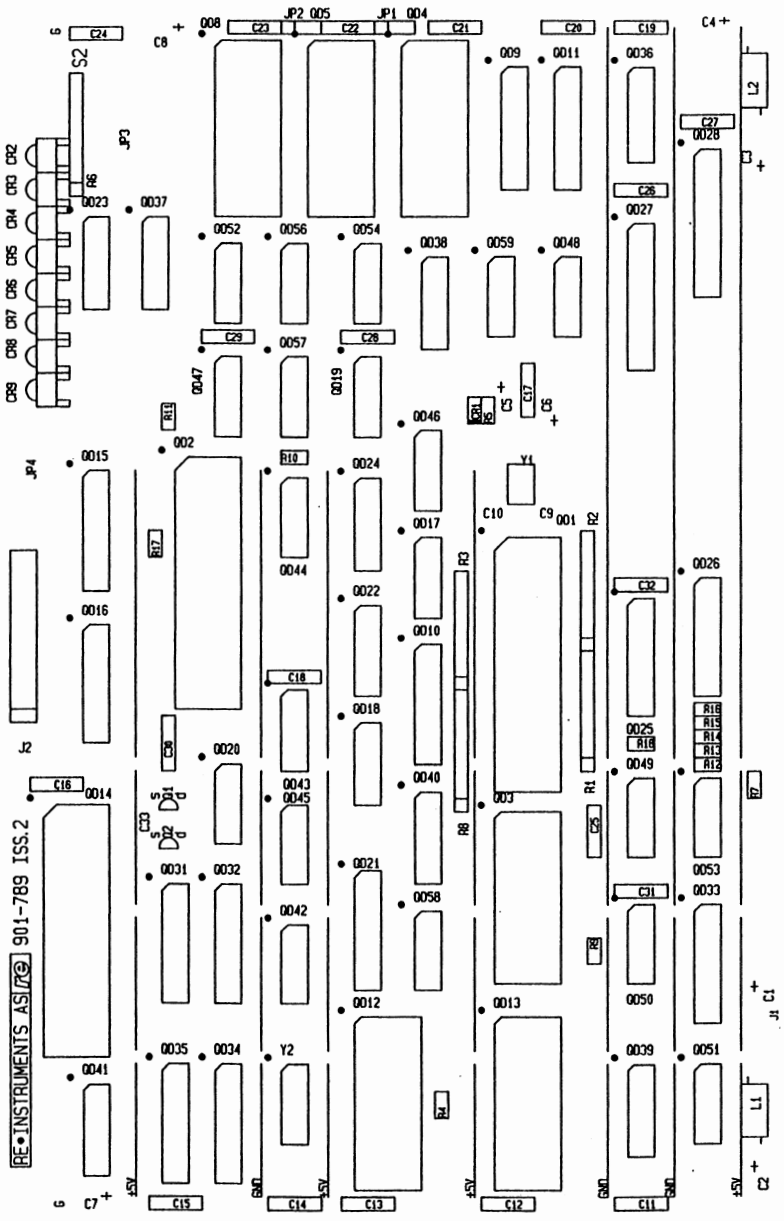


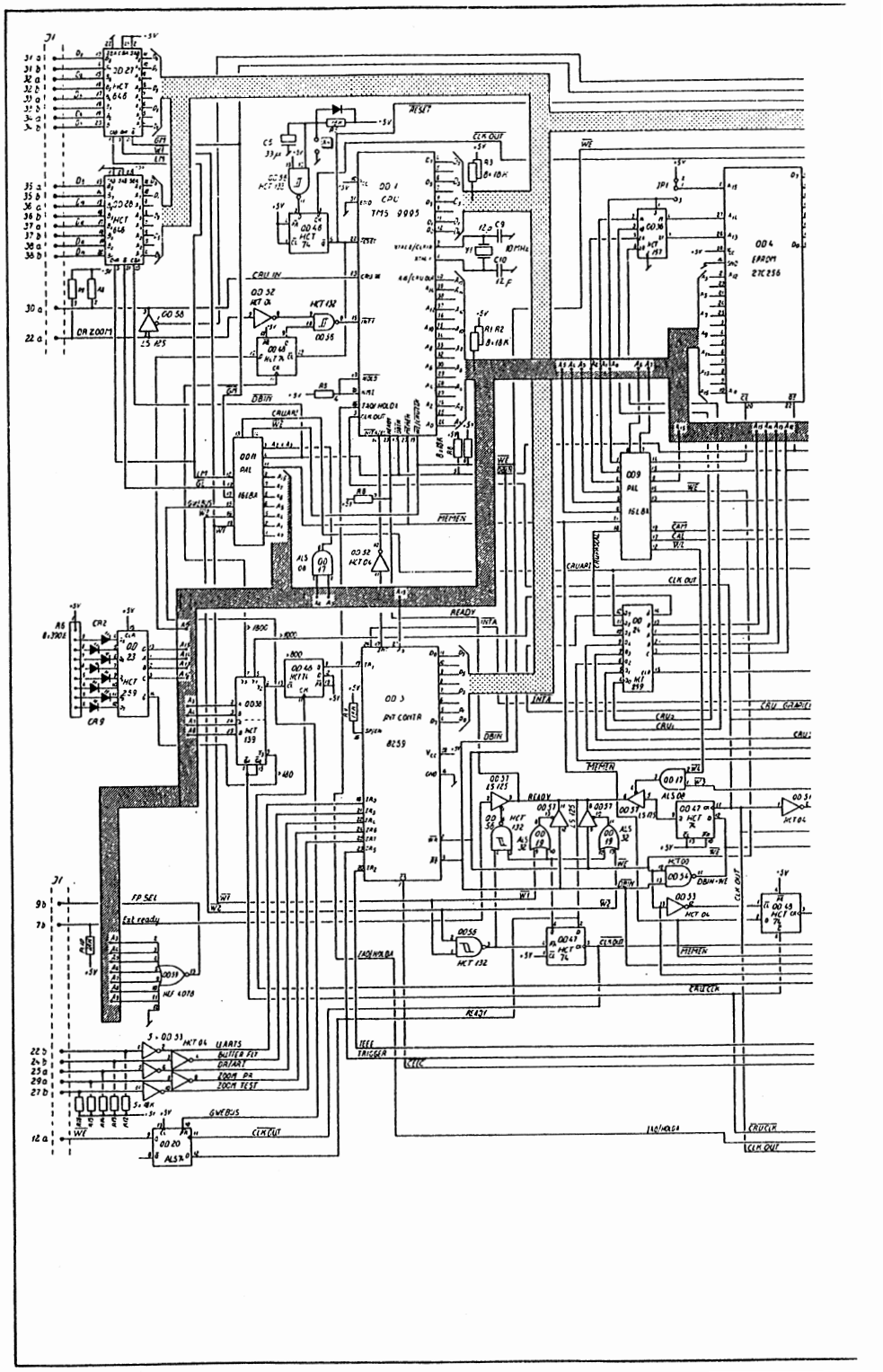
Subject: Static CPU VERSION 2			RE INSTRUMENTS AS Emdrupvej 26 DK-2100 Copenhagen O Denmark +45 (01) 18 44 22 Teletax +45 1 184401 Telex 22211 redk				Sheet of
used in RE 201							Scale
Issue/Rev no	1/	2/	3/	4/	5/	PCB	971-350
Date	861210					PCB Assy	901-788
Drawn	UTH					Schematic Drawing	985-251
App.							

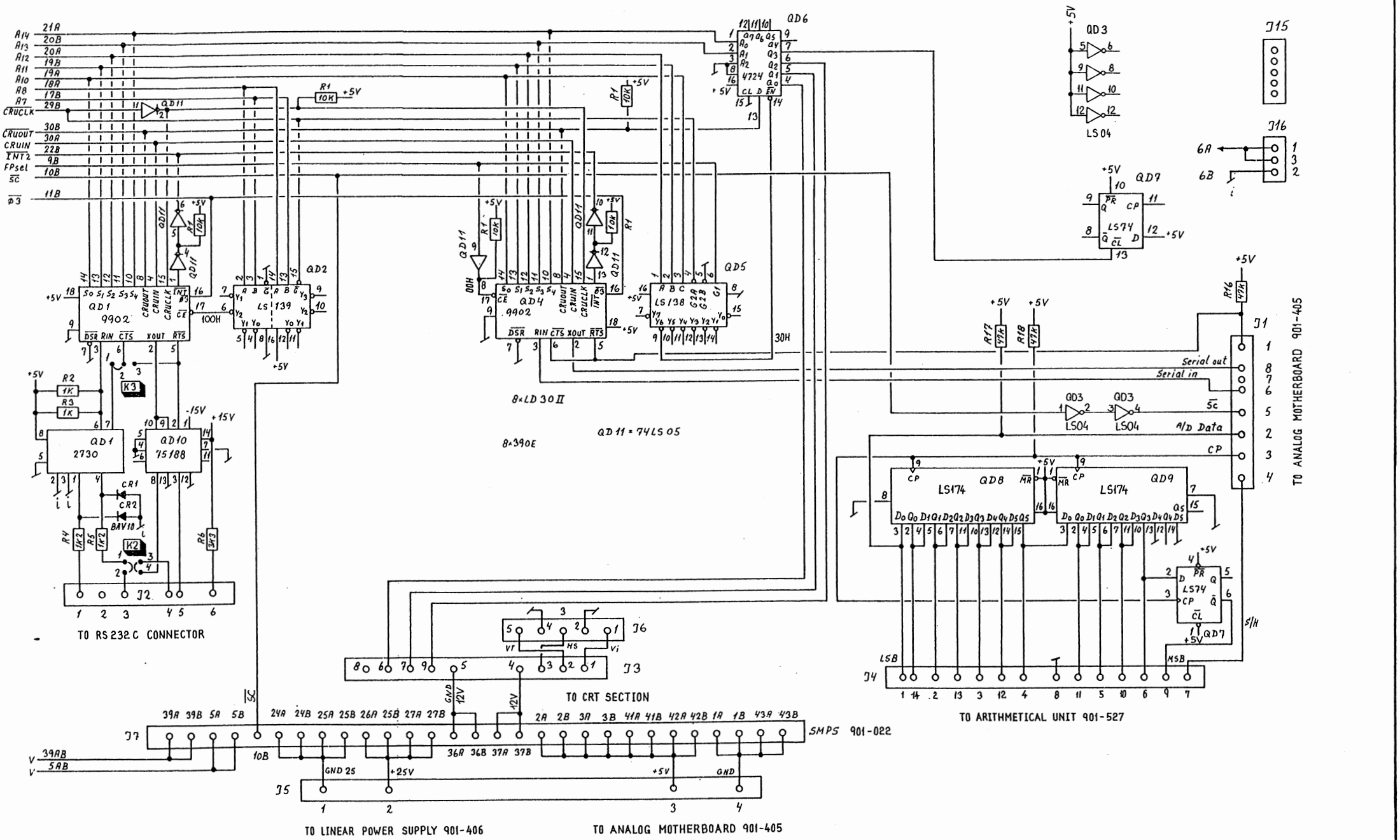

TEXAS INSTRUMENTS ASC 901-788 ISS.2 87-41
BAT1
ON
STRAP
+5V
Vbat
20V




0000 SYSTEM PROM
3FFF
3000 ARI PROM (OFF BOARD)
3FFF
4000 TELE PROM
7FFF
8000 IEEE RAM
9FFF
A000 SYSTEM BANKS PROM
BFFF
C000 SYSTEM RAM
EFFF
F000 INTERNAL RAM
FOFF
F100 BUTTERFLY UNIT & ZOOM ADDRES 8000-80FF
F1FF
F200 CRT RAM DATA
F2FF
F300 CRT RAM ADDRESS
F3FF
F400 CRT CONTROLLER
F43F
F440 GPIA
F47F
F480 INTERRUPT CONTR., CONTROL
F4BF
F4C0 INTERRUPT CONTR., INTA
F4FF
F500 BUFFER RAM
F7FF
F800 ARI RAM (DOUBLED) EXTERNAL ADDRESS 9000-97FF
FFFF
MAIN CPU
RE201
VERSION 2
RE INSTRUMENTS AB
PCB 971-352
PCB Assy 901789
Schematic Drawing 985-252

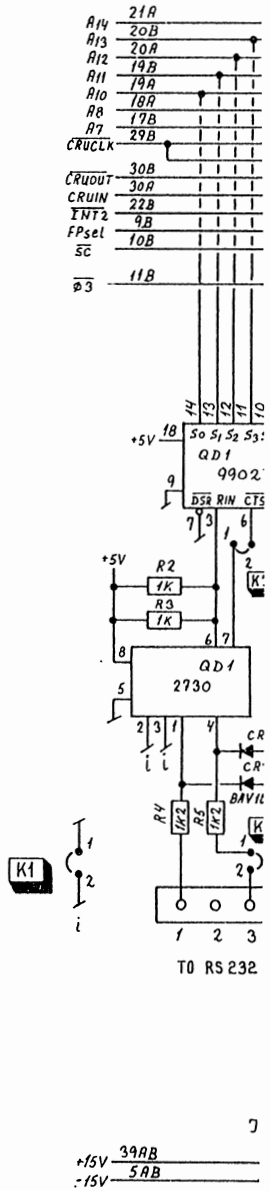

RE•INSTRUMENTS AS 901-789 ISS.2
JP1 JP2 JP3 JP4 JP5
S2
J1 J2
L1 L2
C1 C2 C3 C4 C5 C6 C7 C8
Y1 Y2
D1 D2
R1 R2 R3 R4 R5 R6 R7 R8
CR1 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9
U001 U002 U003 U004 U009 U011 U012 U013 U014 U015 U016 U017 U018 U019 U020 U021 U022 U023 U024 U025 U026 U027 U028 U029 U030 U031 U032 U033 U034 U035 U036 U037 U038 U039 U040 U041 U042 U043 U044 U045 U046 U047 U048 U049 U050 U051 U052 U053 U054 U056 U057 U058 U059
+5V GND


J1
RESET
CLK OUT
CRU IN
DBIN
MEMEN
READY
INTA
WE
FP SEL
Ext ready
GWEBUS
CLKOUT
IEEE TRIGGER
UARTS
BUFFER FLT
DRTART
ROM PA
ROM TEST
CRUCLK
IAQ/HOLDA

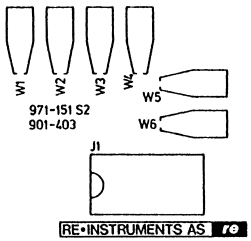


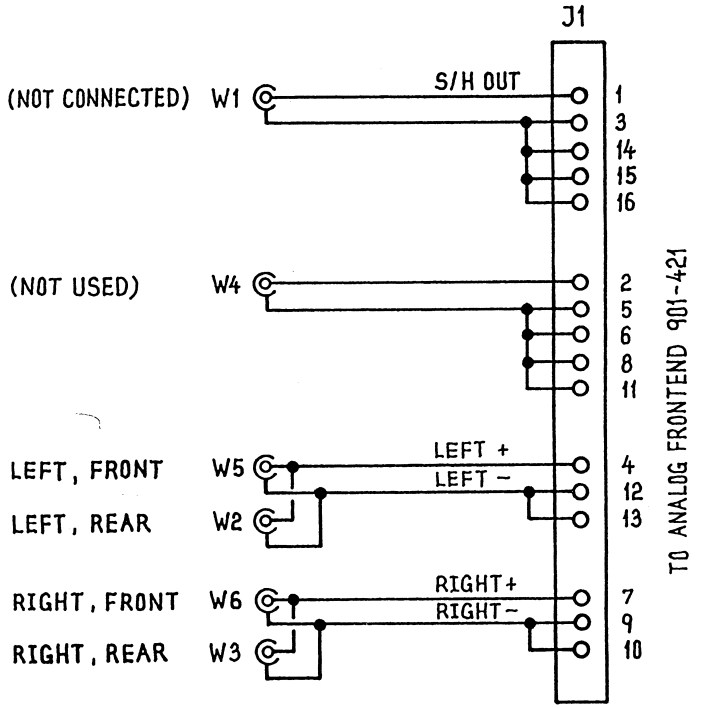
Subject: Digital Motherboard	VERSION 2	RE INSTRUMENTS AS Emdrupvej 26 DK 2100 Copenhagen O Denmark +45) 01 18 44 22 Telefax +45 1 184401 Telex 22211 redx				Sheet of	
used in RE201						Scale	
Issue/Rev no	1/	2/	3/	4/	5/	PCB	971-351
Date	87 10 27					PCB Assy	901-790
Drawn	KMA					Schematic Drawing	985-253
App							

PIN NO	MNEM	DESCRIPTION	PIN NO	MNEM	
1A	GND	Digital Ground	1B	GND	Digital Ground
2A	+5V	+5V DC	2B	+5V	+5V DC
3A	+5V	+5V DC	3B	+5V	+5V DC
4A	GND	Analog Ground	4B	GND	Analog Ground
5A	-15V	-15V	5B	-15V	-15V
6A			6B	GNDi	Isolated Ground
7A	Wait		7B	Ready	
8A	HorSync	Horizontal CRT Sync.	8B	VertSync	Vertical CRT Sync.
9A	VIDEO	CRT VIDEO	9B	FPSEL	Front Panel Select
10A	IAQ	Instr. Acquisition	10B	Sync	Power Supply Sync
11A	P4		11B	Ø3	Clockout from CPU
12A	$\overline{WE}$	Write Enable	12B	$\overline{MEMEN}$	Memory Enable
13A	$\overline{DBIN}$	Data Bus In	13B	14.o8	14.o8 MHZ Sysclk
14A	A0	MSB of Address	14B	A1	
15A	A2		15B	A3	
16A	A4		16B	A5	
17A	A6		17B	A7	
18A	A8		18B	A9	
19A	A1o		19B	A11	
20A	A12		20B	A13	
21A	A14		21B	A15	LSB of address (=0)
22A	I1	$\overline{DR}$ from Zoom	22B	I2	Interrupt from RS232C
23A	I3	Timerinterrupt	23B	I4	CRT Interrupt
24A	I5	IEEE 488 Interrupt	24B	I6	Butterfly Interrupt
25A	I7	$\overline{DR}$ from ARI.Unit	25B	I8	
26A	I9		26	I1o	
27A	I11		27B	I12	Zoom Test
28A	I13	IEEE $\overline{PRESENT}$	28B	I14	Trigger
29A	I15	Zoom $\overline{PRESENT}$	29B	CRUCLK	$\overline{Cruclk}$
30A	CRUIN	CRU Input	30B	CRUOUT	CRU Output
31A	DO	MSB of Databus	31B	D1	
32A	D2		32B	D3	
33A	D4		33B	D5	
34A	D6		34B	D7	
35A	D8		35B	D9	
36A	D1o		36B	D11	
37A	D12		37B	D13	
38A	D14		38B	D15	LSB of databus
39A	+15V	+15V	39B	+15V	+15V
40A	GND	Analog Ground	40B	GND	Analog Ground
41A	+5V	+5V DC	41B	+5V	+5V DC
42A	+5V	+5V DC	42B	+5V	+5V DC
43A	GND	Digital Ground	43B	GND	Digital Ground

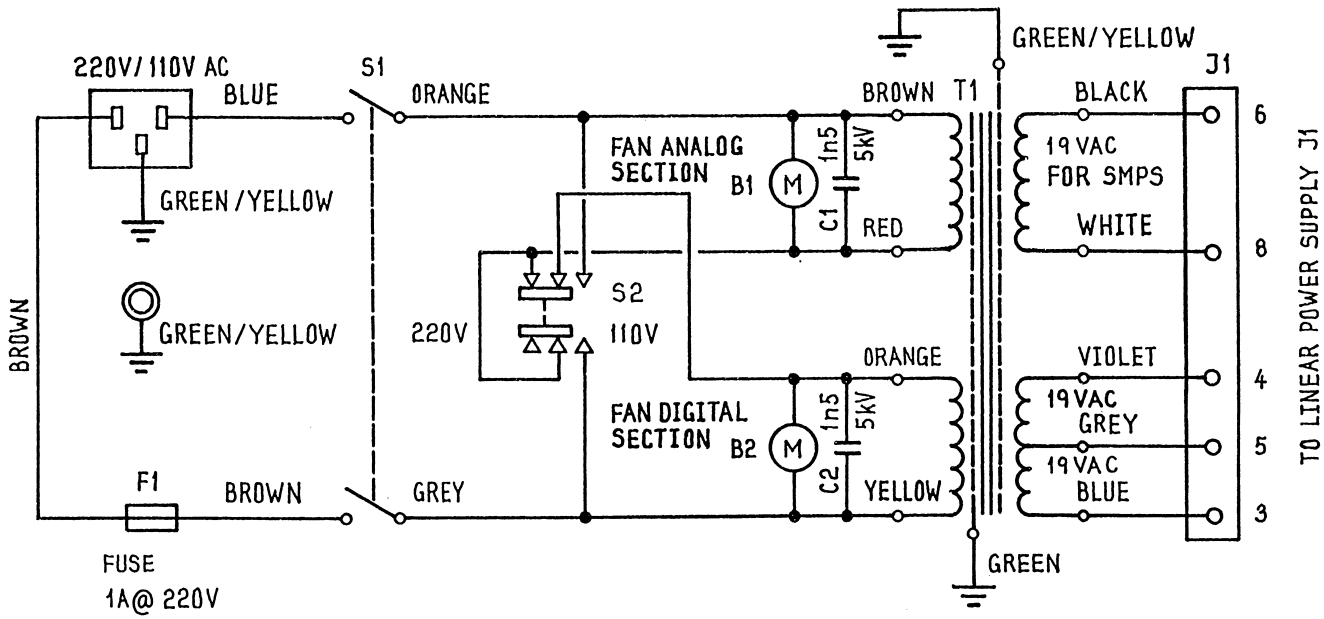


J5
D000
R01
J2
C01
L01
J7
A B
CR1
CR2
RD4
RD5
K2
K3
K1
Q1
Q100
Q000
Q001
Q010
J1
Q004
Q007
R16
Q005
R18
Q008
R17
RD2
RD3
RD6
J4
J2
R13
R15
R11
R14
R08
J8
Q03
C19
C25
C02
C08
2
92
J9
J6
9A
C18
C24
C03
C09
3
J10
8A
S1
C17
C23
C04
C10
4
J11
8B
C16
C22
C05
C11
5
J12
C15
C21
C06
C12
6
J13
C14
C20
C07
C13
7
J14
J16
R12
R10
R09
D000
J15

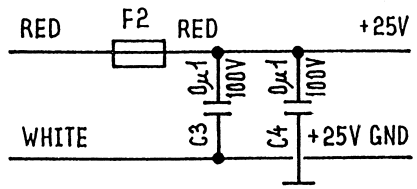




Subject: Interconnection Board used in RE201			RE INSTRUMENTS AS Emdrupvej 26 DK 2100 Copenhagen Ø Denmark +45 (0)1 18 44 22 Telefax +45 (0)1 84401 Telex 22211 reds			Sheet of	
						Scale	
Issue/Rev no	1/	2/	3/	4/	5/	PCB	971-151
Date	850905					PCB Assy	901-403
Drawn	BD					Schematic Drawing	985-210
App	NG						

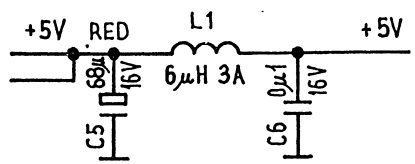


FROM LINEAR POWER SUPPLY J2



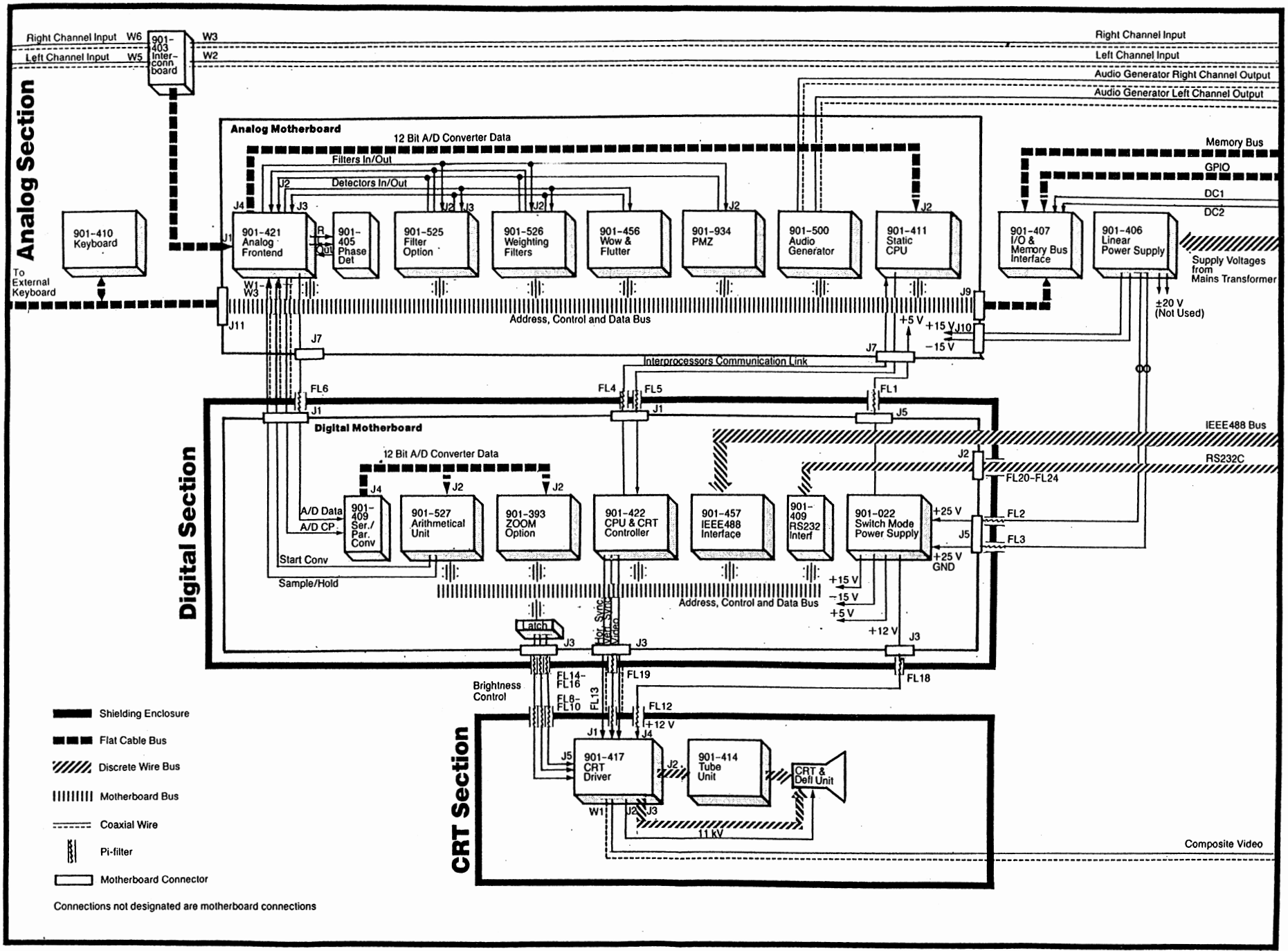
TO DIGITAL MOTHERBOARD J5

TO ANALOG MOTHERBOARD J7

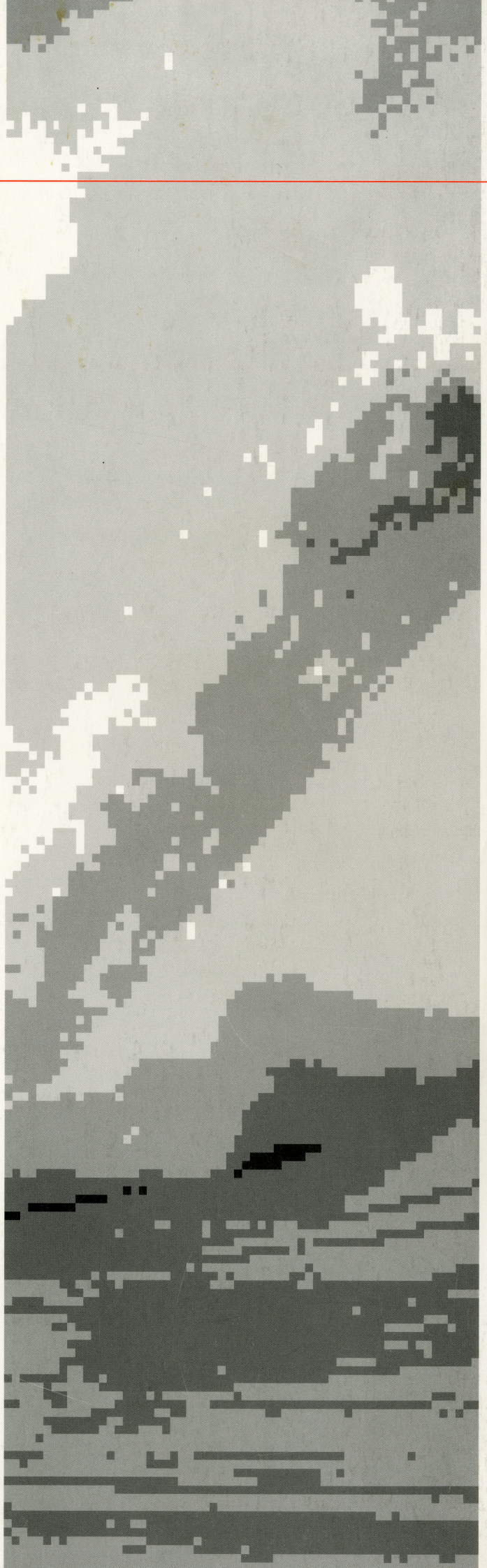


FROM DIGITAL MOTHERBOARD J5

Subject: Mains Input and Power Supply Filters used in: RE201			RE INSTRUMENTS AS				Sheet of
							Scale
Issue/Rev.no	1/	2/	3/	4/	5/	PCB	
Date	850905					PCB Assy	
Drawn	BD					Schematic Drawing	985-211
App	NE						



RE201 Top level interconnections and block diagram 985-217



983-297.20a