

SQUAWK/NAUT I



OVERHAUL MANUAL



© Kustom Electronics, Inc.

USTOM INSTRUMENTS
CHANUTE, KANSAS 66720

P/N 006-0032-00

NOTICE OF OPERATIONAL CHANGE

This unit has been modified to include a Transponder P2 on-off switch.

The DME P2 switch now controls both DME P2 and Transponder P2 on-off functions.

Service bulletin to follow.

NOTICE OF OPERATIONAL CHANGE

This unit has been modified to include a lock-unlock indicator for the frequency synthesizer.

When the synthesizer comes unlocked the upper left vertical segment of the left most display digit will light. This light may come on momentarily when the unit is turned on or when the frequency of the unit is changed. The unit should not be operated if this light stays on or flickers continuously.

Service bulletin to follow.

SQUAWK NAUT
CHECK LIST

S/N

410

Date Finaled

7-10-79

Attenuator S/N

141 (ARRA)

Finaled By

John R. Cation

Isolator S/N

353

0. ☒ A. Check Regulator Voltages
☒ B. Check Card Rack Ground Voltage
80 mv max.

1. Readout Units and Decimal Points

<u>POSITION</u>	<u>UNITS</u>	<u>D.P.</u>
<input checked="" type="checkbox"/> A. XPDR % Return	%	----
<input checked="" type="checkbox"/> B. Δf	MHz	X.XX
<input checked="" type="checkbox"/> C. Squitter Rate	PPS	----
<input checked="" type="checkbox"/> D. Interro. Rate	PPS	----
<input checked="" type="checkbox"/> E. Acc.	FPS	----
<input checked="" type="checkbox"/> F. Vel.	KTS	----
<input checked="" type="checkbox"/> G. Test Dist.	NMi	XXX.XX
<input checked="" type="checkbox"/> H. Meas. Dist.	NMi	XXX.XX
<input checked="" type="checkbox"/> I. Power	WTS	----

2. Acc. Reg. Loading, Clearing and Readout

- ☒ A. Acc. Reg. Loads and displays the value determined by the F.P. Distance - Velocity - Acceleration Switch upon command of the F.P. Acc Load Switch
☒ B. Acc Reg clears to zero upon command of F.P. Acc. Clear switch
☒ C. Contents of the Acc. Reg. are zero upon Power Turn On

3. Vel. Reg. Loading, Clearing and Readout.

- ☒ A. Vel. Reg. Loads and displays the value determined by the F.P. Distance - Velocity - Acceleration switch upon command of the F.P. Vel. Load Switch

- 11 B. Vel. Reg. Clears to zero upon command of F.P. Vel. Clear Switch
- 11 C. Contents of the Vel. Reg. are zero upon Power Turn On
4. Dist. Reg. Loading, Clearing and Readout
- 11 A. Dist. Reg. Load and displays the value determined by the F.P. Distance - Velocity - Acceleration switch upon command of the F.P. Dist. Load Switch.
- 11 B. Dist. Reg. Clears to zero upon command of F.P. Vel. Clear switch.
- 11 C. Contents of the Dist. Reg. are zero upon Power turn on.
5. Acc. Rate Gen.
- 11 A. Acc. Rate changes as the contents of the Acc. Reg. changes
- 11 B. With 200 FPS loaded, read 118 PPS.
6. Vel. Rate Gen.
- 11 A. Vel Rate changes as the contents of the Vel. Reg. change
- 11 B. With 2000 kts. loaded, ready, 55 PPS.
7. Vel. Increase Control
- 11 A. Vel. increases to 4000 KTS and halts
8. Vel. Decrease Control
- 11 A. Vel decreases to 0 KTS and halts
9. Vel ARINC P.O. Control
- 11 A. Vel increments to 0 KTS, then to larger values
- 11 B. Contents of the Acc. Reg. clears to zero when Vel reaches 200 KTS
10. Negative Acc. Indicator
- 11 A. Minus sign appears - to indicate negative Acc. when Vel control is placed in decrease position
11. Distance Inbound Control
- 11 A. Distance decreases to 0 NMi and halts

12. Distance Outbound Control

- ☒ A. Distance increases to 399.99 NMi and halts

13. Distance Auto Control

Direction of distance incrementation reverses at

- ☒ A. 0 NMi ☒ C. 199.99 NMi ☒ E. 399.99 NMi
☒ B. 99.99 NMi ☒ D. 299.99 NMi

14. Measured Dist. Readout

- ☒ A. Data from DME UT displayed on readout when readout selector is placed in Meas. Dist. position.
☒ B. Serial Data Receivers accept as a High Level Voltage a voltage greater than 10V
☒ C. Serial Data Receivers accept as a Low Level Voltage a voltage less than 1V

15. Negative Velocity Indication

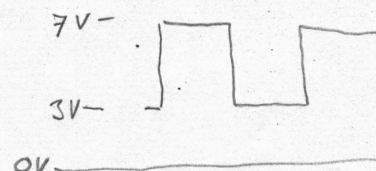
- ☒ A. Minus sign appears when the Direction control is in the Inbound position

16. Indicator U.T. Serial Data Clock Freq. Pin T pa Jack J4 (baksida)

- ☒ A. Clock Freq. is 11 ± 0.5 Khz in 11 Khz position
☒ B. Clock Freq. is 7 ± 1 Khz in 7 Khz position
☒ C. Clock Freq. is $15 \pm$ Khz in 15 Khz position

17. Indicator U.T. Serial Data Clock Driver Output

- ☒ A. Low Driver Level is 3 ± 0.2 Volts
☒ B. High Driver Level is 7 ± 0.2 Volts
☒ C. Rise time is 1-10 usec
☒ D. Fall time is 1-10 usec



18. Indicator U.T. Serial Date Sync. Driver Output

Pin 5 pin Jack J4

- ☐ A. Low Driver Level is 3 ± 0.2 Volts
- ☐ B. High Driver Level is 7 ± 0.2 Volts
- ☐ C. Rise time is 1-10 usec
- ☐ D. Fall time is 1-10 usec

19. Indicator U.T. Serial Data Driver Output

Pin 13 Jack J4

- ☐ A. Low Driver Level is 3 ± 0.2 Volts
- ☐ B. High Driver Level is 7 ± 0.2 Volts
- ☐ C. Rise time is 1-10 usec
- ☐ D. Fall time is 1-10 usec

20. Indicator U.T. Flag Alarm Driver Output

Pin 6 Jack J4

- ☐ A. Flag alarm voltage is 1 ± 0.2 volts when control is placed in the Flag position and 18.5 ± 0.2 volts when returned to normal position.

21. Indicator U.T., Distance, Flag and Dash Indications

- ☐ A. Indicator U.T. displays same distance as displayed by S/N Readout when in Test Distance position
- ☐ B. Indicator U.T. Blanks or displays a Flag when the Flag control is placed in the Flag position and the S/N readout selector is in the Test Dist. position
- ☐ C. Indicator U.T. displays Dashes when the Dash control is placed in the Dash position and the S/N readout selector is in the Test Dist. position.

22. Analog P.P. Control

- ☐ A. In Analog P.P. position on R.F. pulse pair is originated by the Initial Delay Logic
- ☐ B. Repetition rate is 10-15 per sec.

23. Analog Pulse Pair Driver Output

- ☒ A. Low Driver level 3 ± 0.2 Volts
- ☒ B. High Driver level 7 ± 0.2 Volts
- ☒ C. Rise Time 3 usec max.
- ☒ D. Fall Time 7 usec max.
- ☒ E. Pulse duration 4-10 usec
- ☒ F. A pair of pulses appear each time an R.F. reply pulse pair is originated.
- ☒ G. Spacing between pulses is 50 usec plus the Distance Delay in X-Mode

24. Range Rate Driver Output

- ☒ A. Low Driver level 3 ± 0.2 Volts
- ☒ B. High Driver level 7 ± 0.2 Volts
- ☒ C. Rise Time 3 usec max.
- ☒ D. Fall Time 7 usec max.
- ☒ E. Pulse duration 4-10 usec
- ☒ F. A pulse appears each time distance delay is changed 0.01 Nmi

25. Interrogation P1-P2 Spacing

- ☒ A. P1-P2 Spacing over-ride is not present
- ☒ B. No reply pulses are present unless Interrogation pulse pair spacing is 12 ± 0.5 usec in X mode and 36 ± 0.5 usec in Y mode
- ☒ C. Acc. Clear causes P1-P2 Spacing Override

26. DME % Reply

- ☒ A. Ratio of replies to interrogations vary in accordance with the setting of the DME % Reply control.

27. Suppression Pulse Driver Output

- ☒ A. Low level driver output 0 volts
- ☒ B. High level driver output 18 ± 0.2 volts.
- ☒ C. Driver output goes to the high level 1-5 usec prior to the 10% level of the first pulse of Replay pulse pair or the P1 pulse of the XPDR Interrogation
- ☒ D. Driver output returns to 0 volts 8 usec after the 50% point of P2 pulse of the reply or 2 usec after the 50% point of the P3 pulse of the XPDR Interrogation.

28. Squitter Rate

- Jul R51 k0t9*
- ☒ A. Squitter Rate varies from 9500 ± 250 PPS to less than 800 PPS in Hi range in both the DME and XPDR Modes.
 - ☒ B. Squitter Rate varies from greater than 800 PPS to less than 100 PPS in both the DME and XPDR Modes.
 - ☒ C. Squitter rate accurate to ± 1 count to $\pm 0.5\%$
 - ☒ D. The pulse spacing is random in the DME Mode and regular in the XPDR Mode.

29. Generator Frequency Accuracy

- ☒ A. Generator Frequency within $\pm 0.001\%$ of assigned frequency.
- ☒ B. MHz Freq. Select
 - ☒ 1. Gen. Freq. increments in 1 MHz steps as 1 MHz Freq. Select is incremented
 - ☒ 2. Gen. Freq. increments in 10 MHz steps as 10 MHz Freq. Select is incremented
 - ☒ 3. Gen. Freq. increments in 100 MHz steps as 100 MHz Freq. Select is incremented

- ☒ C. Channel Freq. Select

Gen. Freq. is the assigned frequency for all Channel Freq. Select positions

☒ D. Remote Freq. Select

Gen. Freq. is the assigned frequency for all Remote Freq. Select positions

30. UNCAL Control ΔF Control and ΔF Readout Accuracy

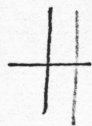
- ☒ A. In Uncal mode generator frequency variable by means of the ΔF Control
- ☒ B. ΔF control varies generator frequency at least ± 2 MHz from the assigned frequency.
- ☒ C. ΔF indicates within ± 0.01 MHz deviation of the generator frequency from the CAL Frequency

31. Generator Frequency Spectrum (DME)

- ☒ A. Generator frequency spectrum has no discrete spurious outputs at any level greater than 60db below the desired output level at any frequency up to 1920 MHz.
- ☒ B. Generator frequency spectrum does not display more than 30 KHz P.P. residual FM measured with a 1 KHz bandwidth
- ☒ 960 ☒ 1080 ☒ 1215
- ☒ C. Generator frequency spectrum at the -60db level is not broader than 300 KHz measured with a 1 KHz bandwidth
- ☒ 960 ☒ 1080 ☒ 1215
- ☒ D. Generator frequency spectrum does not display more than 50 KHz pulling due to modulation affects
- ☒ 960 ☒ 1080 ☒ 1215

32. R.F. CW Output Level Accuracy (DME)

- ☒ A. R.F. level does not vary more than 1 db over the frequency range of 962 MHz to 1213 MHz
- ☒ B. R.F. level is -10 ± 0.5 dbm at the -10 dbm attenuator setting for all freq. between 962 to 1213 MHz
- ☒ C. Level variation centered about -10 dbm.
- ☒ D. R.F. level attenuation below the -10 dbm level agrees with the attenuator dial setting to within ± 0.25 db or ± 0.004 (Dial Setting - 10 db whichever is greater.



- E. CW level available when the CW output control is placed in the ON position and the Mode Select Control is placed in the DME mode

33. Main Reply Pulse Level Accuracy



- A. Peak amplitude of the main reply pulses is within $\pm 0.1\text{db}$ of the CW output level

34. Tacan Mod. Control



- A. With Tacan Mod. Control ON, R.F. pulse amplitude is modulated by a composite 15 Hz and 135 Hz signal
- B. Each component has a modulation factor of 15% - 25%

35. Video Output Monitor



- A. Echo pulses appear when the Echo Injection control is in the "ON" position
- B. 0 db setting the Echo Pulse Pair Amplitude is within 0.1db of the Main Reply Amplitude.
- C. -6db setting the Echo Pulse Pair amplitude is $-6 \pm 0.5\text{db}$ below the Main Reply Amplitude
- D. Echo Pulse Pair occurs at a range of $30 \pm 1 \text{ NMi}$ in X Mode and $30 \pm 1 \text{ NMi}$ in Y mode
- E. Echo Pulse Pair spacing is $12 \pm 1 \text{ usec}$ in X Mode and $30 \pm 1 \text{ usec}$ in Y mode

37. R.F. ON-OFF Ratio



- A. RF CW level is at least 80 db below the RF Pulse peak amplitude between pulse intervals

38. Mode Select Control



- A. P1-P2 spacing in X position corresponds to X mode
- B. P1-P2 spacing in Y mode corresponds to Y mode
- C. P1-P2 spacing in the AUTO X-Y Mode corresponds to X Mode when Remote Frequency control is in X Mode or Channel Frequency select is in XXX.X0 or corresponds to Y Mode when Remote Frequency control is in Y Mode or Channel Frequency control is in XXX.X5

☒ D. In A, B, C, D, or A-C positions the XPDR Interro P1-P3 pulse spacing corresponds to that mode

☒ E. No pulses originated internally in EXT. position

39. P2 Deviation Control

☒ A. P1-P2 pulse spacing varies in accordance with the P2 Deviation Control

☒ B. 0 position on the control P1-P2 pulse spacing is 12 ± 0.1 usec in X mode and 30 ± 1 usec in Y mode

☒ C. With control set at ± 4 usec the deviation is $\pm 4 \pm 0.3$ usec

☒ D. P2 Pulse is not present when the P2 ON-OFF Control is in the OFF position

40. Power Readout Accuracy

☒ A. Power Readout indicates zero power 0.4 usec after removal of the RF pulses

☒ B. When RF input is decreased by a factor of 10 the Power Readout indicates a value in the range of $(10 \pm 0.5)\%$ of the previous reading

☒ C. Power Readout is accurate to within ± 0.5 db when a 1 KW pulse is applied over the frequency range of 1025 MHz to 1150 MHz

41. Detected Output Monitor

☒ A. The detected pulse monitor displays the demodulated envelope of either the DME Interrogation Pulses or the XPDR Reply pulses

42. Scope Sync. Control

☒ A. With scope Sync. Control in the TO position there is a pulse present on the scope Sync. Output which is synchronous with the DME Interrogation P1 pulse or the XPDR Interrogation P1 pulse

☒ B. In the squitter position the sync. pulse is synchronous with each DME Squitter Pulse, Reply pulse, Ident Pulse, or the XPDR Interrogation P1 Pulse

☒ C. In the TD position the sync. pulse is synchronous with the DME Reply pulse or the XPDR Interrogation P3 pulse.

43. Interrogation Rate Readout Accuracy

- ☒ A. Interro Rate Readout indicates to within ± 1 count the true DME Interro Rate

44. Range Delay Accuracy

- ☒ A. The Demodulator 50% Det. is set for 2 ± 0.05 usec delay *Pin 3, 4 pi Dem.*
☒ B. The Modulator 50% Det. is set for 2 ± 0.05 usec delay *Pin 34 pi Mod. Trig pi Det. pulse monitor*
☒ C. Zero NMI delay accurate within ± 0.04 NMI
☒ D. Range Delay accurate within ± 0.005 NMI per 100 NMI plus the zero NMI delay

45. -1 NMI Control

- ☒ A. Range decreases by 1 NMI when the -1 NMI switch is activated
☒ B. "-1NMI" appears in readout when switch is activated.

46. Pulse Priority

- ☒ A. Pulses have the following priority: Ident pulses, reply pulses, and squitter pulses
☒ B. Squitter pulses are inhibited so that they do not occur closer than 50 usec of the reply pulses

47. Ident Control and Equalizing Pulse Control

- ☒ A. When the Ident. Control is placed in the Ident. position the code KID is generated *Kolla Scope sync. out @ Video out monit. Upptviter oreg. bundet nagra sek. Seda for vinnar*
☒ B. When placed in the Tone position a continuous string of pulses appear
☒ C. Repetition rate of the pulses is 1350 PPS
☒ D. When the Equalization Pulse control is placed in the ON position a pulse pair appears 100 ± 10 usec after each Ident. pulse pair.
☒ E. At least a 5 sec interval between Ident Code cycles

48. Flag Alarm Level

- ☒ A. When the voltage on Flag Alarm Receiver input is 1.0 volt or less the Readout Blanks in the Meas. Dist. Mode.

49. Frequency Monitor Output



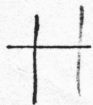
- A. At the Freq. Monitor output a beat frequency appears which is the difference between the Generator frequency \pm MHz and the DME Transmitter frequency
- B. In the XPDR mode the beat frequency is the difference between the Generator frequency ± 60 MHz and the XPDR Transmitter frequency.

50. Calibrate Phase Control and Cal. Output



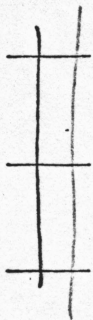
- A. With the Calibrate Phase Control in the 1.45 usec position there appears 1.45 usec pulse at the Cal. output
- B. Any delay can be overlaid by means of either a rising or falling edge of the 1.45 usec pulse
- C. A 1.0 usec phase variable pulse appears in the 1.0 usec position

51. XPDR Pulse Level



- A. Peak amplitude of the XPDR Interrogation P1 pulse is within ± 0.1 db of the CW output level

52. XPDR P2, P3 Suppression Control



- A. XPDR P2, P3 Pulse level varies with position of XPDR suppression control
- B. 0db setting, peak amplitude is within ± 0.1 db of the CW output level
- C. At the -6db setting the amplitude is -6 ± 0.3 db below the CW output level

53. XPDR Pulse Width Control



- A. The XPDR RF Pulse width is ± 0.025 usec of the setting of the control

54. XPDR P2 Deviation Controls



- A. The P1-P2 spacing is within ± 0.025 usec of the setting of the XPDR P2 control

55. XPDR P3 Deviation Control and Interrogation Modes



- A. The P1-P3 spacing is within ± 0.025 usec of the setting of the XPDR P3 control

- ☒ B. 8 us A mode
- ☒ C. 17 us B mode
- ☒ D. 21 us C mode
- ☒ E. 25 us D mode
- ☒ F. A-C mode there are three A-mode interrogations to one C-mode interrogation
- ☒ G. EXT. mode no XPDR interrogations

56. XPDR Double Interrogation Control

- ☒ A. With double interrogation ON-OFF control in the ON position there follows each XPDR Interrogation a second Interrogation
- ☒ B. Double Interrogation Control varies the delay of these pulses from 20-25 usec to 250-270 usec after P3

57. XPDR % Return Readout

- ☒ A. The ratio of XPDR returns to Interrogations is accurate to within \pm count

58. Remote Operation

- ☒ A. When Frequency Sel. Control is in Remote, the Generator Freq. is determined by the inputs to the rear connector only
- ☐ B. When Remote Control is placed in ALL Remote position all functions listed are controllable from the rear connectors.

59. XPDR Spectrum

- ☒ A. At RF output, the spectrum is within the following limits:
 Peak at -7db
 \pm 10MHz at -42db
 \pm 20 MHz at -52db
 \pm 30 MHz at -57db

60. XPDR Spurious Pulse

- ☒ A. Video output of XPDR has no detectable pulses at 1150 MHz and at 970 MHz pulse are less than 100m volt

61. XPDR Rise Time

- ☒ A. At output of EMI filter, the rise time is 50-100 nsec
- ☒ B. At output of EMI filter, the fall time is 50-200 nsec

62. Regulator Voltage Accuracy

Reg.	Output Voltage Range	120V	100V	Ripple @100V
A. 28V	28±0.05V	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
B. +16V	16± 0.20V	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
C. +10V	+10 ± 0.05V	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D. +5V	+5 ± 0.05V	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
E. -5V	-5 ± 0.20V	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
F. -10V	-10 ±0.20V	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
G. -28V	-28 ± 0.30V	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
H. +16±2V	+16 ± 2V	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

63. Environmental Record

1. 7 day Burn

Start 7-2-79
Stop 7-9-79

2. Timer On-Off

Start 7-9-79
Stop 7-10-79

CHECK LIST

1. With the Freq. Gen. Channelled to 960 MHz the ΔF VCO VT voltage is in the range of 0.95 to 1.00 volts.

+ ΔF

- ΔF

2. With the Freq. Gen. Channelled to 1230 MHz the ΔF VCO VT changes by $+0.3 \pm 0.05$ volts when the ΔF VCO ΔF line is shorted and recovers immediately when the short is removed.

+ ΔF

- ΔF

3. The Master VCO RF output is at least +21 dbm and flat to within 1 db over the frequency range of 960 to 1220 MHz

The Master VCO VT is in the range of 15 to 17 Volts when the freq. is 1200 MHz

With the Master VCO VT shorted to ground the freq. is less than 900 MHz

4. The delay between the 0.5 Amplitude point on the rising edge of the P1 pulse, as observed at the Video Output Monitor, and the falling edge of the pulse on the Mod 50% Level Pulse line, G18-34, may be varied by means of the Mod 50% level pot over the range of 2.0 ± 0.2 usec.

5. The leads of the ΔF Osc. transistor, Q1, may be mechanically probed without causing loss of "lock."

6. Is the EMI Filter Capacitor correctly installed

7. Lock-Unlock Indicator Modification.

The upper left vertical segment of left digit should light momentarily when Squawk Naut channelled.

8. AFTER P2 On Off Modification

P2 On-Off switch also controls Transponder P2 on-off function

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Due to the complexity of the SQUAWK/NAUT I, a simple reference designator has been assigned to each assembly or major component. The following list has been prepared as a quick cross reference, listing reference designators, KPN of the schematic, a description for the reference designator and which section of the manual that item may be found.

REF.	LOCATED ON SCHEMATIC P/N	DESCRIPTION	P/O SECTION
B1	002-0095-00	POWER SUPPLY	F.P. & PWR. SUPPLY
B2	002-0095-01	" "	" " "
B3	002-0095-02	" "	" " "
C1	002-5053-00	CARD 1	VIDEO
C2	002-5054-00	CARD 2	"
C3	002-5055-00	CARD 3	"
C4	002-5056-00	CARD 4	"
C5	002-5057-00	CARD 5	"
C6	002-5058-00	CARD 6	"
C7	002-5059-00	CARD 7	"
C8	002-5060-00	CARD 8	"
C9	002-5061-00	CARD 9	"
C10	002-5062-00	CARD 10	"
C11	002-5063-00	CARD 11	"
F.P.	002-0094-00	FRONT PANEL	F.P. & PWR. SUPPLY
G1	002-5077-00	LOW FREQ LOOP	FREQ. GEN.
G2	002-5082-00	91 MHz, OSC.	" "
G3	002-5082-01	89 MHz, OSC.	" "
G4	002-5078-00	HIGH LOOP BD.	" "
G5	002-5081-00	+ Δ F VCO	" "
G6	002-5081-00	- Δ F VCO	" "
G7	002-5081-00	MASTER VCO	" "
G8	002-5064-00	ISOLATOR	R.F.
G9	002-5064-00	ISOLATION LPF	"
G10	002-5064-00	R.F. MODULATOR	"
G11	002-5064-00	LEVELING LPF	"
G12	002-5064-00	LEVELING COUPLER	"
G13	002-5073-00	SNIFFER	"
G14	002-5073-00	ATTENUATOR	"
G15	002-5073-00	POWER COUPLER	"
G16	002-5073-00	INPUT PAD	"
G17	002-5064-00	LEVELING DETECTOR	"
G18	002-5076-00	MODULATOR	"
G19	002-5080-00	FREQ. MONITOR	"
G20	002-5073-00	POWER PAD	"
G21	002-5073-00	POWER DETECTOR	"
G22	002-5073-00	ULTIMATE LPF	"
G23	002-5073-00	DEMODULATOR	"
G24	002-5083-00	Δ F VFO	FREQ. GEN.
G25	002-5064-00	EMI FILTER	R.F.
L1	002-5079-00	READOUT DRIVER LOGIC	VIDEO
L2	002-5075-00	READOUT CONTROL LOGIC	"
L3	002-5074-00	FREQ. CONTROL LOGIC	FREQ. GEN.

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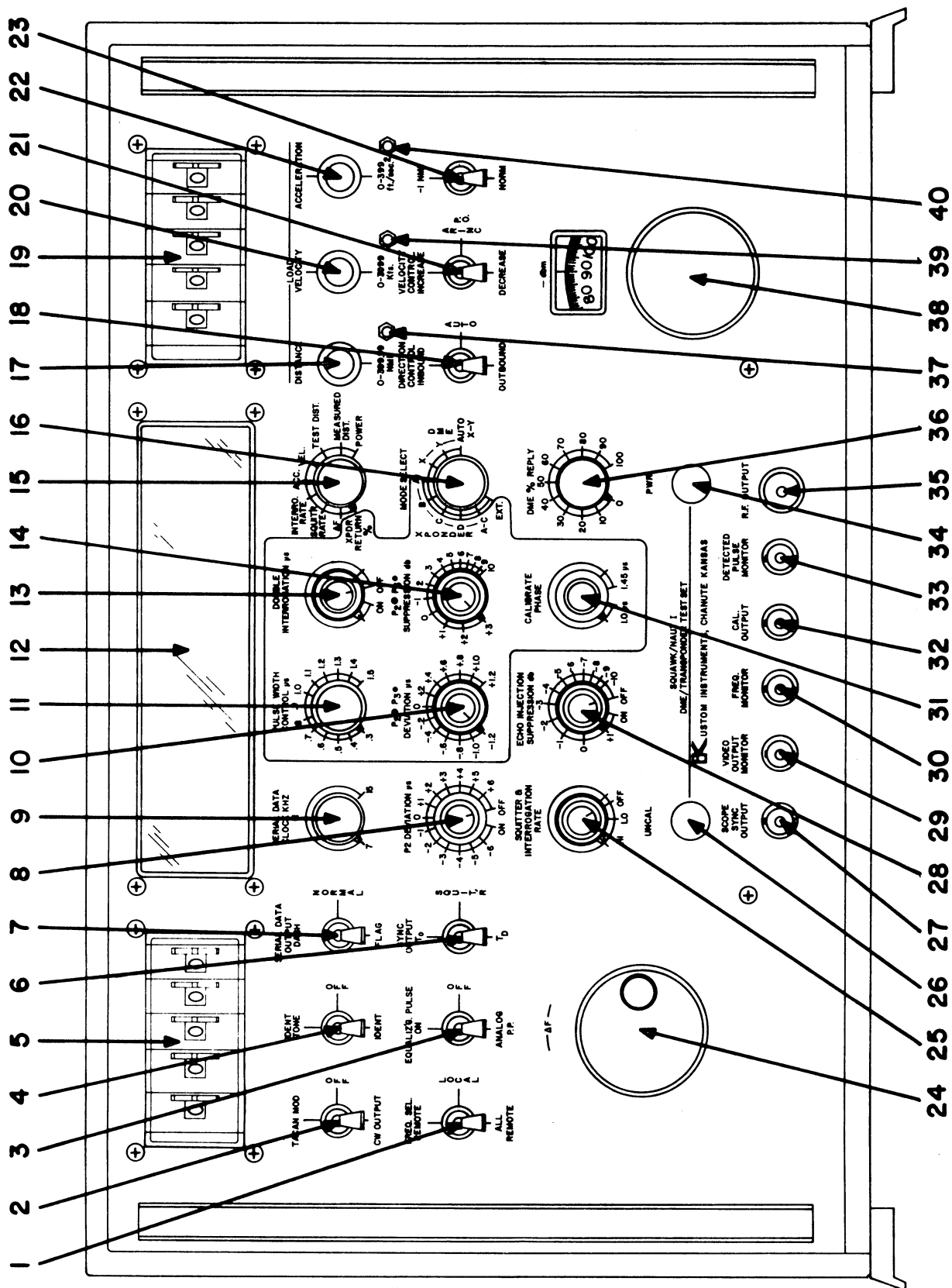


FIGURE I-SQUAWK/NAUT I
FRONT PANEL VIEW

OPERATION

GENERAL

The KUSTOM INSTRUMENTS SQUAWK/NAUT I Test Set is designed for testing and calibrating DME (Distance Measuring Equipment), ATC (Air Traffic Control) Transponder aircraft equipment and ARINC 568 Digital DME Indicators. The system is completely self-contained, providing all necessary functions.

CONTROLS AND INDICATORS

A front view of the Test Set with controls (numbered) is shown in Fig. 1.

1. REMOTE-LOCAL

A. FREQUENCY SELECT REMOTE position

Allows the Test Set frequency to be selected remotely by means of Remote Control Jack, J1, inputs. Remote Frequency Selector inputs are enabled. Internal Frequency Selector is disabled.

B. LOCAL position

All functions are controllable by the front panel controls. Remote Frequency Selector inputs are disabled.

C. ALL REMOTE positions

Allows most functions to be remotely controlled. All appropriate front panel controls are disabled. See Remote Control Section.

2. TACAN MOD-CW OUTPUT

A. TACAN MOD position

Adds 15 and 135 cycle modulation to the RF Output to simulate a TACAN station. Reference groups are not included.

B. OFF position

Permits normal Transponder or non-TACAN DME signal to be selected.

C. CW OUTPUT position

When in the DME MODE, this position provides a calibrated CW output at the RF Output jack.

3. EQUALIZING PULSE-ANALOG PULSE PAIRS

A. EQUALIZING PULSE ON position

Adds Equalization Pulses to DME Ident Tone/Code.

B. EQUALIZING PULSE OFF position

Removes Equalization Pulses from Ident Tone/Code.

C. ANALOG PULSE PAIR position

Causes DME Reply Pulse Pairs and Analog Distance Pulse Pairs at a 10-15 PPS rate. Test Set will not Reply to DME Interrogations in this condition. This position is useful with Area Nav. equipment, consult instruction manual. Analog Distance Pulse accurate in X Mode only.

4. IDENT

A. TONE position

Enables 1350 Hz. CW tone

B. OFF position

Disables Ident Tone/Code

C. IDENT position

Enables keyed identifier at 5 sec. intervals. Code is KID.

5. CHANNEL FREQ/MHZ FREQ SECLECTOR

The right most Selector switch has three positions- 0, 5, and MHz. When in the MHz position, MHz Freq. Selector operation allows the selection of any DME or Transponder frequency in the range of 960 to 1215 MHz in 1 MHz steps. When in the 0 or 5 position Channel Freq. Selector operation allows the selection of DME paired VOR/ILS/VHF channels. The 0 or 5 position allows the selection of X or Y DME channels. If the Mode Selector (16) is in the Auto X-Y position the Test Set pulse coding automatically corresponds to X or Y.

6. SYNC OUTPUT

A. To position

Provides Sync Output at P1 in Transponder Mode and the first pulse of DME Interrogation in DME Mode. If the DME Suppressor Output is applied through the Remote Control Jack, J3-V, Sync Output occurs at the leading edge of Suppressor Pulse.

B. SQUITTER position

Provides Sync Output coherent to DME Squitter and Reply Pulses.

C. Td position

Provides Sync Output at P3 in Transponder Mode and first pulse of the Reply in DME Mode.

7. SERIAL DATA OUTPUT

Modifies the Serial BCD Distance Data Output used to drive a remote ARINC 568 Digital DME Indicator.

- A. DASH position
 - Generates the No Computed Data indication on the Serial BCD Distance Data Output to produce "DASH" readout on a Digital DME Indicator.
- B. FLAG position
 - Causes a Flag to be displayed on a Digital DME Indicator.
- C. NORMAL position
 - Allows normal operation of Digital DME Indicator.
- 8. P2 DEVIATION
 - A. Outer knob
 - Permits deviation of DME Pulse Coding by +6 usec. from nominal X or Y pulse coding.
 - B. Inner Knob
 - Removes the DME P2 Pulse in the OFF position.
- 9. SERIAL DATA CLOCK
 - Controls Serial Data Clock Rate to remote Digital DME Indicator. Rate is controllable from 7 KHz to 15 KHz.
- 10. P2-P3 DEVIATION
 - A. Inner knob
 - Permits a +1.2 usec. position change of P3 with respect to P1.
 - B. Outer knob
 - Permits a +1.2 usec position change of P2 with respect to P1.
- 11. PULSE WIDTH
 - Permits the Transponder Interrogation Pulse Width to be varied over a range of 0.3 usec to 1.5 usec.
- 12. READOUT
 - The Readout displays information as selected by the READOUT SELECTOR (15).
- 13. DOUBLE INTERROGATION
 - A. Inner knob, ON-OFF
 - ON position enables the Double Interrogation.
 - B. Outer knob, Delay
 - Controls the delay of the second (Double) Transponder Interrogation as referenced to the P3 pulse of the first (Initial) Interrogation. The delay is continuously variable over the range of 25 usec. to 250 usec.

CAUTION: When the Double Interrogation Delay is less than 25 usec and the RF Attenuator (38) is set for high signal levels it is possible for the XPDR Reply to cause the Test Set Interrogation to become incorrect.

14. P2-P3 SUPPRESSION

A. Inner knob

Varies the amplitude of the Transponder Interrogation P3 Pulse with respect to the P1 Pulse from +3 db to -10 db.

B. Outer knob

Varies the amplitude of the Transponder Interrogation P2 Pulse with respect to the P1 Pulse from +3 db to -10 db.

15. READOUT SELECTOR

A. XPDR % RETURN position

Readout displays Transponder Returns directly in percent of Transponder Interrogations.

B. \triangle F position

When operating Test Set in UNCAL mode, the Readout displays the Frequency Deviation with respect to the selected frequency.

C. SQUITTER RATE position

Readout displays the DME Squitter Rate or the Transponder Initial Interrogation Rate as selected by SQUITTER AND INTERROGATION RATE control (25).

D. INTERRO RATE

Readout displays the DME Interrogation Rate. Can be used to determine Transponder Reply Rate but may be misleading under short delay Double Interrogation conditions.

E. ACC position

Readout displays the Test Set Acceleration or Deceleration in FT./Sec.²

F. VELOCITY position

Readout displays the Test Set Velocity, positive or negative in Knots.

G. TEST DISTANCE position

Readout displays Test Set Distance in Nautical Miles.

H. MEASURED DISTANCE position

Readout displays the Serial BCD Distance Data input to the Test Set from the DME U.T.

I. POWER position

Readout displays the DME or Transponder Peak Pulse Power from 50 watts to 3 kw. When switch is placed in POWER position the Test Set Distance and Velocity are zero. Upon completion of Power measurement, a Velocity or Distance other than zero must be reprogrammed into the Test Set if desired.

16. MODE SELECTOR

A. EXT position

Inhibits any pulses of internal origin. An external source may generate pulse combinations other than those generated internally.

B. A-C position

Automatically interlaces Mode A and Mode C Transponder Interrogations.

C. D position

Selects Transponder Mode D Interrogations.

D. C position

Selects Transponder Mode C Interrogation

E. B position

Selects Transponder Mode B Interrogations.

F. A position

Selects Transponder Mode A Interrogations.

G. X position

DME X Channel pulse coding is selected.

H. Y position

DME Y Channel Pulse coding is selected.

I. AUTO X-Y position

DME X or Y channel pulse coding is selected by the Frequency Selector. MHz Freq Selector operation causes X Channel pulse coding.

17. DISTANCE LOAD

Loads the Test Set Distance Register with information selected by the Register Load Value Control (19).

18. DIRECTION CONTROL

A. INBOUND position

Selects Inbound Direction of Distance change. When Distance reaches zero miles, Velocity and Acceleration become inoperative and Test Set will remain at zero NMi. (Negative Velocity)

B. OUTBOUND position

Selects Outbound Direction of Distance change. Test Set Distance will stop at 399.99 NMi.
(Positive Velocity)

C. AUTOMATIC position

Allows Test Set to cycle between 0 and 99.99. If the Test Set Distance is greater than 99.99 and traveling outbound when the switch is placed in the AUTO position, the Test Set will proceed Outbound to the next 100 mile increment (199.99 or 299.99 NMi.) turn around and proceed to zero miles. Thereafter, the excursion will be between 0 and 99.99 nautical miles.

19. DISTANCE-VELOCITY-ACCELERATION REGISTER LOAD VALUE

Used to select Distance of 0-399.99 Nautical Miles in .01 Nautical Mile increments.

and

selects Velocity of 0-3000 knots in 1 knot increments

and

selects Acceleration of 0-399 Ft./sec². in 1 Ft/sec².

20. VELOCITY LOAD

Loads the Test Set Velocity Register with information selected by the Register Load Value Control (19).

21. VELOCITY CONTROL

A. INCREASE position

Selects a Velocity Increase should the Test Set be programmed for an Acceleration Velocity will Increase to 4000 KTs.

B. DECREASE position

Selects a Velocity Decrease should the Test Set be programmed for an Acceleration. Velocity will Decrease to 0 KTs.

C. ARINC PASS-OVER position

This position allows the simulation of a 200 knot station passover. Select any Distance, such as 50 miles, and 200 knots Velocity. Place the Velocity Control in the Decrease position and then in the ARINC PASS-OVER position. The simulation is initiated by loading an Acceleration of 338 Ft./sec². Upon loading the Acceleration the Velocity will decrease from 200 knots to 0 knots and then increase back to 200 knots in 2 seconds. At this time the Acceleration Register is reset to 0 FPS². This procedure will accomplish a smooth 400 knot change in Velocity in a two second interval.

22. ACCELERATION LOAD

Loads the Test Set Acceleration Register with information selected by the Register Load Value Control (19).

23. -1 NMI/NORMAL

A. NORMAL position

Provides DME Distance as programmed into Distance Register.

B. -1 NMI position

Causes the actual Distance delay to be 1 NMI less than that programmed into the Test Set or displayed by the Readout (12).

24. ΔF

Permits the Test Set frequency to be varied over a range of at least ± 4 MHz from the selected frequency. This control is only operative when the Test Set is in the UNCAL mode.

25. SQUITTER AND INTERROGATION RATE

Provides Squitter Rate control in DME Mode and Interrogation Rate in Transponder Mode.

A. Inner knob

Selects Hi or Lo Range or "OFF"

Hi Range 1,000 - 10,000 PPS.

Lo Range 100 - 1,000 PPS.

B. Outer knob

Provides continuously variable adjustments of the Squitter/Interrogation Rate within range selected.

26. UNCAL

The UNCAL push button allows the frequency to be changed by the ΔF control (24). The pushbutton will be lit when the Test Set is in the UNCAL Mode.

27. SCOPE SYNC OUTPUT

Provides Scope Sync pulses selected by SYNC OUTPUT switch (6).

28. ECHO INJECTION SUPPRESSION

A. Outer knob

Controls the level of the DME Echo with respect to the main pulse level over the range of ± 1 to -10 db. Echo Injection is at approximately 30 NMI.

B. Inner knob

OFF position causes removal of Echo pulses.

29. VIDEO OUTPUT MONITOR

Provides a replica of the detected RF Pulse originating from the Test Set.

30. FREQUENCY MONITOR
Beat frequency output derived from a DME or Transponder pulse and the Test Set Generator Frequency ± 63 or 60 MHz in DME or Transponder Mode respectively. Allows frequency measurements of DME and Transponder pulses by observing zero beat on scope.
31. CALIBRATE PHASE
A. Inner knob
Selects time marker pulses with 1.0 usec or 1.45 usec spacing.
B. Outer knob
Varies phase of time marks pulses.
32. CAL OUTPUT
1.0 usec or 1.45 usec time marker pulse output.
33. DETECTED PULSE MONITOR
Allows monitoring of DME or Transponder video.
34. POWER
This combination power switch and indicator applies power to the Test Set when depressed. Depress button completely a second time to turn off.
35. RF OUTPUT
Connects RF signals to DME and ATC equipment
36. DME % REPLY
Controls Test Set Reply Efficiency. Adjustable from 0% to 100% in 10% increments.
37. DISTANCE CLEAR
Resets the Test Set Distance Register to 0 NMI.
38. ATTENUATOR
The RF Attenuator allows continuously variable signal levels from -10 dbm to -110 dbm.
39. VELOCITY CLEAR
Resets the Test Set Velocity Register to 0 Knots.
40. ACCELERATION CLEAR
Resets the Test Set Acceleration Register to 0 FPS².
Causes the Test Set pulse decoder to become inoperative thus allowing the Test Set to Reply to DME Interrogations which have a pulse coding not in the range of 12 ± 0.5 usec or 36 ± 0.5 usec.

OPERATING INSTRUCTIONS

DME

The following procedure is a typical set-up for DME equipment. Reference should be made to the DME manufacturer's instruction manual covering the particular equipment under test for complete test procedures.

- A. Turn on the SQUAWK/NAUT Test Set and allow a 5-10 minute warmup period.
- B. Connect the DME antenna coax to the SQUAWK/NAUT RF Output connector (35).
- C. Connect the scope sync cable to the SCOPE SYNC OUTPUT connector (27).
- D. Set SQUAWK/NAUT controls as listed below, referring to Fig. 1 for location of controls.
 1. POWER (34) "ON" (button lit)
 2. OUTPUT LEVEL (38) -50 dbm
 3. TACAN MOD (2) As desired, in either "OFF" or TACAN MOD. position.
 4. REMOTE—LOCAL (1) As necessary with equipment being tested. Refer to Controls and Indicators Section for detailed description of function.
 5. CHANNEL FREQ./MHz FREQUENCY SELECTOR (5) Set to desired frequency by choosing appropriate VOR/ILS/VHF channels if LOCAL in (4) above is selected.
 6. UNCAL (26) Set to CALIBRATE position (light "OFF").
 7. ΔF (24) Not operable.
 8. MODE SELECTOR (16) Place in AUTO X-Y position.
 9. READOUT (12) & READOUT SELECOR (15) READOUT SELECTOR (15) may be positioned as necessary to verify control settings as they are adjusted (ACC., VELOCITY, TEST DISTANCE, SQUITTER RATE, ETC.)
 10. SYNC OUTPUT (6) Set as desired, referring to Controls and Indicators Section for detailed description of function.
 11. SQUITTER AND INTERROGATION RATE (25) Inner knob to HI. Outer knob set to 2700, as read on READOUT (12) with READOUT SELECTOR (15) in Squitter Rate position (2700 PPS).
 12. ECHO INJECTION (28) Inner knob to "OFF" position. Outer knob is then inoperative.
 13. IDENT (4) OFF position
 14. EQUALIZING PULSE (3) OFF position

15. P2 DEVIATION (8) Inner knob to "ON" position. Outer knob to +0.
16. DME % REPLY (36) As desired (70-100%)
17. DISTANCE LOAD (17) Any desired Distance, such as 050.00 (50Nmi.) may be dialed into Register Load Value (19) and loaded into the Distance Register by pushing DISTANCE LOAD pushbutton (17). This distance may be verified by selecting TEST DISTANCE position of READOUT SELECTOR (15).
18. VELOCITY LOAD (20) Any desired Velocity, such as 00175 (175 knots) may be dialed into Register Load Value (19), and loaded into the Velocity Register by pushing VELOCITY LOAD pushbutton (20). This VELOCITY may be verified by selecting VELOCITY position of READOUT SELECTOR (15) or TEST DISTANCE position of READOUT SELECTOR (15). In VELOCITY position 175 Knots will be displayed, while in DISTANCE position the distance will be changing at 175 Knot rate either Inbound or Outbound as determined by DIRECTION CONTROL (18).
19. ACCELERATION LOAD (22) Any desired Acceleration, such as 00100 (100 Ft./Sec²) may be dialed into the Register Load Value (19) and loaded into the Acceleration Register by pushing ACCELERATION LOAD pushbutton (22). This Acceleration may be verified by selecting ACCELERATION position of READOUT SELECTOR (15). Readout will indicate 100 if VELOCITY CONTROL switch (21) is in INCREASE position (indicating Acceleration), or -100 if VELOCITY CONTROL switch (21) is in DECREASE position (indicating Deceleration.)

The effects of Acceleration may also be observed by selecting VELOCITY position of READOUT SELECTOR (15). VELOCITY will be increasing or decreasing as determined by VELOCITY CONTROL switch. "NORMAL" position.

20. -1 NMi/NORMAL (23)
- E. Turn on DME and select channel. DME should lock to Test Set signal. If the DME does not lock check for the presence of Test Set Replies by observing the Video Output Monitor (28)⁷⁹ place the Sync Output control (6) in the To position. There should be a Reply present with a rate equal to the Interrogation rate providing the DME % Reply Control (36) is set for 100%. If not present check to determine if Equalizing Pulse/Analog P.P. Control (3) is in OFF position. Depress the Acceleration Clear push-button (40) which causes the Test Set Interrogation pulse decoder to be inoperative. If this causes Replies to appear the DME U.T. pulse coding is not in the range of 12 ± 0.5 usec or 36 ± 0.5 usec.
- F. To check power output of DME, set READOUT SELECTOR (15) to POWER position and read Power in Watts on READOUT (12). When READOUT SELECTOR switch is in the POWER position the Test Distance and Velocity are zero. The DME will lock at 0 NMi. After the Power measurement is completed, it is necessary to reprogram the Distance, Velocity and Acceleration Registers if non zero values are desired. Power may be read in the DME track mode as described above or the DME % Reply (36) may be set to zero and the Power read in the search mode. Detected RF pulse output may be observed on a scope by monitoring the DETECTED PULSE MONITOR (33).
- G. To check frequency of DME transmitter.
1. Set READOUT SELECTOR (15) to ΔF position.
 2. Place Test Set frequency in UNCAL condition by pressing UNCAL button (26) (light will be lit in the UNCAL mode). Adjust ΔF Control (24) for 0.00 MHz ΔF as observed on READOUT (12).
 3. Check to determine that the DME is Interrogating the Test Set.
 4. Turn RF ATTENUATOR (38) to -10 dbm. This is necessary to assure sufficient DME transmitter signal input to the internal mixer.
 5. Connect scope vertical channel to FREQUENCY MONITOR connector (30) and scope sync to SCOPE SYNC OUTPUT connector (27). Scope should be adjusted to display both DME pulses.
 6. Set SYNC OUTPUT switch (6) to To.

By varying ΔF Control (24), a zero beat condition will be observed on the scope. DME transmitter frequency may then be determined by combining the Selected channel frequency and the plus or minus ΔF deviation on READOUT (12). By expanding scope display the frequency of each pulse on an individual basis may be read. This permits checking for any transmitter frequency pulling effects, etc.

TRANSPONDER

The following procedure is a typical set-up for Transponder equipment. Reference should be made to the Transponder manufacturer's instruction manual covering the particular equipment under test for complete test procedures.

- A. Turn on the SQUAWK/NAUT Test Set and allow a 5-10 minute warmup period.
- B. Connect the Transponder antenna coax to the SQUAWK/NAUT RF Output connector (35).
- C. Connect the scope sync cable to the SYNC OUTPUT connector (27).
- D. Set SQUAWK/NAUT controls as follows, referring to Fig. 1 for location of controls.
 1. POWER (34) "ON" (button lit)
 2. OUTPUT LEVEL (38) -50 dbm
 3. CW OUTPUT (2) "OFF"
 4. REMOTE-LOCAL (1) As necessary with equipment being tested. Refer to Controls and Indicators Section for detailed description of function.
 5. CHANNEL FREQ/MHz Set to 1030 MHz.
 6. UNCAL (26) Set to CAL. position (light "OFF").
 7. ΔF (24) Not operable.
 8. MODE SELECTOR (16) Place in Mode A,B,C,D, or A-C as desired.
 9. READOUT (12) & READOUT SELECTOR (15) Readout Selector (15) may be positioned as necessary (SQUITTER RATE, POWER, ΔF , XPDR RETURN %).
 10. SYNC OUTPUT (6) Set as desired referring to Controls and Indicators Section for detailed description of function.
 11. SQUITTER AND INTERROGATION RATE (25) Inner knob to LO. Outer knob set to 500, as read on READOUT (12) with READOUT SELECTOR (15) in SQUITTER RATE position (500 PPS. rate).
 12. PULSE WIDTH (11) Set to .8 usec
 13. P2-P3 DEVIATION (10) Both inner and outer knobs set to +0.
 14. P2-P3 SUPPRESSION Inner knob (P $\bar{3}$ Suppression) set to 0. Outer knob (P2 Suppression) set to -10 db.

15. DOUBLE INTERROGATION Inner knob to "OFF" position
(13)

- E. Turn Transponder on. Transponder should reply to Test Set Interrogations.
- F. To check transmitter power output of Transponder, set READOUT SELECTOR (15) to POWER position and read Power in watts on READOUT (12). Power droop and pulse shape may be observed on a scope by monitoring the DETECTED PULSE MONITOR (33).
- G. To check Transmitter frequency,
 - 1. Set READOUT SELECTOR switch (15) to ΔF position.
 - 2. Place Test Set RF generator in UNCAL condition by pressing UNCAL button (26) (Light will be lit in the UNCAL mode).
 - 3. Dial 1030 MHz on Channel Freq/MHz Freq. SELECTOR (5).
 - 4. Turn RF ATTENUATOR (38) to -10 dbm. This is necessary to assure sufficient Transponder signal input to the internal mixer. If this causes the Transponder to cease replying set the P2 Deviation Control (10) to +1.2 usec.
 - 5. Connect scope vertical channel to FREQUENCY MONITOR connector (30) and scope sync to SCOPE SYNC OUTPUT connector (27).
 - 6. Set SYNC OUTPUT switch to Td. Scope should be adjusted to display Transponder Reply.

By varying ΔF control (24), a zero beat condition will be observed on the scope. The transmitter frequency deviation from 1090 MHz may be read on READOUT (12).

H. To check Transponder Dead Time.

- 1. Place the inner knob of the Double Interrogation control (13) in the ON position.
- 2. Place the Readout Selector (15) in the XPDR & Return position.
- 3. Observe the Double Interrogation Delay by means of a scope attached to the Video Output Monitor. Place the Sync Output control (3) in the To position.
- 4. While varying the outer knob of the Double Interrogation control (13) observe both the Readout and the scope to determine the Delay at which the Transponder U.T. does not Reply to the second Test Set Interrogation.
- 5. By also observing the Detected Pulse Monitor on the scope it is possible to determine when the Transponder U.T. is not Replying to the second Test Set Interrogation.
- 6. Caution. When the Double Interrogation Delay becomes less than 25 usec. and the RF Attenuator (38) is set for high signal levels it is possible for the XPDR Reply to cause the Test Set Interrogations to be incorrect.

ARINC 568 DIGITAL DME INDICATOR

The following procedure is a typical set-up for Digital DME Indicator equipment. Reference should be made to the Indicator manufacturer's instruction manual covering the particular equipment under test for complete test procedures.

- A. Turn on the Squawk/Naut Test Set and allow a 5-10 minute warm-up period.
- B. Connect the ARINC 568 Digital DME Indicator to the Indicator U.T. Jack, J4, located on the Test Set rear panel. Apply 115 VAC, 400 Hz, to Remote Control Jack, J3, Pins AA and BB in order to power the Indicator from the Indicator U.T. Jack, J4, Pins W and X.

Refer to Indicator U.T. Jack, J4, Pin Assignment at the end of this section.

- C. Set the Squawk/Naut Controls as listed below, referring to Fig. 1 for location of Controls.

- | | |
|---|---|
| 1. POWER (34) | "ON" (button lit) |
| 2. SERIAL DATA
OUTPUT (7) | Normal position |
| 3. SERIAL DATA
CLOCK (9) | 11 KHz position |
| 4. READOUT (12)
& READOUT
SELECTOR (15) | Readout Selector (15)
may be set to either
Acceleration, Velocity,
or Test Distance positions
as required. When in the Test
Distance position the Readout
will indicate the Distance as
sent to the Indicator by the
Serial BCD Distance Data output. |

NOTE: The Indicator manufacturer's test procedures should be consulted and followed for complete Indicator Testing. By referring to the detail description of the Control functions, any particular characteristic of the Digital DME Indicator may be thoroughly tested.

Refer to the Indicator U.T. Jack, J4, Pin Assignment at the end of this section for such additional outputs as the Analog Distance Pulse and Range Rate Pulse. The Analog Distance Pulse output is accurate only if the Test Set is operating in X Mode. Refer to Remote Control Schematic in Remote Control section for wiring diagram.

REAR PANEL CONNECTING CABLES

INDICATOR U.T. JACK J4 PIN ASSIGNMENT

PIN	DESCRIPTION	CONNECTION
A.		
B.	SERIAL BCD DISTANCE DATA Hi	C10-A26
C.	" " " " Lo	Gnd
D.	5V INSTRUMENT LIGHTS Hi	
E.		
F.		
G.		
H.	SPARE	
J.	SPARE	
K.		
L.	ANALOG DISTANCE PULSE Hi	C10-A11
M.	ANALOG DISTANCE PULSE Lo	Gnd
N.	FUNCTIONAL TEST CONTROL	
P.	SPARE	
R.	SPARE	
S.	SERIAL BCD WORD SYNC Hi	C10-B31
T.	SERIAL BCD CLOCK Hi	C10-A2
U.	SERIAL BCD CLOCK Lo	Gnd
V.	5V INSTRUMENT LIGHTS Lo	Gnd
W.	26VAC 380-420 Hz	T2-4
X.	AC COMMON GROUND	T2-3
Y.	RANGE RATE PULSE Hi	C10-A8
Z.	" " " " Lo	Gnd
a.	SERIAL BCD WORD SYNC Lo	Gnd
b.	WARNING FLAG	C11-B30
c.	CHASSIS GROUND	Gnd

OPERATION: This connector is for use in check out of DME Indicator complying with ARINC Characteristic 568.

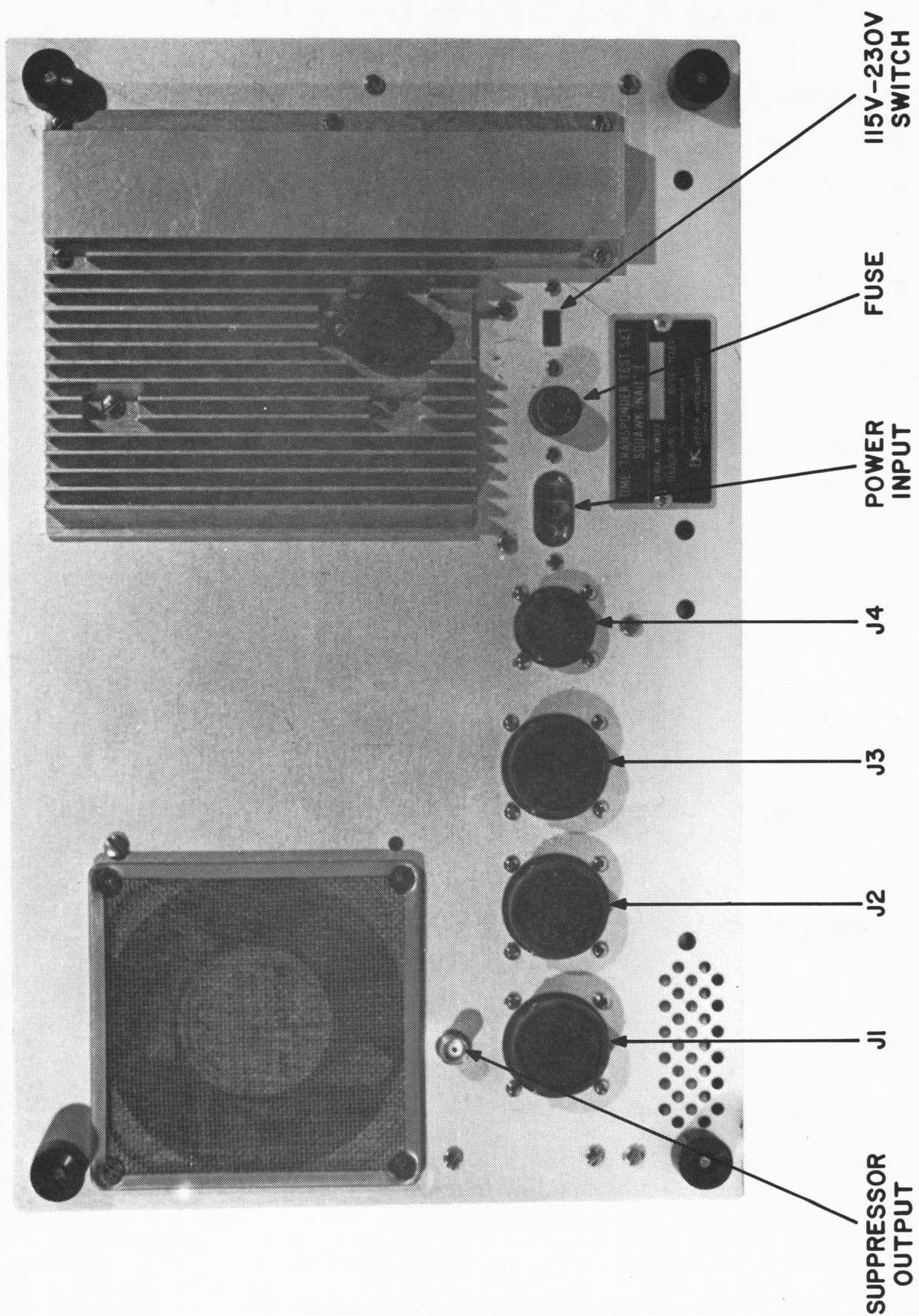


FIGURE 2-SQUAWK/NAUT I
REAR PANEL VIEW

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FREQUENCY GENERATOR

BLOCK DIAGRAM THEORY

PURPOSE:

To generate a +20 DBM minimum RF signal varying in frequency between 962 MHz and 1213 MHz with crystal controlled accuracy.

OPERATION:

A. $+\Delta F$ VCO AND $-\Delta F$ VCO LOOPS

Since the $+\Delta F$ VCO loop and the $-\Delta F$ VCO loop are identical, except for the use of an 89 MHz oscillator with the $-\Delta F$ VCO and a 91 MHz oscillator with the $+\Delta F$ VCO, only the $+\Delta F$ VCO loop shall be discussed.

The $+\Delta F$ VCO VT output of the LEAD/LAG AMPLIFIER which is controlled by the PHASE/FREQUENCY DETECTOR, determines the frequency of the $+\Delta F$ VCO. The PHASE/FREQUENCY DETECTOR causes VT to go to its maximum level, therefore causing the $+\Delta F$ VCO frequency to be maximum anytime the VARIABLE FREQUENCY input is less than the REFERENCE FREQUENCY input for an appreciable length of time. The opposite effect on VT and the $+\Delta F$ VCO frequency occurs when the VARIABLE FREQUENCY input is greater than the REFERENCE FREQUENCY input. Thus the $+\Delta F$ VCO frequency is caused to vary in the direction which will cause the VARIABLE FREQUENCY input to be the same as the REFERENCE FREQUENCY input. When the $+\Delta F$ VCO frequency is such that the VARIABLE FREQUENCY is equal to the REFERENCE FREQUENCY, the $+\Delta F$ LOOP is said to be "LOCKED". The "LOCK" frequency should be maintained. Should the VARIABLE FREQUENCY input begin leading the REFERENCE FREQUENCY input in phase, VT will decrease. If the VARIABLE FREQUENCY input begins to lag the REFERENCE FREQUENCY input VT will increase.

The purpose of the MAXIMUM FREQUENCY CIRCUIT is to limit the maximum frequency of the $+\Delta F$ VCO. This prevents the frequency of the $+\Delta F$ VCO ΔF output, of the 91 MHz oscillator module, from being 2(91 MHz) minus the $+\Delta F$ VCO frequency.

The VARIABLE FREQUENCY input to the PHASE/FREQUENCY DETECTOR is generated in the following manner. The 91 MHz MIXER INJECTION output of the $+/F$ VCO is mixed with the output of the 91 MHz crystal oscillator. The difference frequency output of the mixer, the $+/F$ VCO ΔF , is filtered to eliminate the 2(91 MHz) minus the $+\Delta F$ VCO frequency from the output. The $+\Delta F$ VCO ΔF frequency is divided by 20 and then by the PROGRAMMABLE $\div N$ section. The resulting frequency is the VARIABLE FREQUENCY input to the PHASE/FREQUENCY DETECTOR.

The N value for the PROGRAMMABLE $\div N$ is determined by the output of the FREQUENCY CONTROL LOGIC which is determined by either the REMOTE CONTROL 2/5 INPUTS, the CHANNEL FREQUENCY SELECTOR or the MHz FREQUENCY SELECTOR.

The REFERENCE FREQUENCY input to the PHASE/FREQUENCY DETECTOR is 5 KHz. This is derived from either the 2 MHz CRYSTAL OSCILLATOR in the CAL mode or the 4 MHz VFO in the UNCAL mode, as selected by the UNCAL switch located on the front panel.

Thus the "LOCK" frequency of the $+\Delta F$ VCO is $(20 \times N \times 5 \text{ KHz})$ plus 91 MHz.

$$+\Delta F \text{ VCO "LOCK" frequency} = \left(\frac{N}{10} + 91 \right) \text{ MHz}$$

$$-\Delta F \text{ VCO "LOCK" frequency} = \left(\frac{N}{10} + 89 \right) \text{ MHz}$$

B. HIGH FREQUENCY LOOP

The HIGH FREQUENCY LOOP controls the frequency of the MASTER VCO in the following manner.

The MASTER VCO will tend to "LOCK" at any frequency which causes the MASTER VCO $+\Delta F$ and the MASTER VCO $-\Delta F$ frequencies to be the same. These "lock point" frequencies occur at $K(+\Delta F \text{ VCO freq. plus } -\Delta F \text{ VCO freq.}) \div 2$, $K = 1, 2, \dots, 9, 10, 11, 12$, etc.

Operation of the PHASE/FREQUENCY DETECTOR-AMPLIFIER section of the HIGH FREQUENCY LOOP is such that when the MASTER VCO $+\Delta F$ frequency is greater than the MASTER VCO $-\Delta F$ frequency, the output, the Master VCO VT, increases thus causing the MASTER VCO frequency to increase. The output decreases when the MASTER VCO $-\Delta F$ frequency is greater than the MASTER VCO $+\Delta F$ frequency. Thus the MASTER VCO frequency is caused to vary in the direction which will cause the MASTER VCO $+\Delta F$ frequency to equal the MASTER VCO $-\Delta F$ frequency which is the condition for "LOCK".

The "LOCK" frequency is maintained because should the phase of the MASTER VCO $+\Delta F$ input began leading the phase of the MASTER VCO $-\Delta F$ input the MASTER VCO VT is caused to increase thus increasing the MASTER VCO frequency. The Master VCO VT decreases when the MASTER VCO $-\Delta F$ input phase begins leading the MASTER VCO $+\Delta F$ input phase.

The MASTER VCO $+\Delta F$ frequency is generated by the MIXER section in the $+\Delta F$ VCO module. The $+\Delta F$ Mixer Injection output of the MASTER VCO is mixed with the output of the HARMONIC GENERATOR section. The filtering of the MIXER output allows only the difference frequency between the MASTER VCO frequency and one of the harmonics generated in the HARMONIC GENERATOR to appear in the output, the MASTER VCO $+\Delta F$.

The MASTER VCO is caused to "LOCK" at the proper "LOCK POINT" in the following manner. The MASTER VCO $+\Delta F$ frequency is divided by 20 and becomes the variable input to the FREQUENCY COMPARATOR. The reference input to the FREQUENCY COMPARATOR is 0.5 MHz. Anytime the variable frequency is not equal to the reference frequency the FREQUENCY COMPARATOR output causes the triggering of the SWEEP DOWN CIRCUIT. Thus the MASTER VCO VT is caused to sweep down in value until the MASTER VCO $+\Delta F$ frequency is equal to 10 MHz and remains 10 MHz. This only occurs when the MASTER VCO frequency is equal to $10(+\Delta F \text{ VCO frequency plus } -\Delta F \text{ VCO frequency}) \div 2$. If the MASTER VCO does not "LOCK" during the sweep down portion of the search cycle, the CHARGE UP CIRCUIT is activated and the MASTER VCO VT is caused to take on its maximum value after which the SWEEP DOWN CIRCUIT is activated.

Should the MASTER VCO "LOCK" frequency of 1000 MHz be required, the $+\Delta F$ VCO is "LOCKED" to 101 MHz and the $-\Delta F$ VCO is "LOCKED" to 99 MHz.

When in "LOCK" the $+\Delta F$ MIXER INJECTION is mixed with 1010 MHz yielding a 10 MHz value for the MASTER VCO $+\Delta F$ output. The $-\Delta F$ MIXER INJECTION is mixed with 990 MHz yielding a 10 MHz value for the MASTER VCO $-\Delta F$ output.

$$\begin{aligned} \text{MASTER VCO "LOCK" Frequency} &= \left(\frac{N}{10} + 90 \right) \times 10 \\ &= 900 + N \end{aligned}$$

Fig. 1 illustrates the frequencies involved when the "LOCK" frequency of 1000 MHz is required.

C. ΔF VFO

The 4 MHz VFO frequency is controlled by the front panel ΔF control. After a division by 2 it becomes an input to the INT/EXT. 2 MHz SWITCH. This SWITCH also has an EXT. 2 MHz VFO input to allow remote variation of the generator frequency. The 1 MHz VFO output is used to generate the REFERENCE FREQUENCY input to the PHASE/FREQUENCY DETECTOR in the UNCAL mode. Thus the generator frequency may be varied by means of the front panel ΔF control.

D. FREQUENCY CONTROL LOGIC

The REMOTE/LOCAL FREQUENCY CONTROL input causes N to be determined by either the REMOTE FREQUENCY selector or the CHANNEL FREQUENCY/MHz FREQUENCY SELECTOR.

FREQUENCY CONTROL SOURCE LOGIC inputs determine the state, "1" or "0", of the various outputs. These outputs determine whether the REMOTE FREQUENCY SELECTOR or the CHANNEL FREQUENCY/MHz FREQUENCY SELECTOR shall determine the FREQUENCY GENERATOR frequency.

REMOTE FREQUENCY SELECTOR levels are converted to TTL levels by the LEVEL TRANSLATORS.

The MHz 2/5 TO 1/10 DECODE sections cause the ARINC 2 out of 5 code, used by the REMOTE FREQUENCY SELECTOR, to be converted to a 1 out of 10 code. These sections also determine whether the REMOTE FREQUENCY SELECTOR or the CHANNEL FREQUENCY/MHz FREQUENCY SELECTOR shall determine the FREQUENCY GENERATOR frequency depending on the state of the Remote Control line. These sections also accept the inputs from the CHANNEL FREQUENCY SELECTOR which is a 1/10 code.

The X-Y MODE LOGIC section outputs determine whether the FREQUENCY GENERATOR frequency corresponds to X or Y Mode.

The PS-1,2,4,8 1/10 TO BCD DECODE section converts the 1/10 code output of the 0.1 MHz 2/5 TO 1/10 DECODE section to the corresponding BCD code. This section also accepts the inputs from the MHz FREQUENCY SELECTOR which is a BCD code.

The PS-100,200 and PS-10,20,40,80 DECODE section converts the 1/10 code output of the 1.0 MHz 2/5 TO 1/10 DECODE and 10 MHz 2/5 TO 1/3 DECODE sections and the outputs of the X-Y MODE LOGIC to the necessary BCD code to cause the FREQUENCY GENERATOR to have the proper output frequency. This section also accepts the inputs from the 10 MHz FREQUENCY SELECTOR which is a BCD code and the 100 MHz FREQUENCY SELECTOR which is a 1/4 code.

The XPS-4,8 LOGIC section converts the inputs from the PS-100,200 and PS-10,20,40,80 to the required states of the XPS-4 and XPS-8 outputs to cause the FREQUENCY GENERATOR to have the proper frequency.

The X-Y PULSE SPACING LOGIC generates the required state on the X-Y PULSE SPACING CONTROL output as determined by the various inputs. The AUTO X-Y MODE input causes the X-Y pulse spacing to be determined by the input from the X-Y MODE LOGIC section. The X Mode input causes the X-Y PULSE SPACING CONTROL to correspond to X MODE. If neither the Auto X-Y MODE or X MODE input is at a "0", the X-Y PULSE SPACING CONTROL corresponds to Y MODE.

THEORY OF OPERATION

LOW FREQUENCY BOARD, G1, THEORY

PURPOSE:

To supply the necessary voltage on the ΔF VCO VT outputs to cause the respective ΔF VCO to "LOCK" at the proper frequency.

OPERATION:

Since the $+\Delta F$ and $-\Delta F$ functions are identical in operation, only the $-\Delta F$ sections will be discussed.

A. $-\Delta F$ AMPLIFIER

I19 provides the amplification of the $-\Delta F$ VCO ΔF input to produce a signal level sufficient to drive I20A.

B. $-\Delta F \div 20$

I16B and I21 provide frequency division of 20. I18B provides buffering.

C. $-\Delta F$ PROGRAMMABLE $\div N$

I22, I23 and I24 supply frequency division of N. These devices are programmable, cascadable, modulo N down counters. When the whole counter has been counted down to the "0" state by the clock input to I22, Pin 6, the gate inputs to Pin 4 of I22, I23 and I24 go to a "0" and the counter is preset to the value N. When the whole counter is in the "0" state the "Buss" output Pin 12 of I22, I23 and I24 is at a "1". This pulse on the "Buss" is the $-\Delta F$ VARIABLE FREQUENCY input to the PHASE/FREQUENCY DETECTOR. If the XPS-0 line is at a "0", I16A is held RESET and there is a "1" on the \bar{Q} output of I16A, Pin 8. This allows all pulses on the "Buss" line to appear on the $-\Delta F$ VARIABLE FREQUENCY line. If the XPS-0 is at a "1", I16A is caused to "Toggle" by the pulses on the "Buss" line. This causes the counter to be preset alternately to the value on the PS-X lines and then the XPS-X lines. Since only every other pulse on the "Buss" line appears on the $-\Delta F$ VARIABLE FREQUENCY line, the division ratio is the sum of the PS-X and XPS-X values. When the XPS-X value is being preset into I22 the \bar{MR} input to Pin 10 of I23 and I24 is at a "0" which causes I23 and I24 to be preset to "0".

D. $-\Delta F$ PHASE/FREQUENCY DETECTOR

If the $-\Delta F$ VARIABLE FREQUENCY input to I7A, Pin 3 is a faster frequency then the REFERENCE FREQUENCY input to I17A, Pin 1, the waveforms at the various points correspond to the PD (Pull Down) condition. If the frequency is lower, the PU (Pull Up) condition is present. If the frequencies are equal, the "LOCK" condition is present. The waveforms on the LOW FREQUENCY LOOP schematic should be present under the various conditions.

E. $-\Delta F$ LEAD/LAG AMPLIFIER

The LEAD/LAG AMPLIFIER provides integration and inversion of the pulses present on the output of the PHASE/FREQUENCY DETECTOR.

F. $-\Delta F$ MAXIMUM FREQUENCY CIRCUIT

The maximum voltage level that can be generated on the $-\Delta F$ VCO VT output is limited by the setting of R22. The voltage is limited because should Q6 be turned on by the $-\Delta F$ VCO VT voltage, the voltage on the gate input to Q5 is increased due to current flow from the collector of Q6.

G. 2MHz OSCILLATOR

The 2MHz OSCILLATOR is straight forward with the output taken from the collector of Q1. Amplification of this signal by Q2 and limiting by CR1 and CR2 provides TTL level required at the input to Pin 1 of 11A. 11B provides buffering.

H. $\div 2$

I2B provides frequency division while 11C provides buffering.

I. CAL/UNCAL SWITCH

The CAL/UNCAL switch provides selection of either the 1MHz reference or 1 MHz VFO frequency as the source of the 5KHz reference used by the PHASE/FREQUENCY DETECTOR. Selection is made by means of the CAL/UNCAL control line.

J. $\div 200$

I2A, I4 and I5 provide frequency division of 200 to provide a 5KHz output from a 1MHz input.

89 MHz OSCILLATOR, G3, AND 91 MHz OSCILLATOR, G2, THEORY

PURPOSE:

To generate an output which is the difference frequency between the ΔF VCO and the crystal frequency.

OPERATION:

Only the 91 MHz OSCILLATOR operation will be described since the 89 MHz OSCILLATOR is the same except for the crystal frequency.

A. 91 MHz OSCILLATOR

The 91 MHz OSCILLATOR operation is straight forward with the output taken from the collector of Q1. Fine frequency adjustment is made by means of C6.

B. MIXER

The difference frequency between the 91 MHz OSCILLATOR frequency and the 91 MHz MIXER INJECTION frequency is generated in the hot-carrier diode, CR1.

C. LPF

The LPF with a cut-off frequency of 40 MHz prevents the difference between $2(91\text{MHz})$ minus the 91 MHz MIXER INJECTION frequency from appearing in the $+\Delta F$ VCO ΔF output.

D. AMPLIFIER

The AMPLIFIER, I1 provides amplification of the output of the LPF.

HIGH FREQUENCY LOOP BOARD, G4, THEORY

PURPOSE:

To supply the necessary voltage on the MASTER VCO VT output to cause the MASTER VCO to "LOCK" at the proper frequency.

OPERATION:

A. $+\Delta F$ AMPLIFIER AND $-\Delta F$ AMPLIFIER

The MASTER VCO $+\Delta F$ and MASTER VCO $-\Delta F$ inputs are amplified to ECL levels by the $+\Delta F$ AMPLIFIER and $-\Delta F$ AMPLIFIER.

B. PHASE/FREQUENCY DET-AMPL

The operation of the PHASE/FREQUENCY DET-AMP is best described by means of the timing diagram shown in Fig 2. As can be seen when the frequency of the $-\Delta F$ signal is greater than the $+\Delta F$ signal the PU output consists of narrow pulses whereas the PD output pulse width is much greater. This results in different average voltages on the bases of Q2 and Q3 causing Q2 to turn on. When Q2 is turned on, Q5 conducts and the Master VCO VT decreases causing the MASTER VCO frequency to decrease. Thus the MASTER VCO is caused to maintain the "LOCK" frequency. Should the $+\Delta F$ frequency be greater than the $-\Delta F$ frequency, Q3 is turned on resulting in the MASTER VCO VT increasing causing the MASTER VCO frequency to increase.

C. LEVEL TRANSLATOR

The LEVEL TRANSLATOR, consisting of Q1, translates the ECL level to TTL level required as the input level to the $\div 20$ circuit.

D. $\div 20$

The $\div 20$ circuit divides the MASTER VCO $+\Delta F$ frequency to provide a 0.5 MHz output frequency when the input is 10 MHz.

E. $\div 2$

The $\div 2$ circuit divides the 1 MHz REFERENCE input to provide a 0.5 MHz output.

F. REFERENCE PULSE GENERATOR AND VARIABLE PULSE GENERATOR

The REFERENCE PULSE GENERATOR will be described only as the operation of the VARIABLE PULSE GENERATOR is identical. When the 0.5 MHz input to Pin 13 of I8D goes to a "0", the output. Pin 11, goes to a "1". This "1" causes the output, Pin 3 of I8A, to go to a "0" causing the output, Pin 6 of I8B, to go to a "1".

This "1" causes the output of I8A, pin 3, to be latched at a "0" and the output of I8D, Pin 11, to go to a "0". Thus a short duration positive pulse is generated at the output of I8D, pin 11, and a negative pulse to be present on the output of I8C, Pin 8. The purpose of R28 and C4 is to widen the pulse.

G. FREQUENCY COMPARATOR

Should the PRF of the VARIABLE PULSE input be greater than that of the REFERENCE PULSE, at some time I10A and triggered more than once for a single SET pulse on I10A and I10B. Therefore the \bar{Q} output, Pin 6 of I10A, is triggered from a "1" to a "0" causing the Q output of I10B, Pin 9, to be triggered to a "0" causing a negative pulse to be generated. The portion of the FREQUENCY COMPARATOR consisting of I11 operates in the same manner.

H. SWEEP DOWN CIRCUIT

When the VARIABLE PULSE PRF does not equal the REFERENCE PULSE PRF, the negative pulses appearing on the inputs to I12, Pin 1 or Pin 2, cause the Q output to be triggered to a "1". This causes Q7 to conduct and the MASTER VCO VT to decrease. The above operation is inhibited by the "0" on the input of I12, Pin 4, during the CHARGE UP portion of the SEARCH CYCLE.

I. SEARCH CYCLE TIMER

The Q9 output of the timer is set to a "1" at the end of the CHARGE UP portion of the SEARCH CYCLE due to current flowing thru R43 causing Q8 to conduct. After an interval of approximately 50 msec. Q9 goes to a "0" which will allow a "1" to appear on collector of Q10 should the \bar{Q} output of I12, Pin 6, go to a "0". Thus a "1" will appear on the collector of Q10 if the loop has not properly "LOCKED" by the time the SEARCH CYCLE TIMER has timed out. This "1" initiates the CHARGE UP operation.

J. CHARGE UP CIRCUIT

If Q11 is caused to conduct due to current flowing thru R45, the "1" appearing on the collector of Q12 causes Q14 to conduct and the MASTER VCO VT to increase. When VT reaches a level sufficient to cause Q15 to conduct, current flowing thru R46 will cause Q12 to conduct. While Q11 is at a "0" the SWEEP DOWN CIRCUIT is inhibited due to the "0" on the input to I12, Pin 4.

+ ΔF VCO, G5, and - ΔF VCO, G6, THEORY

PURPOSE:

To generate a difference frequency which is the difference between the MASTER VCO frequency and the tenth harmonics of the ΔF VCO frequency.

OPERATION:

Only the + ΔF VCO will be described since the - ΔF VCO is identical.

A. + ΔF VCO and BUFFER

The + ΔF VCO is of the reactance switching type. On the peak positive swing of the collector waveform of Q1 the diode CR1 is caused to conduct thus allowing C2 to be "seen" by the oscillator circuitry. Therefore the lower the + ΔF VCO VT is the longer C2 is "seen" thru CR1, hence the lower the frequency of oscillation.

The HEATER, C01, provides thermal stability of the parameters of the transistor, Q1 and the diode, CR1. The buffer, Q2, provides isolation and amplification of the + ΔF VCO output.

B. AMPLIFIER/HARMONIC GENERATOR

The AMPLIFIER, Q3, amplifies the BUFFER output to provide an adequate drive level for the HARMONIC GENERATOR which in turn generates harmonically related frequencies of the + ΔF VCO frequency in the step-recovery diode, CR2. An attenuated portion of the BUFFER output is used to provide the 91 MHz MIXER INJECTION.

C. MIXER

The MIXER generates the difference frequencies between the various harmonics of the + ΔF VCO frequency and the + ΔF MIXER INJECTION from the MASTER VCO in hot carrier diode CR3.

D. LPF/AMPLIFIER

The LPF, with a 40 MHz cut-off frequency, attenuates all the difference frequencies generated in the MIXER except that difference frequency which is 40 MHz or less.

The AMPLIFIER, I1, amplifies the output of the LPF.

MASTER VCO, G7, THEORY

PURPOSE:

To generate a +20dbm signal at a frequency in the 962 MHz - 1213 MHz range to be used, after modulation, as the test set RF output.

OPERATION:

The frequency of oscillation of the MASTER VCO is controlled by the biasing of the varactor diode CR1 by the MASTER VCO VT input. Attenuated outputs are used for the $+\Delta F$ MIXER INJECTION, the $-\Delta F$ MIXER INJECTION and the FREQUENCY MONITOR MIXER INJECTION.

FREQUENCY CONTROL LOGIC, L3, THEORY

PURPOSE:

To convert the various inputs to the necessary program to cause the RF Generator frequency to correspond to the selected frequency.

The source of frequency selection may be

- a. REMOTE FREQUENCY SELECTOR
- b. MHz FREQUENCY SELECTOR
- c. CHANNEL FREQUENCY SELECTOR

OPERATION:

REMOTE FREQUENCY SELECTOR inputs are selected by the REMOTE/LOCAL FREQUENCY CONTROL switch. The MHz FREQUENCY SELECTOR is selected by having the 0-5 MHz CONTROL switch in the MHz position. Placing the switch in the 0 or 5 position causes CHANNEL FREQUENCY SELECTOR control.

A. LEVEL TRANSLATORS

PURPOSE:

To cause the large voltages present on the inputs to be translated to TTL levels on the outputs.

OPERATION:

When the input voltage level passes thru the 7.5 ± 1 volt level the output changes TTL level state.

The output level is inverted from the input level.

B. 10, 1.0 and 0.1 MHz 2/5 TO 1/10 DECODE

PURPOSE:

To cause the 2/5 inputs to be decoded into 1 of 10 outputs corresponding to the CHANNEL FREQUENCY.

OPERATION:

Since the 10 MHz, 1.0 MHz and 0.1 MHz sections work alike only the 1.0 MHz will be described.

Observation of 2/5 to Decimal Chart below shows that if

the A and B inputs are at a "0", CHANNEL FREQUENCY XX1.XX is called for. The state of the inputs would cause the inputs of the NAND Gate I17c, Pins 1 and 13, to be at a "1" causing the output, Pin 12 of I17c, to be a "0" providing the input of I17c, Pin 2, is at a "1". The input to I17c, Pin 2 will be a "1" only if REMOTE CONTROL is called for. This operation is typical throughout the rest of this section and also for the 10 MHz and 0.1 MHz sections.

	0	1	2	3	4	5	6	7	8	9
A	1	0	0	1	1	1	1	1	0	0
B	0	0	1	0	0	1	1	1	1	1
C	1	1	0	0	1	0	0	1	1	1
D	1	1	1	1	0	0	1	0	0	1
E	0	1	1	1	1	1	0	0	1	0

C. FREQUENCY CONTROL SOURCE LOGIC

PURPOSE:

To cause the source of frequency control to be that called for by the REMOTE/LOCAL FREQUENCY CONTROL switch and the 0-5-MHz CONTROL switch.

OPERATION:

If the REMOTE/LOCAL FREQUENCY CONTROL switch is in the REMOTE position, the inputs to NAND Gates I10B, Pin 4, and I10C, Pin 9, and Inverter I25D, Pin 9, are at a "0" causing all outputs to be at a "1". Thus none of the CHANNEL FREQUENCY SELECTOR inputs or the MHz FREQUENCY SELECTOR inputs can assume a "0". Neither can the outputs of the 0-5-MHz CONTROL switch. The "1" on the inputs to the NAND gates in the 10 MHz, 1.0 MHz, 0.1 MHz 2/5 TO 1/10 DECODE sections enable these decode gates.

If the REMOTE/LOCAL FREQUENCY CONTROL switch is in the LOCAL position, the "1" present on the input to Inverter I25D, pin 9 causes a "0" on the common of the 0-5-MHz CONTROL switch and causes all outputs of the 10 MHz, 1.0 MHz, 0.1 MHz 2/5 TO 1/10 DECODE sections to be "0".

If the 0-5-MHz CONTROL switch, is in either the 0 or 5 position, the MHz FREQUENCY SELECTOR common is at a "1" and the CHANNEL FREQUENCY SELECTOR common is at a "0" thus allowing selection of a Channel Frequency.

D. PS-1,2,4,8 1/10 TO BCD DECODE

PURPOSE:

To cause the outputs of the 0.1 MHz 2/5 TO 1/10 DECODE section to be converted to the required states of the PS-1,2,4,8 lines for proper generator frequency control.

D. PS-1,2,4,8 1/10 TO BCD DECODE (Cont'd)

OPERATION:

If CHANNEL FREQUENCY XXX.7X is selected, the inputs to NAND gates I12A, Pin 4, I13B, Pin 10 and I13A, Pin 5, are at a "0" causing the PS1, PS2 and PS4 lines to be at a "1" thus causing the generator to be properly programmed.

Operation is similar for other CHANNEL FREQUENCIES. The 1 MHz FREQUENCY SELECTOR inputs are all at "1"'s in the above case.

If MHz FREQUENCY XXX7 is selected, the "0"'s present inputs to NAND gates I12A, Pin 3, I13B, Pin 11 and I13A, Pin 3 cause the PS-1, PS-2 and PS-4 lines to be at a "1".

E. PS-100, 200 AND PS-10,20,40,80 DECODE

PURPOSE:

To cause the outputs of the 10 MHz and 0.1 MHz 2/5 TO 1/10 DECODE sections to be converted to the required states of the PS-100, 200* and PS-10, 20, 40, 80 lines for proper generator frequency control.

OPERATION:

If CHANNEL FREQUENCY 133.3X is selected either REMOTELY or LOCALLY, all inputs to NAND gate I22C, Pin 1, 2 and 13 are at "1"'s and the output, Pin 12 of I22C, is at a "0". This "0" controls the states of the PS-100 and PS-10 outputs. If CHANNEL FREQUENCY 133.30 is selected, the PS-10 and PS-100 outputs are caused to be "1"'s due to the turning off of the appropriate transistors, Q4 and Q8. For all XXX.X0 frequencies the X MODE FREQUENCY line is at a "1" and the Y MODE FREQUENCY line is at a "0". If 133.35 were selected instead, the PS-40 and PS-200 outputs would be a "1" and all other PS-10, 20, 40, 80 and PS-100 200 outputs would be at a "0".

Operation is similar for all other CHANNEL FREQUENCIES selected.

If the MHz FREQUENCY SELECTOR has control, the X MODE FREQUENCY line is at a "1" and the Y MODE FREQUENCY line is at a "0". Thus a "0" on the 10 MHz FREQUENCY SELECTOR input or the 100 MHz FREQUENCY SELECTOR input, causes the appropriate PS-100, 200 or PS-10, 20, 40, and 80 outputs to be a "1".

F. X-Y MODE LOGIC

PURPOSE:

To cause the X MODE FREQUENCY and Y MODE FREQUENCY lines to be in the proper state as called for by either the .01 MHz

*Channeling starts from 900 MHz

F. X-Y MODE LOGIC (Cont'd)

REMOTE FREQUENCY SELECTOR input or the XXX.X5 CHANNEL FREQUENCY SELECTOR. Also to provide an input to the X-Y MODE PULSE SPACING LOGIC for use in the AUTO X-Y MODE.

OPERATION:

If either the .01 MHz FREQUENCY SELECTOR input or the XXX.X5 CHANNEL FREQUENCY SELECTOR input is at a "0", the output of NAND gate 110A, Pin 3 is a "1". This "1" causes the l=Y MODE FREQUENCY line to be a "1" and the l=X MODE FREQUENCY line to be a "0" for proper generator programming. The output to the X-Y PULSE SPACING LOGIC causes the Y-MODE to be selected if the AUTO X-Y MODE is selected.

G. X-Y PULSE SPACING LOGIC

PURPOSE:

To generate an output which determines the REPLY PULSE PAIR SPACING, C7, and to control the INTERROGATION P2 WINDOW GENERATOR, C6, which is in accordance with the state of the inputs. These inputs are the AUTO X-Y MODE, X-MODE and the output of the X-Y MODE LOGIC.

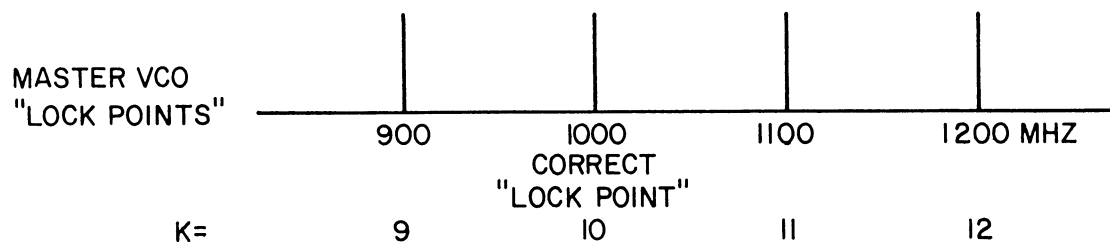
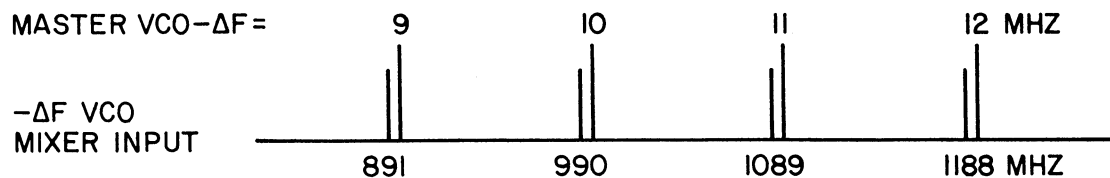
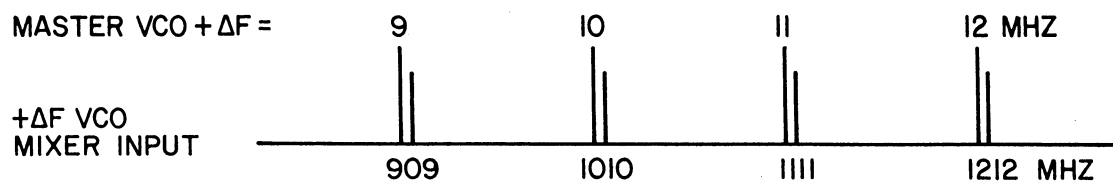
OPERATION:

If the AUTO X-Y MODE input is at a "0", the output varies in accordance with the output of the X-Y MODE LOGIC. If the X-MODE input is at a "0", the output is at a "1". If neither the Auto X-Y Mode or the X-MODE inputs are at a "0", the output is at a "0" for Y-MODE.

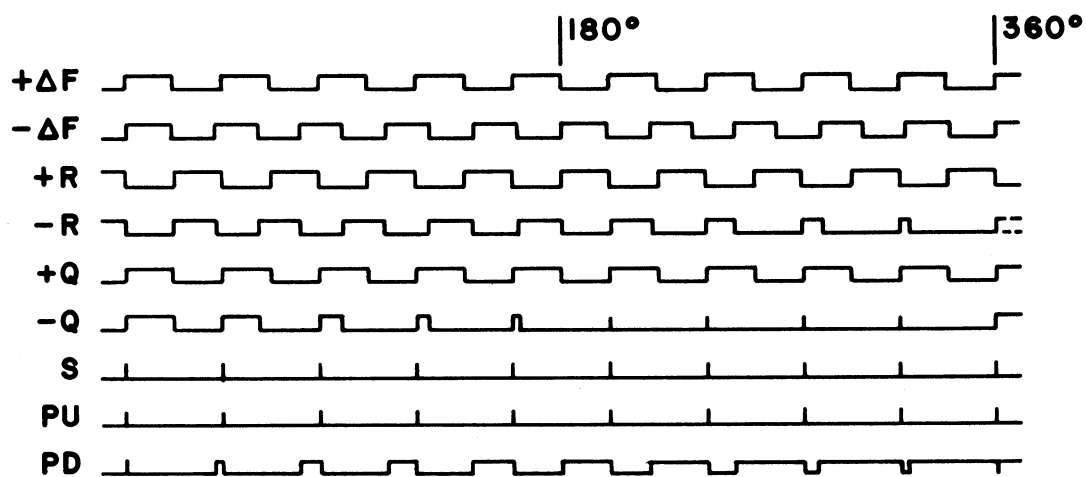
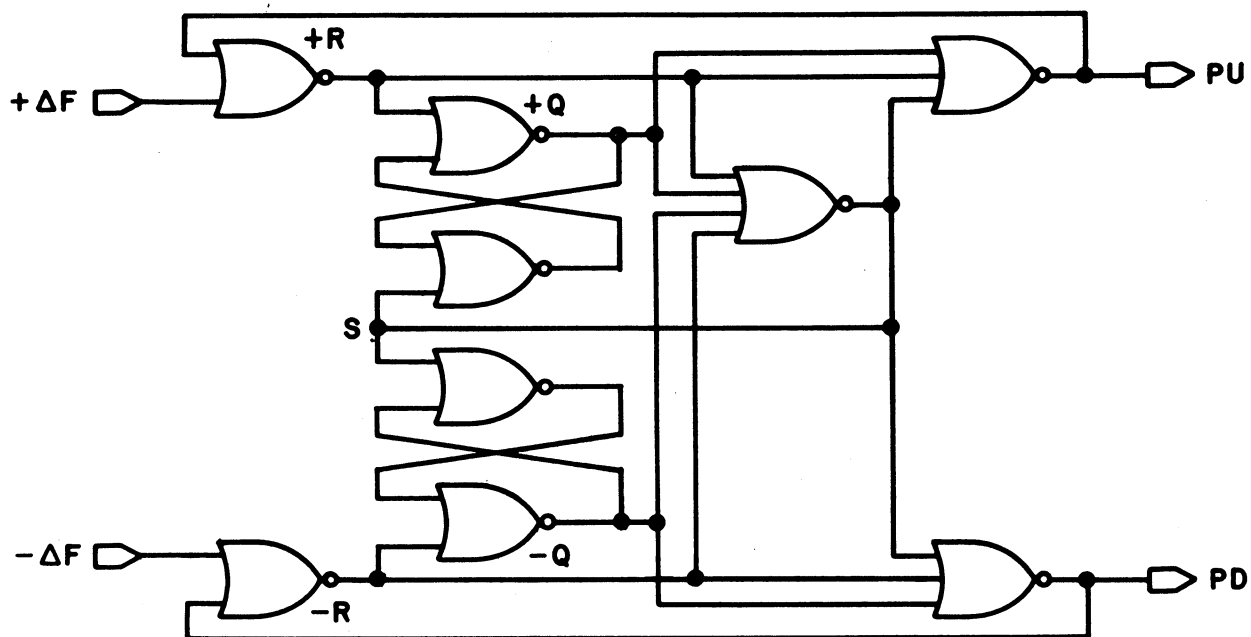
H. FREQUENCY CONTROL INPUTS STATES TO PS-X AND XPS-X OUTPUT STATES

Figure 3 gives the required PS-X and XPS-X states for a given REMOTE FREQUENCY SELECTOR or CHANNEL FREQUENCY SELECTOR position for X-MODE frequencies. Figure 4 is for Y-MODE frequencies. The required states of the PS-1,2,4,8 outputs and the required PS-X and XPS-X states for MHz FREQUENCY SELECTION are given in Figure 5.

Figure 6 gives the ARINC 2/5 BINARY CODE required by the REMOTE FREQUENCY SELECTOR inputs.



FREQUENCIES INVOLVED FOR LOCK FREQ. OF 1000 MHZ
FIG 1



PHASE FREQUENCY DETECTOR
TIMING DIAGRAM
FIG 2

REMOTE FREQ. SELECTOR TACAN CHAN.	CHAN. FREQ. SELECTOR	FREQ. GEN. FREQ.	XPS 4	XPS 8	PS 10	PS 20	PS 40	PS 80	PS 100	PS 200
1X	134.40	962	0	1	1	0	1	0	0	0
6X	134.90	967								
7X	135.00	968	0	1	0	1	1	0	0	0
16X	135.90	977								
17X	108.00	978	0	1	1	1	1	0	0	0
26X	108.90	987								
27X	109.00	988	0	1	0	0	0	1	0	0
36X	109.90	997								
37X	110.00	998	0	1	1	0	0	1	0	0
46X	110.90	1007								
47X	111.00	1008	0	1	0	0	0	0	1	0
56X	111.90	1017								
57X	112.00	1018	0	1	1	0	0	0	1	0
59X	112.20	1020								
60X	133.30	1021	0	1	1	0	0	0	1	0
63X	133.60	1024								
64X	133.70	1151	1	0	0	0	1	0	0	1
66X	133.90	1153								
67X	134.00	1154	1	0	1	0	1	0	0	1
69X	134.20	1156								
70X	112.30	1157	1	0	1	0	1	0	0	1
76X	112.90	1163								
77X	113.00	1164	1	0	0	1	1	0	0	1
86X	113.90	1173								
87X	114.00	1174	1	0	1	1	1	0	0	1
96X	114.90	1183								
97X	115.00	1184	1	0	0	0	0	1	0	1
106X	115.90	1193								
107X	116.00	1194	1	0	1	0	0	1	0	1
116X	116.90	1203								
117X	117.00	1204	1	0	0	0	0	0	1	1
126X	117.90	1213								

$\overline{\text{XPS}-0} = 1$

X MODE FREQUENCIES
FIG 3

REMOTE FREQ. SELECTOR TACAN CHAN.	CHAN. FREQ. SELECTOR	FREQ. GEN. FREQ.	XPS 4	XPS 8	PS 10	PS 20	PS 40	PS 80	PS 100	PS 200
1Y	134.45	1088	1	0	0	0	0	1	1	0
6Y	134.95	1093								
7Y	135.05	1094	1	0	1	0	0	1	1	0
16Y	135.95	1103								
17Y	108.05	1104	1	0	0	0	0	0	0	1
26Y	108.95	1113								
27Y	109.05	1114	1	0	1	0	0	0	0	1
36Y	109.95	1123								
37Y	110.05	1124	1	0	0	1	0	0	0	1
46Y	110.95	1133								
47Y	111.05	1134	1	0	1	1	0	0	0	1
56Y	111.95	1143								
57Y	112.05	1144	1	0	0	0	1	0	0	1
59Y	112.25	1146								
60Y	133.35	1147	1	0	0	0	1	0	0	1
63Y	133.65	1150								
64Y	133.75	1025	0	1	1	0	0	0	1	0
66Y	133.95	1027								
67Y	134.05	1028	0	1	0	1	0	0	1	0
69Y	134.25	1030								
70Y	112.35	1031	0	1	0	1	0	0	1	0
76Y	112.95	1037								
77Y	113.05	1038	0	1	1	1	0	0	1	0
86Y	113.95	1047								
87Y	114.05	1048	0	1	0	0	1	0	1	0
96Y	114.95	1057								
97Y	115.05	1058	0	1	1	0	1	0	1	0
106Y	115.95	1067								
107Y	116.05	1068	0	1	0	1	1	0	1	0
116Y	116.95	1077								
117Y	117.05	1078	0	1	1	1	1	0	1	0
126Y	117.95	1087								

XPS-0 = 1

Y MODE FREQUENCIES
FIG 4

PS-1,2,4,8						
MHz FREQ. SELECTOR	REMOTE FREQ. SELECTOR	CHAN, FREQ. SELECTOR	PS 1	PS 2	PS 4	PS 8
XXX0	X7	XXX.OX	0	0	0	0
XXX1	X8	XXX.1X	1	0	0	0
XXX2	X9	XXX.2X	0	1	0	0
XXX3	X0	XXX.3X	1	1	0	0
XXX4	X1	XXX.4X	0	0	1	0
XXX5	X2	XXX.5X	1	0	1	0
XXX6	X3	XXX.6X	0	1	1	0
XXX7	X4	XXX.7X	1	1	1	0
XXX8	X5	XXX.8X	0	0	0	1
XXX9	X6	XXX.9X	1	0	0	1

PS-10,20,40,80				
MHz FREQ. SELECTOR	PS 10	PS 20	PS 40	PS 80
XXOX	0	0	0	0
XX1X	1	0	0	0
XX2X	0	1	0	0
XX3X	1	1	0	0
XX4X	0	0	1	0
XX5X	1	0	1	0
XX6X	0	1	1	0
XX7X	1	1	1	0
XX8X	0	0	0	1
XX9X	1	0	0	1

PS-100,200		
MHz FREQ. SELECTOR	PS 100	PS 200
X9XX	0	0
X0XX	1	0
X1XX	0	1
X2XX	1	1

XPS-0 = 0 in MHz Freq. Select Mode
 XPS-4 = 0 in MHz Freq. Select Mode
 XPS-8 = 0 in MHz Freq. Select Mode

PS-X CHART
 FIG 5

ARINC 10 MHz CODE

	A	E
10X.XX	1	0
11X.XX	0	1
13X.XX	1	1

ARINC FREQ. SELECTOR
2 OUT OF 5 BINARY CODE

	A	B	C	D	E
0	1	0	1	1	0
1	0	0	1	1	1
2	0	1	0	1	1
3	1	0	0	1	1
4	1	0	1	0	1
5	1	1	0	0	1
6	1	1	0	1	0
7	1	1	1	0	0
8	0	1	1	0	1
9	0	1	1	1	0

C.01 = 1 for X Mode
= 0 for Y Mode

1 = Greater than 8V
0 = Less than 6V

ARINC CODE
FIG 6

CALIBRATIONS

1. Allow 30 minute warm-up period.
2. Connect frequency counter to G1-23. Adjust capacitor C20 on the LOW LOOP BOARD for counter reading of 2,000,000 Hz.
3. Connect counter to junction of R4 and CR1 in the 91 MHz OSCILLATOR, G2. Adjust C6 for counter reading of 91.00 MHz. CAUTION After adjustment check to insure 91 MHz OSCILLATOR will start after SQUAWK/NAUT has been turned off. Readjust C6 if necessary.
4. Same as 3 except adjust 89 MHz OSCILLATOR, G3, for counter reading of 89.00 MHz.
5. Connect counter to RF OUTPUT. Determine if frequency is within tolerance. If not, readjust 2 MHz OSCILLATOR frequency to bring within tolerance.

ADJUSTMENT PROCEDURE FOR ΔF VCO INDUCTANCE L3, (G5 and G6) AND ΔF MAXIMUM FREQUENCY CIRCUIT, (G1)

1. ΔF VCO INDUCTANCE L3, (G5 and G6)*
Select 960 MHz and adjust L3 for ΔF VCO VT of 0.95 to 1.00 volts. Allow 10 minute warm up.
2. ΔF MAXIMUM FREQUENCY CIRCUIT (G1)*
Select 1230 MHz and note ΔF VCO VT value. Short the ΔF VCO ΔF input, (G1-19 or G1-17), to the ΔF AMPLIFIER to ground. Adjust the pot in the ΔF MAXIMUM FREQUENCY CIRCUIT for a ΔF VCO VT value which is 0.3V greater than that observed when ΔF VCO was "LOCKED". When short is removed ΔF VCO should immediately "RELOCK" for 1230 MHz operation.

CAUTION: DO NOT TURN THE POT FULL CW

*Covers for ΔF VCO modules must be on.

SELECTION PROCEDURE FOR LOW FREQUENCY LOOP BOARD, G1

1. Selection of R14 and R20 in ΔF LEAD/LAG AMPLIFIER section.

R14 is selected so the IDSS of Q3, times the value of R14, is less than 1.4 volts so the inverting amplifier, I6C will shut off. R14 is also selected so that the pulse width, when in "LOCK", at the D1 output of I6A, Pin 2 is not greater than 200 nsec.

2. Selection of R27 and R34 in ΔF AMPLIFIER section.

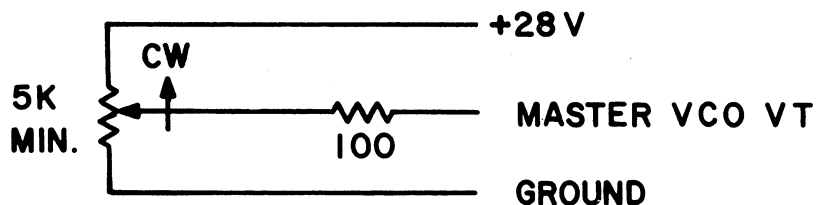
R27 is selected so the inputs to I20D are biased near the transition level.

SELECTION PROCEDURE FOR ΔF VCO FEEDBACK CAPACITOR, C6 (G5 and G6)

1. Disconnect ΔF VCO VT from input to ΔF VCO. Supply tuning voltage with pot or power supply.
2. Attach counter probe to collector of Q3. Use high impedance probe.
3. With approximately 1.0 volt on VT, adjust L3 and L2 for oscillator frequency of 95 MHz for the $-\Delta F$ VCO or 97 MHz for the $+\Delta F$ VCO.
4. Decrease VT voltage while monitoring frequency. At some voltage, frequency will cease decreasing and begin increasing. If this voltage is above 0.7 volts, increase the value of C6. If lower than 0.4 volts decrease the value of C6.
5. Repeat steps 3 and 4 as there is some interaction.
6. Slowly vary the VT voltage while observing the frequency. There should be no sudden changes in frequency. Check up to a frequency of 132 MHz. Check for hysteresis in the frequency vs. VT curve. The ΔF VCO should turn smoothly. If not, it may be necessary to replace Q1 and CR1.

MASTER VCO DOES NOT CHANNEL PROPERLY, G7

1. Check pertinent Power Supply Voltages -28V, +28V, +5V, +16V, +16±2V. Check for AC Ripple.
2. Check + Δ F VCO LOOP for proper channeling.
3. Check - Δ F VCO LOOP for proper channeling.
4. Observe MASTER VCO VT and determine if the complete SEARCH CYCLE is performed. If not go to Step 9.
5. Disconnect MASTER VCO VT from HIGH LOOP BOARD. Supply VT voltage by means of a pot connected as shown below. Disconnect resistors R36 and R54 on the HIGH LOOP BOARD, G4.



6. Do Step 5. Adjust MASTER VCO VT for selected MASTER VCO frequency and observe wave form on MASTER VCO + Δ F and MASTER VCO - Δ F inputs to the HIGH LOOP BOARD. If observed amplitude and frequency not as should be, determine why, fix, reconnect resistors and MASTER VCO VT.
7. Do Step 5. Adjust MASTER VCO VT for selected MASTER VCO frequency and observe MASTER VCO VT output of HIGH LOOP BOARD. As MASTER VCO frequency is varied about selected frequency, VT should go low as frequency goes above and high as frequency goes below the selected frequency. If VT does not behave in this manner determine why, fix, reconnect resistors and MASTER VCO VT.
8. Do Step 5 except do not disconnect the MASTER VCO VT. By means of a voltage source, steer the MASTER VCO to "LOCK" points and determine if lock is achieved. If not, this is an indication of a malfunction in the MASTER VCO or that the MASTER VCO output is "seeing" an improper load due to high VSWR caused by faulty cable or ISOLATOR, G8, input.
9. Will not perform SWEEP DOWN portion of SEARCH CYCLE, G4.
 - A. Check the Q output of I12, Pin 8 for positive pulses. If present check Q7 for failure. If not present - -

- B. Check trigger inputs to I12, Pins 1 and 2 for negative pulses on one or the other. If not present, check the FREQUENCY COMPARATOR for cause of lack of output. If present - -
 - C. Check trigger input to I12, Pin 4, for presence of a "1". If not present determine why the collector of Q11 is not caused to go to a "1" at the end of the CHARGE UP portion of the SEARCH CYCLE. If "1" is present replace I12.
10. Will not perform CHARGE UP portion of SEARCH CYCLE, G4.
- A. Check the collector of Q12 for presence of "1". If present, check Q13 and Q14 for failure. If not present -
 - B. Check the collector of Q10 for presence of positive pulse. If present, check for failure of Q11, Q12, or Q15. If not present - -
 - C. Check \bar{Q} output of I12, Pin 6, for presence of negative pulses. If not present determine cause of malfunction of SWEEP DOWN circuit. If present - -
 - D. Check the collector of Q9 for presence of "0". If not present determine cause of failure of SEARCH CYCLE TIMER. If present check Q10 for failure.

- Δ F VCO DOES NOT CHANNEL PROPERLY*

To determine if the - Δ F VCO is properly locked, observe the outputs of the - Δ F PHASE/FREQUENCY DETECTOR located on the LOW FREQUENCY LOOP BOARD, G1. Observe the U and D outputs of I7A, Pins 13 and 2. If the - Δ F VCO is properly locked, narrow, negative, pulses of 200 nsec. or less duration, with very small jitter should be observed.

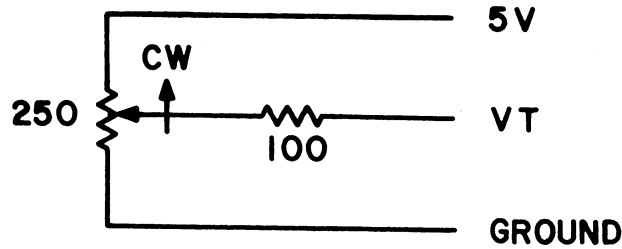
To determine if the - Δ F VCO is operating at the proper frequency, a frequency count at the collector of Q3 in the - Δ F VCO, G6, should be taken. Use a high impedance probe. The proper frequency may be determined with the use of information given in the FREQUENCY CONTROL LOGIC, L3, THEORY and the FREQUENCY GENERATOR BLOCK DIAGRAM THEORY.

1. - Δ F VCO does not "LOCK" properly.

- A. Check pertinent Power Supply Voltages +5V, +16V, 16 \pm 2V. Check for AC Ripple.

* Typical for + Δ F VCO

- B. Disconnect $-\Delta F$ VCO VT line at the input to $-\Delta F$ VCO. Apply a voltage to the $-\Delta F$ VCO VT input to the $-\Delta F$ VCO by means of a pot and resistor as shown below or a power supply.



- C. Select MHz Frequency of 1000 MHz.

Do step 1B. Adjust $-\Delta F$ VCO frequency for 99.9 MHz. Observe $-\Delta F$ VCO VT. As $-\Delta F$ VCO frequency is caused to go below 99.9 MHz the $-\Delta F$ VCO VT should go to the maximum value determined by the $-\Delta F$ MAXIMUM FREQUENCY CIRCUIT on the LOW FREQUENCY LOOP BOARD, G1. As the frequency is caused to go above 99.9 MHz VT should go to the low value of 0.8V. If VT behaves in this manner the reason for failure to "LOCK" properly is located in the $-\Delta F$ VCO OSCILLATOR circuitry, go to step 1G. If VT does not behave in this manner go to step 1D.

- D. Select 1000 MHz.

Do step 1B. Adjust VT for $-\Delta F$ VCO frequency of 99.9 MHz. Observe the V1 input to I7A, Pin 3 in the PHASE/FREQUENCY DETECTOR on G1. A narrow positive pulse should be present with a 5 KHz PRF. Also check for presence of the 5 KHz REFERENCE FREQUENCY input to the R1 input, to I7A, Pin 1. If the VARIABLE FREQUENCY input is not as it should be go to Step E. If the REFERENCE FREQUENCY input is not as it should be determine why and fix.

If these signals are present check $-\Delta F$ PHASE FREQUENCY DETECTOR and $-\Delta F$ LEAD/LAG AMPLIFIER for proper operation. Observe the various points of the PHASE/FREQUENCY DETECTOR for the proper wave form under the "LOCK", PU and PD conditions. To check $-\Delta F$ LEAD/LAG AMPLIFIER short the gate input to Q5 to ground. The VT should go to maximum value. Connect a 1K resistor between +5V and I7C, Pin 9. The VT should go to 0.8V. See SELECTION PROCEDURE FOR ΔF LEAD/LAG AMPLIFIER.

- E. 1. Select 1000 MHz. Do step 1B. Adjust $-\Delta F$ VCO frequency for 99.9 MHz.
2. Check for output of the $-\Delta F \div 20$ at I8B, Pin 6 for the presence of a 0.5 MHz signal. If not present go to step F.

3. Check the "BUSS" line for presence of a positive 5 KHz pulse. If present, determine why it does not appear on the $-\Delta F$ VARIABLE FREQUENCY line.
4. Check the \overline{MR} inputs to Pin 10 of I23 and I24, of the LOW FREQUENCY LOOP, G1, for the presence of a "1". No pulses should be present if the MHz FREQUENCY SELECTOR is in use. Check the P0, P1, P2, P3 inputs to Pins 5, 11, 14 and 2 of I22, I23 and I24, for the proper states. Only I24, Pin 5 should be at a "1" for 1000 MHz.
5. Select 900 MHz. Ground the "BUSS" line. I22, I23 and I24 should function as $\div 10$ counters. Replace any section which does not.
6. Select 900 MHz. All P0, P1, P2 and P3 inputs to I22, I23 and I24 should be at a "0". The "BUSS" line should be at a "1". If not a direct short to ground or a failure in I22, I23, I24, I18A, or I16A is indicated. Cutting of the path between I22, Pin 12 and 13, and I18A, Pin 2 narrows the problem. If the "BUSS" output is still "0" cutting of path between I24, Pin 12 and I23, Pin 12 narrows the problem and cutting the path between I22, Pins 12 and 13 and I23, Pin 12 further reduces the problem.
7. Selection of 901 MHz thru 909 MHz should cause the counter to be a $\div 1$ thru $\div 9$ divider. Selection of 910 thru 990 should cause the counter to be a $\div 10$ thru $\div 90$ divider. Selection of 1000 thru 1200 MHz should cause the counter to be a $\div 100$ thru $\div 300$ divider.

F. Do step 1B

Adjust $-\Delta F$ VCO VT for a $-\Delta F$ VCO frequency of 99.9 MHz. Check the output of the $-\Delta F \div 20$ at Pin 6 of I18B for the presence of a 0.5 MHz signal. If not present check the input to $-\Delta F \div 20$ at Pin 1 of I16B for a 10 MHz signal. If not present check the RF levels the 89 MHz OSCILLATOR, G3. See SELECTION PROCEDURE FOR LOW FREQUENCY LOOP BOARD, G1.

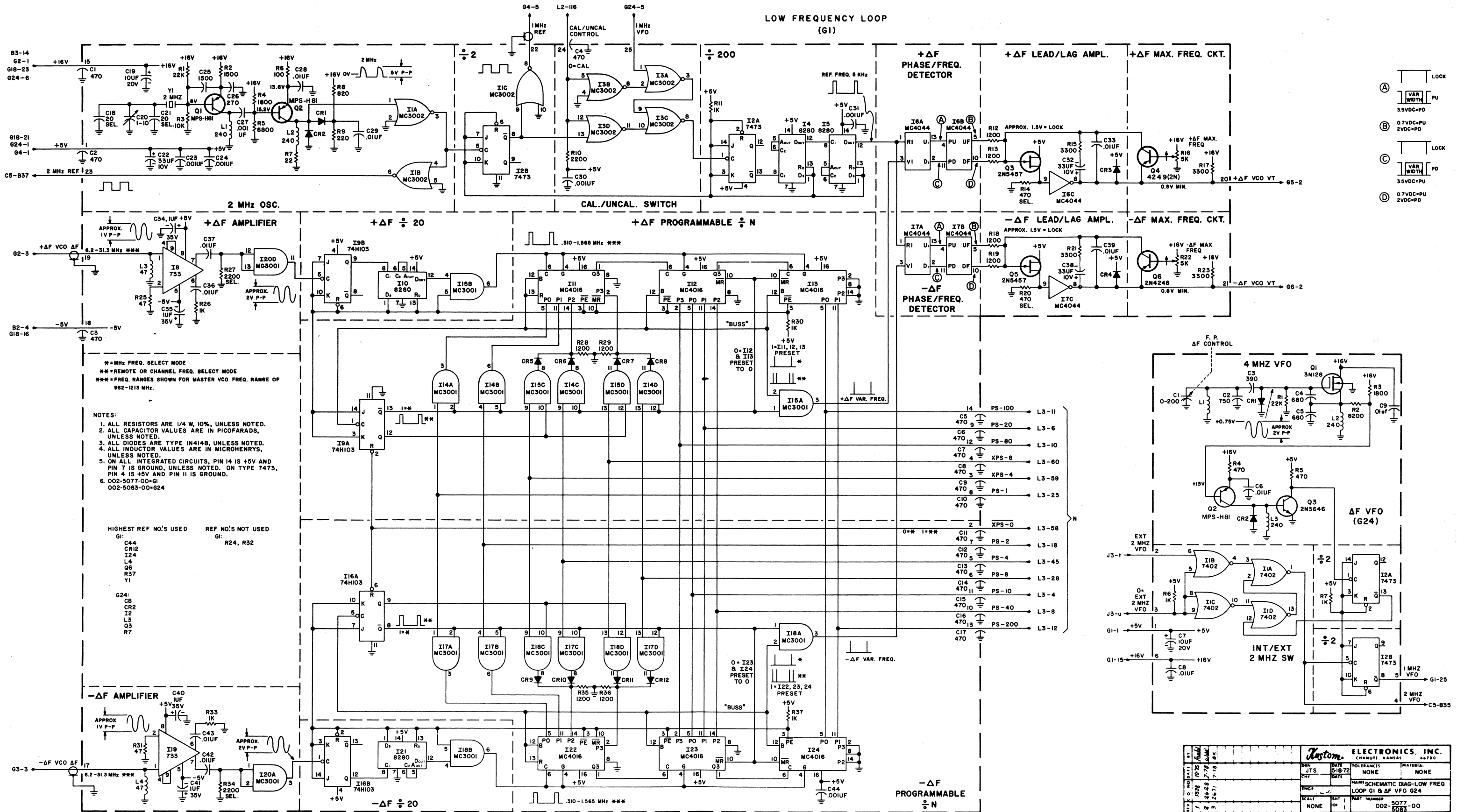
G. Do step 1B.

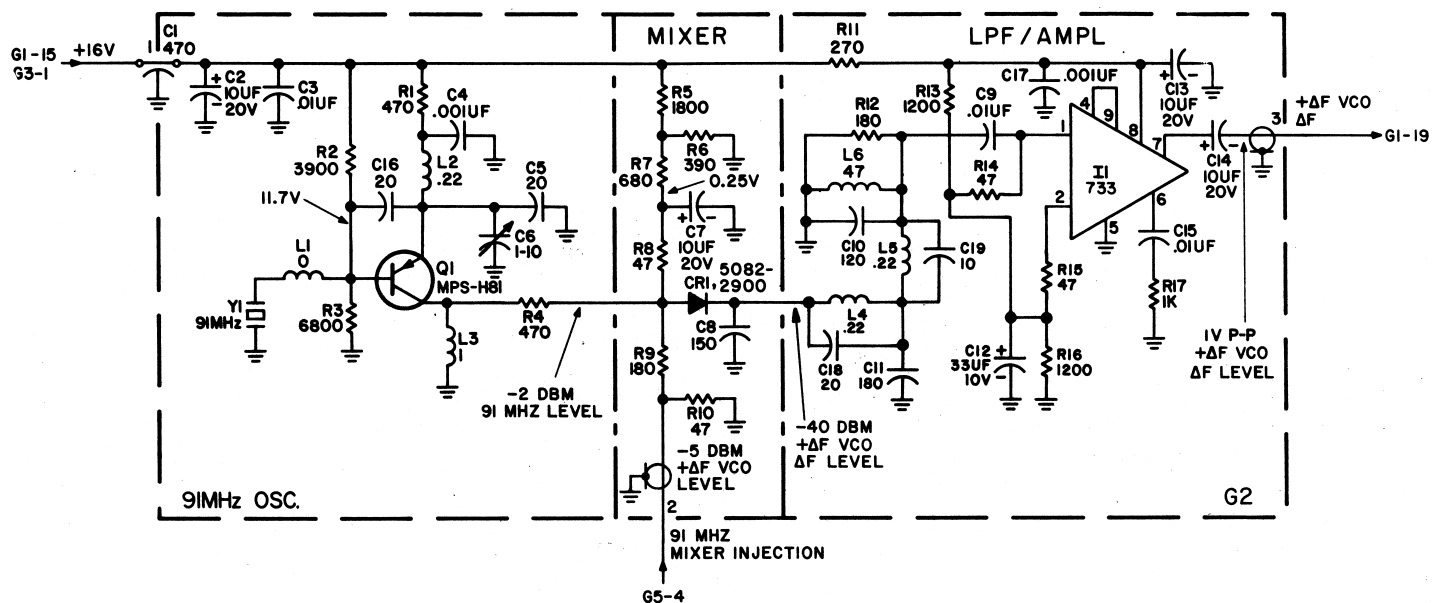
Attach counter to the collector of Q3 of $-\Delta F$ VCO, G6. Vary $-\Delta F$ VCO VT voltage and observe frequency. There should be no sudden jumps in frequency vs. VT or any indication of hysteresis in the frequency vs. VT Curve, the $-\Delta F$ VCO should tune smoothly. The frequency should constantly decrease with decreasing VT for VT values above 0.7V. If this behavior is not observed see SELECTION PROCEDURE for ΔF VCO.

2. $-\Delta F$ VCO does not operate at the proper frequency but does "LOCK".

- A. Determine if the $+\Delta F$ VCO exhibits the same "LOCK" but improper frequency. If so, check the state of the N inputs for proper values.
- B. 1. Do step 1E1 and 1E7. This checks the programmability of I22, I23, and I24 in the $-\Delta F$ PROGRAMMABLE $\div N$.
2. Select a channel frequency of 111.00. The counter should operate alternately as a $\div 100$ and a $\div 8$. This should result in one pulse on the $-\Delta F$ VARIABLE FREQUENCY line for every 108 pulses of the clock. If this performance is not observed, check the R input to Pin 6 of I16A for presence of a "1", check for toggling action of I16A, check for proper operation of I18D and CR11.

Select a channel frequency of 135.05. The counter should operate alternately as a $\div 190$ and a $\div 4$. This should result in one pulse on the $-\Delta F$ VARIABLE FREQUENCY line for every 194 pulses of the clock. If this performance is not observed check as in the above paragraph except check I18C and CR9.





NOTES:



BOTTOM
VIEW OF II

LAST REF NO. USED

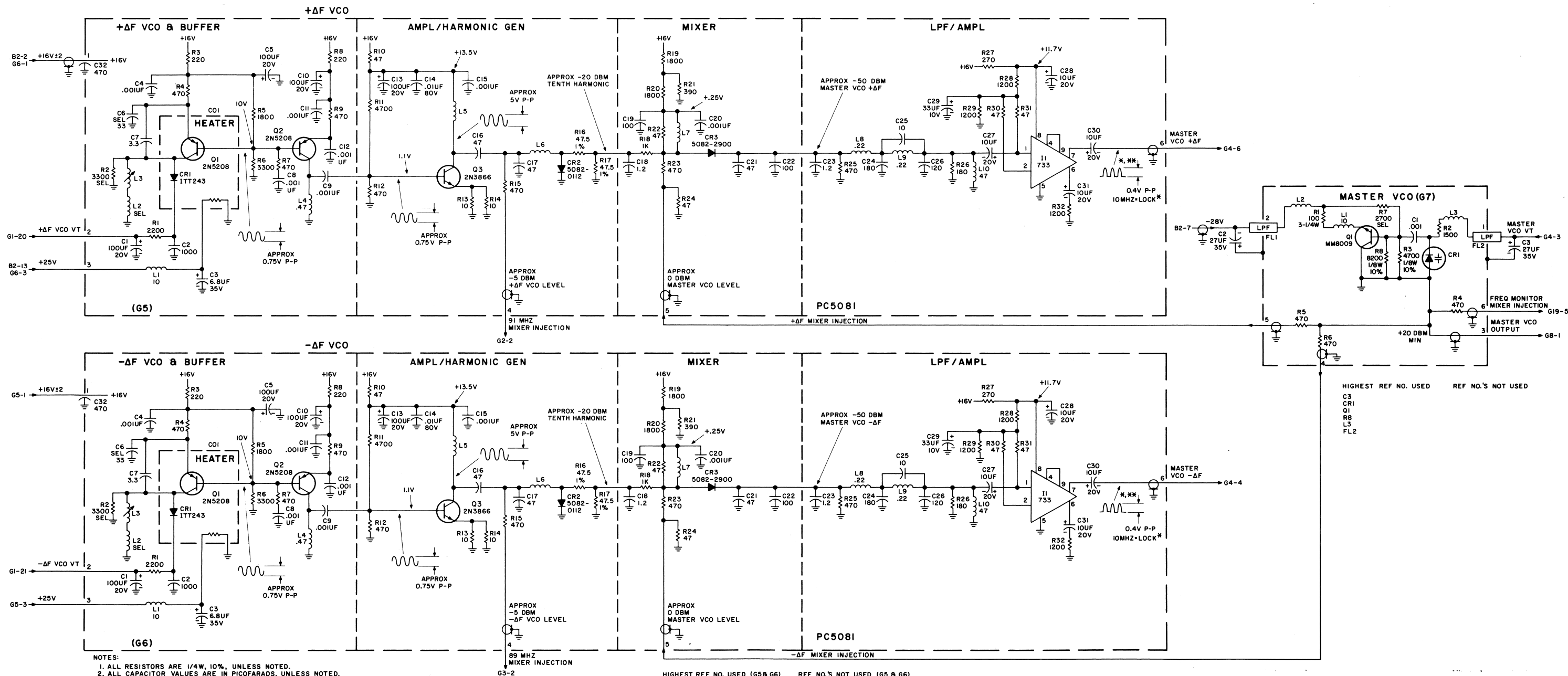
CI7
CRI
II
L6
QI
RI7

Rev. 4 Feb. 1979



1. ALL RESISTORS ARE 1/4W, 10%, UNLESS NOTED.
2. ALL CAPACITOR VALUES ARE IN PICOFARADS, UNLESS NOTED.
- * WHEN MASTER VCO IS PROPERLY LOCKED, ΔF VCO AND $-\Delta F$ VCO ALSO LOCKED.
- ** ECL VOLTAGE LEVELS.
3. ALL INDUCTOR VALUES ARE IN MICROHENRYS, UNLESS NOTED.
4. ON ALL INTEGRATED CIRCUITS, PIN 14 IS +5V AND PIN 7 IS GROUND, UNLESS NOTED.
ON TYPE 74H103, PIN 4 IS +5V AND PIN II IS GROUND.

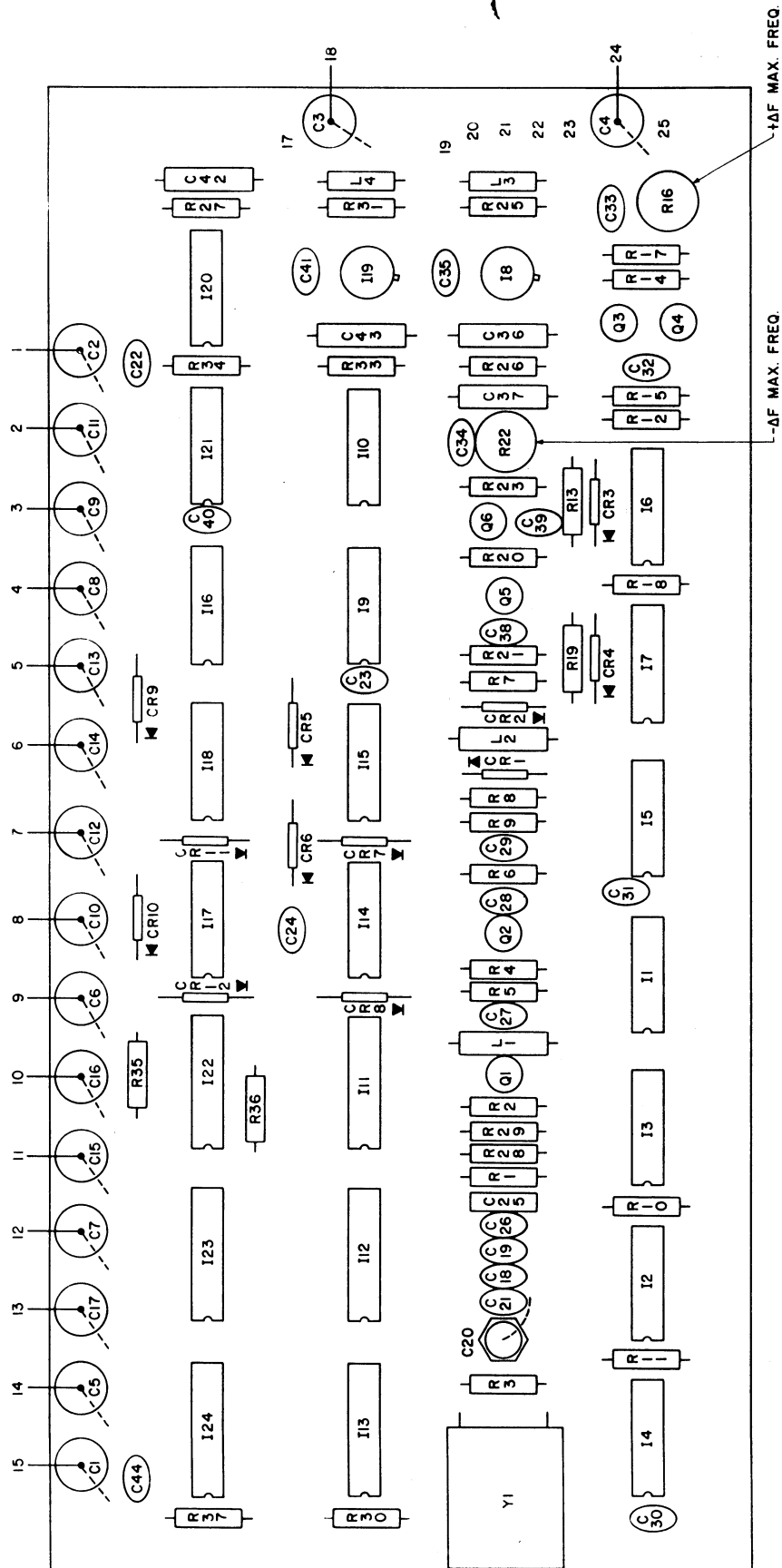
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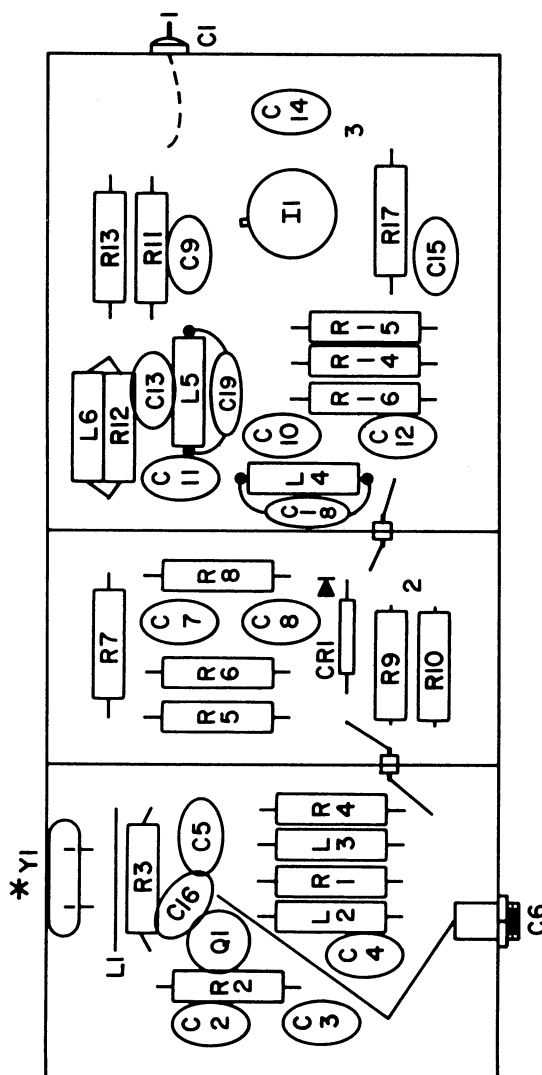


NOTES:

1. ALL RESISTORS ARE 1/4W, 10%, UNLESS NOTED.
2. ALL TRANSISTORS ARE TYPE 35677
3. KPN 007-0008-00, UNLESS NOTED.
4. ALL DIODES ARE TYPE IN4148, UNLESS NOTED.
5. SWITCHES S26, S27, S28, AND S29 ARE MOUNTED ON THE FRONT PANEL, AND ARE SHOWN HERE FOR CLARITY ONLY.

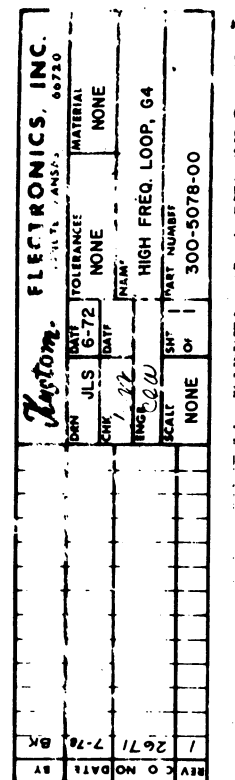


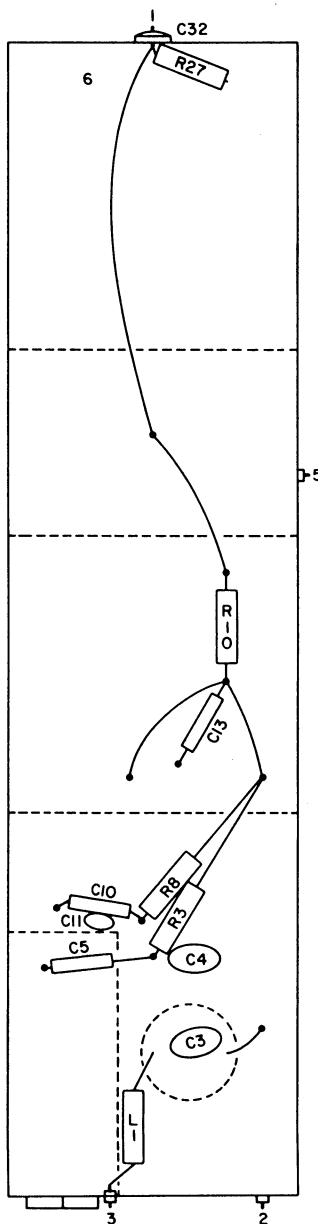
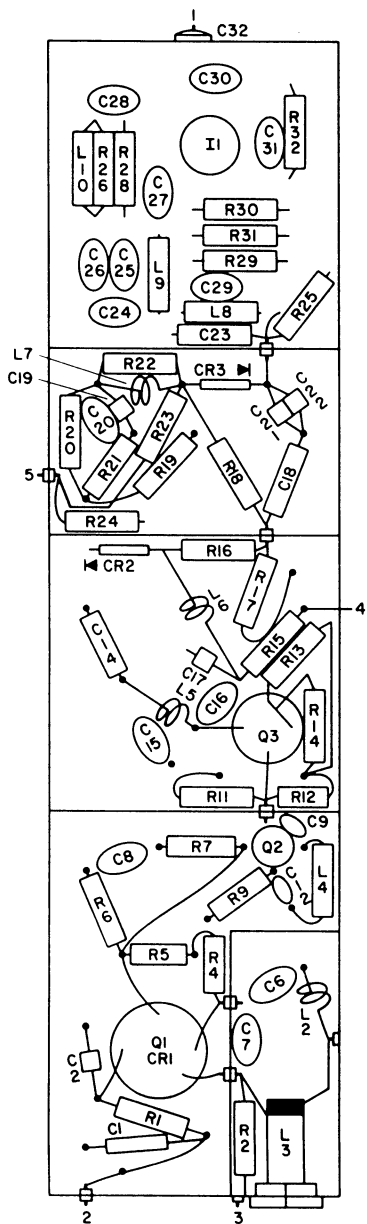
ELECTRONICS INC.									
REV	C NO	DATE	BY	CHKD	TEST	SCALE	UNIT	OF	300-5077-00
1	1								
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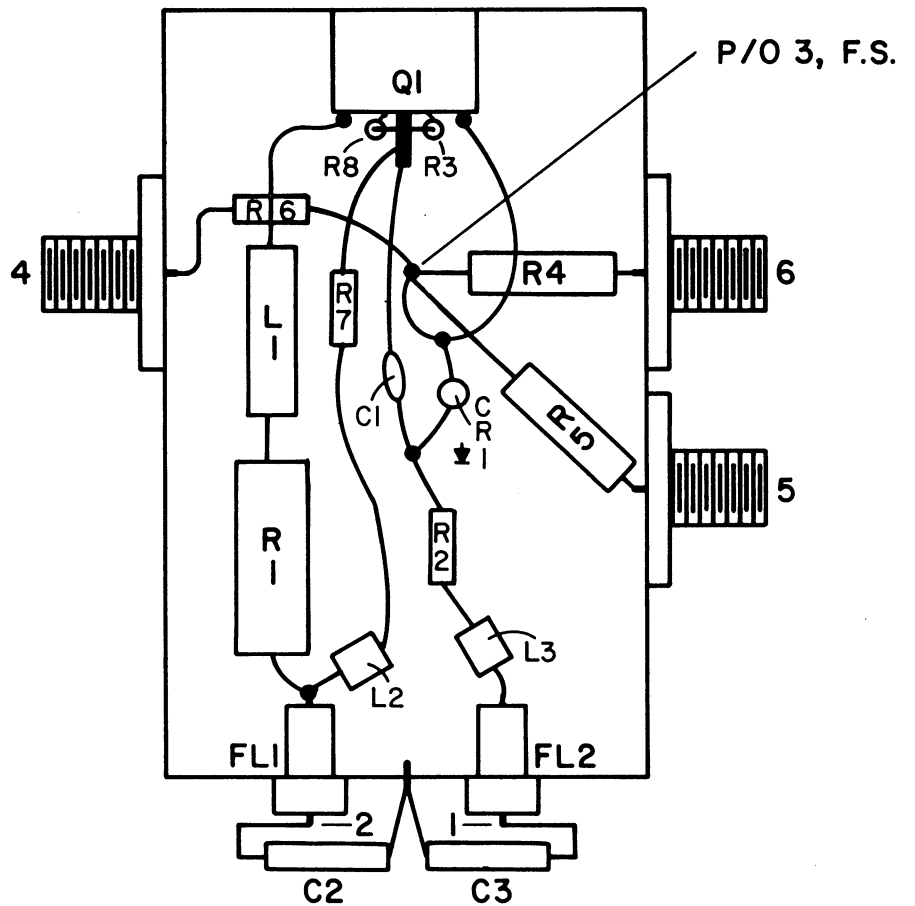
* Y1 IS 91MHz ON SCHEMATIC 002-5082-00.
 * Y1 IS 89MHz ON SCHEMATIC 002-5082-01.

Custom. ELECTRONICS, INC. CHANUTE, KANSAS 66720									
DRN	JLS	DATE	TOLERANCES	MATERIAL					
CHK	DATE	6-72	NONE	NONE					
ENGR	SCALE	DATE	NAME	91MHz OSC., G2 89MHz OSC., G3					
REV	C	O	N	O	PART NUMBER				
1	1	1	1	1	300-5082-00				





REV. C		DATE		BY	
JLS		6-72		NONE	
PMP		DATE		NONE	
IMP		DATE		NONE	
SCALE		PART NUMBER		300-5081-00	
NONE		OF		1	
ΔF VCO, G5 & G6		PART NUMBER		300-5081-00	
NONE		OF		1	
JLS		6-72		NONE	
PMP		DATE		NONE	
IMP		DATE		NONE	
SCALE		PART NUMBER		300-5081-00	
NONE		OF		1	
ΔF VCO, G5 & G6		PART NUMBER		300-5081-00	
NONE		OF		1	



REV	CO	DATE	BY										
1	1424	3-75	SMITH										
2	1603	3-76	AWALD										
				Rev. 3 Aug. 1978									
				Kustom. ELECTRONICS, INC. CHANUTE, KANSAS 66720									
				DRN	JLS	DATE	6-72	TOLERANCES	NONE	MATERIAL	NONE		
				CHK	JEN	DATE		NAME					
				ENGR	CEW	MASTER V.C.O., G7							
				SCALE	NONE	SHT	OF	PART NUMBER					
								300-5081-01					

PARTS LIST

ASSEMBLY NO: 200-5077-00
 DESCRIPTION: LOW FREQ LOOP BD SUB-ASSY (G1)
 ASSY DWG NO: 300-5077-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1-C17	CAPACITOR F/T 470 PF	106-0002-00
C18	CAPACITOR D/C 20 PF NPO 5%	110-2000-04
C19	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C20	CAPACITOR TRIMMER 1-10 PF	102-0002-00
C21	CAPACITOR D/C 20 PF NPO 5%	110-2000-04
C22	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C23	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C24	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C25	CAPACITOR MICA 1500 PF 300V 10%	100-0000-09
C26	CAPACITOR D/C 270 PF X5F 10%	109-2710-35
C27	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C28	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C29	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C30	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C31	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C32	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C33	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C34	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C35	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C36	CAPACITOR MLR .01 UF 80V 10%	105-0031-08
C37	CAPACITOR MLR .01 UF 80V 10%	105-0031-08
C38	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C39	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C40	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C41	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C42	CAPACITOR MLR .01 UF 80V 10%	105-0031-08
C43	CAPACITOR MLR .01 UF 80V 10%	105-0031-08
C44	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
CR1-CR12	DIODE 1N4148	007-6016-00
I1	VT IC MC3002P	007-7077-01
I2	VT IC SN7473N	007-7057-01
I3	VT IC MC3002P	007-7077-01
I4	VT IC SN74196	007-7006-01
I5	VT IC SN74196	007-7006-01
I6	VT IC MC4044P	007-7081-01
I7	VT IC MC4044P	007-7081-01
I8	VT IC LM733CH	007-7082-01
I9	VT IC SN74H103	007-7085-01
I10	VT IC SN74196	007-7006-01
I11	VT IC MC4016P	007-7080-01
I12	VT IC MC4016P	007-7080-01
I13	VT IC MC4016P	007-7080-01
I14	VT IC MC3001P	007-7076-01
I15	VT IC MC3001P	007-7076-01
I16	VT IC SN74H103	007-7085-01
I17	VT IC MC3001P	007-7076-01
I18	VT IC MC3001P	007-7076-01
I19	VT IC LM733CH	007-7082-01
I20	VT IC MC3001P	007-7076-01

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
I21	VT IC SN74196	007-7006-01
I22	VT IC MC4016P	007-7080-01
I23	VT IC MC4016P	007-7080-01
I24	VT IC MC4016P	007-7080-01
L1	INDUCTOR RF 240 UH	019-2015-47
L2	INDUCTOR RF 240 UH	019-2015-47
L3	INDUCTOR 47 UH	019-2016-30
L4	INDUCTOR 47 UH	019-2016-30
Q1	TRANSISTOR MPS H81	007-0077-00
Q2	TRANSISTOR PNP 2N5208	007-0026-00
Q3	TRANSISTOR 2N5457 FET	007-0037-00
Q4	TRANSISTOR PNP 2N4249	007-0009-00
Q5	TRANSISTOR 2N5457 FET	007-0037-00
Q6	TRANSISTOR PNP 2N4249	007-0009-00
R1	RESISTOR F/C 22K 1/4W 10%	130-0223-25
R2	RESISTOR F/C 1.5K 1/4W 10%	130-0152-25
R3	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R4	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R5	RESISTOR F/C 6.8K 1/4W 10%	130-0682-25
R6	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R7	RESISTOR F/C 22 OHM 1/4W 10%	130-0220-25
R8	RESISTOR F/C 820 OHM 1/4W 10%	130-0821-25
R9	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R10	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R11	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R12	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R13	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R14	RESISTOR F/C 470 OHM 1/4W 10%	130-0471-25
R15	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R16	POT 5K TYPE SV 1 TURN	133-0042-10
R17	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R18	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R19	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R20	RESISTOR F/C 470 OHM 1/4W 10%	130-0471-25
R21	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R22	POT 5K TYPE SV 1 TURN	133-0042-10
R23	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R25	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R26	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R27	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R28	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R29	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R30	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R31	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R33	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R34	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R35	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R36	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R37	RESISTOR F/C 1K 1/4W 10%	130-0102-25
Y1	XTAL 2 MHZ	044-0002-00
	PC BD LOW FREQ LOOP	009-5077-00
	CLIP CRYSTAL	090-0106-01
	RIVET BUTTON HEAD	092-0012-22

ASSEMBLY NO: 200-0199-00
 DESCRIPTION: VFO SUB-ASSY (G24)
 ASSY DWG NO: 300-5083-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR VARIABLE 0-200 PF	102-0000-00
C2	CAPACITOR MICA 750 PF 300V 10%	100-0000-11
C3	CAPACITOR MICA 390 PF 300V 10%	100-0000-08
C4	CAPACITOR MICA 680 PF 300V 10%	100-0000-06
C5	CAPACITOR MICA 680 PF 300V 10%	100-0000-06
C6	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C7	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C8	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C9	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
CR1	DIODE 1N4148	007-6016-00
CR2	DIODE 1N4148	007-6016-00
I1	VT IC SN74C2	007-7048-01
I2	VT IC SN7473N	007-7057-01
L1	INDUCTOR 7T	019-2010-00
L2	INDUCTOR RF 240 UH	019-2015-47
L3	INDUCTOR RF 240 UH	019-2015-47
Q1	TRANSISTOR 3N128	007-0034-00
Q2	TRANSISTOR PNP 2N5208	007-0026-00
Q3	TRANSISTOR 2N3646	007-0025-00
R1	RESISTOR F/C 22K 1/4W 10%	130-0223-25
R2	RESISTOR F/C 8.2K 1/4W 10%	129-0822-25
R3	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R4	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R5	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R6	RESISTOR F/C 1K 1/4W 10%	129-0102-25
R7	RESISTOR F/C 1K 1/4W 10%	129-0102-25
	LUG GND #6	008-0000-00
	GNT TERMINAL #2X.531	008-0017-02
	PC BD VFO	009-5083-00
	TERMINAL STANDOFF	010-0007-00
	TERMINAL FEEDTHRU	010-0008-00
	WIRE 26 GA TFE CW WHT	025-0006-99
	GEAR SPUR 21T	029-0000-00
	GEAR SPUR 130T	029-0003-00
	GEAR DIS SPUR 120T	029-0004-00
	CLUTCH SLIP	029-0008-00
	GEAR SPUR 30T	029-0009-00
	BRKT VFO REAR W/IRIDITE	047-0216-03
	COVER VFO	047-0218-01
	BRKT VFO SIDE W/IRIDITE	047-0219-03
	ENCLOSURE VFO	047-0221-01
	HOUSING GEAR HEAD	047-5011-01
	SPACER	076-0018-02
	SPACER	076-0039-01
	SHAFT CLUTCH	076-0040-00
	SHAFT CAL	076-0041-00
	NUT 2-56	089-2004-21
	SCREW PHP 6-32X3/16 SEM	089-5028-03

200-0199-00

SYMBOL

DESCRIPTION

KPN

SCREW PHP 6-32 X 1/4 SEMS	089-5028-04
SCREW PHP 6-32 X 3/8 SEMS	089-5028-06
WASHER INT TOOTH #2	089-8500-00
ROLL PIN .062 DIA X .312 L	090-0022-01
SPACER CERAMIC	090-0111-00
SELF CLINCH 6-32 040 MATL	092-0003-13
SELF CLINCH FAST #6-32	092-0003-14
SNAP RING	092-0011-02
BEARING BRONZE 1/8 D	147-0000-00
BEARING BRONZE 1/4 D	147-0000-02

ASSEMBLY NO:	200-0189-00
DESCRIPTION:	91 MHZ OSC SUB-ASSY
ASSY DWG NO:	300-5082-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR F/T 470 PF	106-0002-00
C2	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C3	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C4	CAPACITOR D/C .001 UF Z5V 20%	109-1021-16
C5	CAPACITOR D/C 20 PF NPO 5%	110-2000-04
C6	CAPACITOR TRIMMER 1-10 PF	102-0002-00
C7	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C8	CAPACITOR D/C 150 PF X5F 10%	109-1510-35
C9	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C10	CAPACITOR D/C 120 PF X5F 10%	109-1210-35
C11	CAPACITOR D/C 180 PF X5F 10%	109-1810-35
C12	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C13	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C14	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C15	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C18	CAPACITOR D/C 20PF NPO 5%	110-2000-04
C19	CAPACITOR D/C 10 PF NPO 5%	110-1000-04
CR1	DIODE 5082-2900	007-6022-00
I1	VT IC LM733CH	007-7082-01
L1	INDUCTOR	NPN
L2	INDUCTOR RF 22 UH	019-2016-02
L3	INDUCTOR MOLD 1 UH 10%	019-2016-10
L4	INDUCTOR RF 22 UH	019-2016-02
L5	INDUCTOR RF 22 UH	019-2016-02
L6	INDUCTOR 47 UH	019-2016-30
Q1	TRANSISTOR PNP MPS-H81	007-0077-00
R1	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R2	RESISTOR F/C 3.9K 1/4W 10%	130-0392-25
R3	RESISTOR F/C 6.8K 1/4W 10%	130-0682-25
R4	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R5	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R6	RESISTOR F/C 390 OHM 1/4W 10%	130-0391-25
R7	RESISTOR F/C 680 OHM 1/4W 10%	130-0681-25
R8	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R9	RESISTOR F/C 180 OHM 1/4W 10%	130-0181-25
R10	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R11	RESISTOR F/C 270 OHM 1/4W 10%	130-0271-25
R12	RESISTOR F/C 180 OHM 1/4W 10%	130-0181-25
R13	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R14	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R15	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R16	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R17	RESISTOR F/C 1K 1/4W 10%	129-0102-25
Y1	XTAL 91 MHZ	044-0007-00
	PC BD OSC	009-5082-00
	TERMINAL FEEDTHRU	010-0008-00
	ENCLOSURE OSC	047-0150-01
	CLIP CRYSTAL	090-0106-03
	RIVET BUTTON HEAD	092-0012-22

ASSEMBLY NO:	200-0184-00
DESCRIPTION:	89 MHZ OSC SUB-ASSY (G3)
ASSY DWG NO:	300-5082-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR F/T 470 PF	106-0002-00
C2	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C3	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C4	CAPACITOR D/C .001 UF Z5V 20%	109-1021-16
C5	CAPACITOR D/C 20 PF NPO 5%	110-2000-04
C6	CAPACITOR TRIMMER 1-10 PF	102-0002-00
C7	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C8	CAPACITOR D/C 150 PF X5F 10%	109-1510-35
C9	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C10	CAPACITOR D/C 120 PF X5F 10%	109-1210-35
C11	CAPACITOR D/C 180 PF X5F 10%	109-1810-35
C12	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C13	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C14	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C15	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C18	CAPACITOR D/C 20 PF NPO 5%	110-2000-04
C19	CAPACITOR D/C 10 PF NPO 5%	110-1000-04
CR1	DIODE 5082-2900	007-6022-00
I1	VT IC LM733CH	007-7082-01
L1	INDUCTOR	NPN
L2	INDUCTOR RF 22 UH	019-2016-02
L3	INDUCTOR MOLD 1 UH 10%	019-2016-10
L4	INDUCTOR RF 22 UH	019-2016-02
L5	INDUCTOR RF 22 UH	019-2016-02
L6	INDUCTOR 47 UH	019-2016-30
Q1	TRANSISTOR PNP MPS-H81	007-0077-00
R1	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R2	RESISTOR F/C 3.9K 1/4W 10%	130-0392-25
R3	RESISTOR F/C 6.8K 1/4W 10%	130-0682-25
R4	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R5	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R6	RESISTOR F/C 390 OHM 1/4W 10%	130-0391-25
R7	RESISTOR F/C 680 OHM 1/4W 10%	130-0681-25
R8	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R9	RESISTOR F/C 180 OHM 1/4W 10%	130-0181-25
R10	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R11	RESISTOR F/C 270 OHM 1/4W 10%	130-0271-25
R12	RESISTOR F/C 180 OHM 1/4W 10%	130-0181-25
R13	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R14	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R15	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R16	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R17	RESISTOR F/C 1K 1/4W 10%	120-0102-25
Y1	XTAL 89 MHZ	044-0006-00
	PC BD OSC	009-5082-00
	TERMINAL FEEDTHRU	010-0008-00
	ENCLOSURE OSC	047-0150-01
	CLIP CRYSTAL	090-0106-03
	RIVET BUTTON HEAD	092-0012-22

ASSEMBLY NO:	200-5078-00
DESCRIPTION:	HIGH FREQ LOOP BD SUB-ASSY (G4)
ASSY DWG NO:	300-5078-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C2	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C3	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C4	CAPACITOR D/C 100 PF X5F 10%	109-1010-35
C5	CAPACITOR D/C 100 PF X5F 10%	109-1010-35
C6	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C7	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C8	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C9	CAPACITOR TANT 6,8 UF 35V 20%	096-1007-29
C10	CAPACITOR F/T 470 PF	106-0002-00
C11	CAPACITOR F/T 470 PF	106-0002-00
C12	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C13	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C14	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C15	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C16	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C17	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
CR1	DIODE 1N4148	007-6016-00
CR2	DIODE 5082-2800	007-6021-00
CR3	DIODE 1N4148	007-6016-00
CR4	DIODE 1N4148	007-6016-00
I1	VT IC MC1035P	007-7075-01
I2	VT IC MC1010P	007-7074-01
I3	VT IC MC1010P	007-7074-01
I4	VT IC MC1004P	007-7073-01
I5	VT IC MC1004P	007-7073-01
I6	VT IC SN74H103	007-7085-01
I7	VT IC SN74196	007-7006-01
I8	VT IC MC3002P	007-7077-01
I9	VT IC MC3002P	007-7077-01
I10	VT IC MC3062P	007-7079-01
I11	VT IC MC3062P	007-7079-01
I12	VT IC 9601	007-7070-01
L1	INDUCTOR RF 240 UH	019-2015-47
Q1	TRANSISTOR PNP 2N5208	007-0026-00
Q2	TRANSISTOR 35677	007-0008-00
Q3	TRANSISTOR 35677	007-0008-00
Q4	TRANSISTOR PNP 2N4249	007-0009-00
Q5	TRANSISTOR 35677	007-0008-00
Q6	TRANSISTOR PNP 2N4249	007-0009-00
Q7	TRANSISTOR NPN 38869 RCA	007-0003-00
Q8	TRANSISTOR 35677	007-0008-00
Q9	TRANSISTOR 35677	007-0008-00
Q10	TRANSISTOR 35677	007-0008-00
Q11	TRANSISTOR 35677	007-0008-00
Q12	TRANSISTOR 35677	007-0008-00
Q13	TRANSISTOR 35677	007-0008-00
Q14	TRANSISTOR PNP 38870 RCA	007-0004-00
Q15	TRANSISTOR PNP 2N4249	007-0009-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
R1	RESISTOR F/C 47 OHM 1/4 W 10%	130-0470-25
R2	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R3	RESISTOR F/C 560 OHM 1/4W 10%	130-0561-25
R4	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R5	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R6-R17	RESISTOR F/C 560 OHM 1/4W 10%	130-0561-25
R18	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R19	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R20	RESISTOR F/C 470 OHM 1/4W 10%	130-0471-25
R21	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R22	RESISTOR F/C 22 OHM 1/4W 10%	130-0220-25
R23	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R24	RESISTOR F/C 470 OHM 1/4W 10%	130-0471-25
R25	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R26	RESISTOR F/C 22 OHM 1/4W 10%	130-0220-25
R27	RESISTOR F/C 180 OHM 1/4W 10%	130-0181-25
R28	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R29	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R30	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R31	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R32	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R33	RESISTOR F/C 47K 1/4W 10%	130-0473-25
R34	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R35	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R36	RESISTOR F/C 22 OHM 1/4W 10%	130-0220-25
R37	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R38	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R39	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R40	RESISTOR F/C 100K 1/4W 10%	130-0104-25
R41	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R42	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R43	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R44	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R45	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R46	RESISTOR F/C 33K 1/4W 10%	130-0333-25
R47	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R48	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R49	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R50	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R51	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R52	RESISTOR F/C 470 OHM 1/4W 10%	130-0471-25
R53	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R54	RESISTOR F/C 22 OHM 1/4W 10%	130-0220-25
R55	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R56	RESISTOR F/C 3.9K 1/4W 10%	130-0392-25
	PC BD HIGH FREQ LOOP	009-5078-00
	TRANS PAD	090-0189-00

ASSEMBLY NO: 200-0186-00
 DESCRIPTION: + ΔF VCO SUB-ASSY (G5)
 ASSY DWG NO: 300-5081-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR TANT 100 UF 20V 20%	096-1007-32
C2	CAPACITOR UNICERAM 1000 PF UY04	106-0009-00
C3	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C4	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C5	CAPACITOR TANT 100 UF 20V 20%	096-1007-32
C6	CAPACITOR D/C 20 PF NPO 5%	110-2000-04
C7	CAPACITOR D/C 3.3 PF NPO 5%	110-0330-04
C8	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C9	CAPACITOR CER .001 UF 15%	107-0005-00
C10	CAPACITOR TANT 100 UF 20V 20%	096-1007-32
C11	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C12	CAPACITOR CER .001 UF 15%	107-0005-00
C13	CAPACITOR TANT 100 UF 20V 20%	096-1007-32
C14	CAPACITOR MLR .01 UF 80V 10%	105-0031-08
C15	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C16	CAPACITOR D/C 68 PF	110-6800-35
C17	CAPACITOR CER 47 PF	106-0003-00
C18	CAPACITOR 1.2 PF 10%	106-0008-00
C19	CAPACITOR CER 100 PF	106-0004-00
C20	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C21	CAPACITOR CER 47 PF	106-0003-00
C22	CAPACITOR CER 100 PF	106-0004-00
C23	CAPACITOR 1.2 PF 10%	106-0008-00
C24	CAPACITOR D/C 180 PF X5F 10%	109-1810-35
C25	CAPACITOR D/C 10 PF NPO 5%	110-1000-04
C26	CAPACITOR D/C 120 PF X5F 10%	109-1210-35
C27	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C28	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C29	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C30	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C31	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C32	CAPACITOR F/T 470 PF	106-0002-00
C33	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
CO1	KLIXON HEATER	090-0096-00
CR1	DIODE 5082-3188 PIN	007-6031-00*
CR2	DIODE 5082-0112 SRD	007-6024-00
CR3	DIODE 5082-2900	007-6022-00
I1	VT IC LM733CH	007-7082-01
L1	INDUCTOR 10 UH	019-2015-18
L2	INDUCTOR	NPN
L3	INDUCTOR	NPN
L4	INDUCTOR .47 UH	019-2016-06
L5	INDUCTOR	NPN
L6	INDUCTOR	NPN
L7	INDUCTOR	NPN
L8	INDUCTOR RF .22 UH	019-2016-02
L9	INDUCTOR RF .22 UH	019-2016-02
L10	INDUCTOR 47 UH	019-2016-30
Q1	TRANSISTOR PNP 2N5208	007-0026-00*

*CR1 AND Q1 ARE A MATCHED PAIR.

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
Q2	TRANSISTOR PNP 2N5208	007-0026-00
Q3	TRANSISTOR NPN 2N3866	007-0028-00
R1	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R2	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R3	RESISTOR F/C 220 OHM 1/4W 10%	129-0221-25
R4	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R5	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R6	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R7	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R8	RESISTOR F/C 220 OHM 1/4W 10%	129-0221-25
R9	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R10	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R11	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R12	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R13	RESISTOR F/C 10 OHM 1/4W 10%	130-0100-25
R14	RESISTOR F/C 10 OHM 1/4W 10%	130-0100-25
R15	RESISTOR F/C 220 OHM 1/4W 10%	129-0221-25
R16	RESISTOR PREC 47.5 OHM 1%	125-0475-01
R17	RESISTOR PREC 47.5 OHM 1%	125-0475-01
R18	RESISTOR F/C 1K 1/4W 10%	129-0102-25
R19	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R20	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R21	RESISTOR F/C 390 OHM 1/4W 10%	130-0391-25
R22	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R23	RESISTOR F/C 220 OHM 1/4W 10%	129-0221-25
R24	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R25	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R26	RESISTOR F/C 180 OHM 1/4W 10%	130-0181-25
R27	RESISTOR F/C 270 OHM 1/4W 10%	130-0271-25
R28	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R29	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R30	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R31	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R32	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R33	RESISTOR F/C 10 OHM 1/4W 10%	130-0100-25
	GND TERMINAL #2X.531	008-0017-02
	PC BD Δ F VCD	009-5081-00
	TERMINAL STANDOFF	010-0007-00
	TERMINAL FEEDTHRU	010-0008-00
	ENCLOSURE + Δ F VCD	047-0155-01
	NUT 2-56	089-2004-21
	WASHER INT TOOTH #2	089-8500-00
	HEAT SINK	090-0097-00
	COIL FORM	090-0098-00

ASSEMBLY NO: 200-0186-00
 DESCRIPTION: - ΔF VCD SUB-ASSY (G6)
 ASSY DWG NO: 300-5081-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR TANT 100 UF 20V 20%	096-1007-32
C2	CAPACITOR UNICERAM 1000 PF UY04	106-0009-00
C3	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C4	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C5	CAPACITOR TANT 100 UF 20V 20%	096-1007-32
C6	CAPACITOR D/C 20 PF NPD 5%	110-2000-04
C7	CAPACITOR D/C 3.3 PF NPD 5%	110-0330-04
C8	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C9	CAPACITOR CER .001 UF 15%	107-0005-00
C10	CAPACITOR TANT 100 UF 20V 20%	096-1007-32
C11	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C12	CAPACITOR CER .001 UF 15%	107-0005-00
C13	CAPACITOR TANT 100 UF 20V 20%	096-1007-32
C14	CAPACITOR MLR .01 UF 80V 10%	105-0031-08
C15	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C16	CAPACITOR D/C 68 PF	110-6800-35
C17	CAPACITOR CER 47 PF	106-0003-00
C18	CAPACITOR 1.2 PF 10%	106-0008-00
C19	CAPACITOR CER 100 PF	106-0004-00
C20	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C21	CAPACITOR CER 47 PF	106-0003-00
C22	CAPACITOR CER 100 PF	106-0004-00
C23	CAPACITOR 1.2 PF 10%	106-0008-00
C24	CAPACITOR D/C 180 PF X5F 10%	109-1810-35
C25	CAPACITOR D/C 10 PF NPD 5%	110-1000-04
C26	CAPACITOR D/C 120 PF X5F 10%	109-1210-35
C27	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C28	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C29	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C30	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C31	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C32	CAPACITOR F/T 470 PF	106-0002-00
C33	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
CD1	KLIXON HEATER	090-0096-00
CR1	DIODE 5082-3188 PIN	007-6031-00*
CR2	DIODE 5082-0112 SRD	007-6024-00
CR3	DIODE 5082-2900	007-6022-00
I1	VT IC LM733CH	007-7082-01
L1	INDUCTOR 10 UH	019-2015-18
L2	INDUCTOR	NPN
L3	INDUCTOR	NPN
L4	INDUCTOR .47 UH	019-2016-06
L5	INDUCTOR	NPN
L6	INDUCTOR	NPN
L7	INDUCTOR	NPN
L8	INDUCTOR RF .22 UH	019-2016-02
L9	INDUCTOR RF .22 UH	019-2016-02
L10	INDUCTOR 47 UH	019-2016-30
Q1	TRANSISTOR PNP 2N5208	007-0026-00*

*CR1 AND Q1 ARE A MATCHED PAIR.

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
Q2	TRANSISTOR PNP 2N5208	007-0026-00
Q3	TRANSISTOR NPN 2N3866	007-0028-00
R1	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R2	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R3	RESISTOR F/C 220 OHM 1/4W 10%	129-0221-25
R4	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R5	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R6	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R7	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R8	RESISTOR F/C 220 OHM 1/4W 10%	129-0221-25
R9	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R10	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R11	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R12	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R13	RESISTOR F/C 10 OHM 1/4W 10%	130-0100-25
R14	RESISTOR F/C 10 OHM 1/4W 10%	130-0100-25
R15	RESISTOR F/C 220 OHM 1/4W 10%	129-0221-25
R16	RESISTOR PREC 47.5 OHM 1%	125-0475-01
R17	RESISTOR PREC 47.5 OHM 1%	125-0475-01
R18	RESISTOR F/C 1K 1/4W 10%	129-0102-25
R19	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R20	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R21	RESISTOR F/C 390 OHM 1/4W 10%	130-0391-25
R22	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R23	RESISTOR F/C 220 OHM 1/4W 10%	129-0221-25
R24	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R25	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R26	RESISTOR F/C 180 OHM 1/4W 10%	130-0181-25
R27	RESISTOR F/C 270 OHM 1/4W 10%	130-0271-25
R28	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R29	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R30	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R31	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R32	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R33	RESISTOR F/C 10 OHM 1/4W 10%	130-0100-25
	GND TERMINAL #2X.531	008-0017-02
	PC BD Δ F VCO	009-5081-00
	TERMINAL STANDOFF	010-0007-00
	TERMINAL FEEDTHRU	010-0008-00
	ENCLOSURE - Δ F VCO	047-0155-01
	NUT 2-56	089-2004-21
	WASHER INT TOOTH #2	089-8500-00
	HEAT SINK	090-0097-00
	COIL FORM	090-0098-00

ASSEMBLY NO:	200-0185-00
DESCRIPTION:	MASTER VCO SUB-ASSY (G7)
ASSY DWG NO:	300-5081-01

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR CER .001 UF 15%	107-0005-00
C2	CAPACITOR TANT 27 UF 35V 20%	096-1007-30
C3	CAPACITOR TANT 27 UF 35V 20%	096-1007-30
CR1	DIODE VARACTOR STV 100	007-4000-00
FL1	FILTER EMI	017-0002-00
FL2	FILTER EMI	017-0002-00
L1	INDUCTOR 10 UH	019-2015-18
L2	INDUCTOR	NPN
L3	INDUCTOR	NPN
Q1	TRANSISTOR MM 8009	007-0035-00
R1	RESISTOR 100 OHM 3 1/4W 10%	132-0012-00
R2	RESISTOR F/C 1.5K 1/4W 10%	129-1152-25
R3	RESISTOR F/C 4.7K 1/8W 10%	129-1472-05
R4	RESISTOR F/C 470 OHM 1/4W 10%	129-1471-25
R5	RESISTOR F/C 470 OHM 1/4W 10%	129-1471-25
R6	RESISTOR F/C 470 OHM 1/4W 10%	129-1471-25
R7	RESISTOR Q/C 2.7K 1/4W 10%	129-1272-25
R8	RESISTOR F/C 8.2K 1/8W 10%	129-1822-05
	GND TERMINAL #2X.531	008-0017-02
	FERRITE BEADS	013-0003-00
	RECEPTACLE PANEL JACK	030-0012-00
	HOUSING VCO	047-5007-01
	NUT HEX #4-40 KEPS	089-2058-21
	SCREW PHP 2-56 X 3/16	089-5054-03
	SCREW PHP 4-40 X 5/16	089-5058-05
	WASHER INT-TOOTH #2	089-8500-00
	DIODE CLIP	090-0009-00
	HEAT SINK	090-0097-00
	SPAGHETTI TUBING 22 AWG	150-0001-04

ASSEMBLY NO:	200-5074-00
DESCRIPTION:	CONTROL LOGIC BD SUB-ASSY (L3)
ASSY DWG NO:	300-5074-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
CR1-CR113	DIODE 1N4148	007-6016-00
I1-I6	VT IC 946	007-7001-01
I7-I9	VT IC MC1806P	007-7071-01
I10	VT IC 946	007-7001-01
I11	VT IC MC1806P	007-7071-01
I12	VT IC 930	007-7002-01
I13	VT IC 930	007-7002-01
I14-I24	VT IC SN7410N	007-7051-01
I25	VT IC 936	007-7003-01
I26-I28	VT IC 9109	007-7067-01
I29	VT IC MC1810P	007-7084-01
Q1-Q9	TRANSISTOR 35677	007-0008-00
R1	RESISTOR F/C 5.6K 1/4W 10%	130-0562-25
R2	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R3	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R4	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R5	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R6	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R7	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R8	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R9	RESISTOR F/C 5.6K 1/4W 10%	130-0562-25
R10	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R11	RESISTOR F/C 5.6K 1/4W 10%	130-0562-25
R12	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R13	RESISTOR F/C 5.6K 1/4W 10%	130-0562-25
R14	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R15	RESISTOR F/C 5.6K 1/4W 10%	130-0562-25
R16	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R17	RESISTOR F/C 5.6K 1/4W 10%	130-0562-25
R18	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R19	RESISTOR F/C 5.6K 1/4W 10%	130-0562-25
R20	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R21	RESISTOR F/C 5.6K 1/4W 10%	130-0562-25
R22	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R23	RESISTOR F/C 5.6K 1/4W 10%	130-0562-25
R24	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R25	RESISTOR F/C 5.6K 1/4W 10%	130-0562-25
R26	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R27	RESISTOR F/C 5.6K 1/4W 10%	130-0562-25
R28	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R29	RESISTOR F/C 5.6K 1/4W 10%	130-0562-25
R30	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R31	RESISTOR F/C 5.6K 1/4W 10%	130-0562-25
R32	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R33	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R34	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R35	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R36	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R37	RESISTOR F/C 1K 1/4W 10%	130-0102-25

200-5074-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
R38	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R39	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R40	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R41	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R42	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R43	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R44	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R45	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R46	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R47	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R48	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R49	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R50	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R51	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R52	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R53	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R54	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R55	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R56	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R57	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R58	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
	PC BD CONTROL LOGIC	009-5074-00

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R. F. INDEX

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R.F.

BLOCK DIAGRAM THEORY

PURPOSE:

To provide the required modulation of RF OUTPUT and 50% level detection of generated pulses, by means of the MODULATOR, G18, to provide demodulation, the generation of a sync signal, 50% level detection, and pulse peak detection by means of the DEMODULATOR, and the generation of an indication of the frequency of the DME or TRANSPONDER under test by means of the FREQUENCY MONITOR.

OPERATION:

A. MODULATOR, G18

The MODULATOR, G18, operates in 3 different modes, DME MODE, TRANSPONDER MODE and CW MODE. In the DME and TRANSPONDER MODES, RF pulses are generated, in the CW MODE a CW RF level is generated. The selection of the DME or TRANSPONDER MODE determines whether the RF MODULATOR, G10, is to be controlled by the output of the DME PULSE/CW LEVEL COMPARATOR or the LEVEL SW. BUFFER. The selection is made by means of the DME/TRANSPONDER MODE switch.

B. MODULATOR, G18, DME MODE

A pulse on the DME PULSE WIDTH CONTROL causes the DME PULSE SHAPE GENERATOR to generate a Gaussian shaped pulse of an amplitude which is controlled by either the MAIN PULSE LEVEL switch or the ECHO PULSE LEVEL switch as determined by whether the pulse is to be of main reply level or one at the echo level. The output of the DME PULSE SHAPE GENERATOR is fed into the DME PULSE/CW LEVEL COMPARATOR. The RF output of the RF MODULATOR, G10, is detected by LEVELING DETECTOR, G17, which becomes an input to the DME PULSE/CW LEVEL COMPARATOR. If the DME PULSE SHAPE GENERATOR input to the comparator exceeds the LEVELING DETECTOR input, the RF output of the RF MODULATOR is caused to increase. Thus a closed loop system is generated.

The RF SWITCH DRIVER causes the RF SWITCH in the RF MODULATOR to close at the proper time and serve to generate the necessary RF ON-OFF ratio.

C. MODULATOR, G18, TRANSPONDER MODE

A pulse on the RF SWITCH DRIVER CONTROL causes the RF SWITCH in the RF MODULATOR to generate the TRANSPONDER pulse of the proper shape.

The P1, P2 and P3 COMPARE inputs to the P1, P2 and P3 COMPARATOR/LEVEL CONTROL sections of the MODULATOR, cause the detected level of the RF pulse to be compared with the required level of either the P1, P2 or P3 pulse. The P1, P2 and P3 LEVEL inputs cause the RF LEVEL section of the RF MODULATOR to be controlled by the P1, P2 or P3 LEVEL SWITCH outputs in the MODULATOR.

D. MODULATOR, G18, CW MODE

When a CW LEVEL RF OUTPUT is required, the DME MODE must also be selected. The CW OUTPUT SWITCH causes the DME PULSE SHAPE GENERATOR output to be shut off and a DC level to be generated as the compare level for the DME PULSE/CW LEVEL COMPARATOR. The RF switch is made to close.

E. ISOLATOR, G8

The ISOLATOR supplies 60 DB of isolation between the RF MODULATOR, G10, and the MASTER VCO, G7, at the fundamental frequency.

F. ISOLATION LPF, G9

The ISOLATION LPF provides 60 DB isolation between the RF MODULATOR, G10, the MASTER VCO, G7, at the harmonic frequency.

G. LEVELING LPF, G11

The LEVELING LPF provides 40 db isolation between the RF MODULATOR, G10, and the LEVELING DETECTOR, G17 at the harmonic frequency.

H. EMI FILTER, G25

The EMI FILTER provides additional attenuation of the RF LEVEL present on the LEVELING DETECTOR, G17, output.

I. LEVELING COUPLER, G12

The LEVELING COUPLER provides a coupled output which is not sensitive to the VSWR presented by the LEVELING DETECTOR input.

J. SNIFFER, G13

The SNIFFER provides a signal for use in the FREQUENCY MONITOR, G19, which is attenuated by approximately 60 db.

K. POWER COUPLER, G15

The POWER COUPLER provides a coupled output to the POWER DETECTOR, G21, which is not sensitive to the VSWR presented by the ATTENUATOR, G14.

L. INPUT PAD, G16

The INPUT PAD provides 10 db attenuation of the input power from the DME or TRANSPONDER under test.

M. POWER PAD, G20

The POWER PAD provides 10 db attenuation of the coupled power output of the POWER COUPLER, G15.

N. ATTENUATOR, G14

The ATTENUATOR provides a variable attenuation of the RF OUTPUT signal.

O. POWER DETECTOR, G21

The POWER DETECTOR provides demodulation of the RF input from the DME or TRANSPONDER under test. The POWER DETECTOR is linear over an input power range of 1 mw to 10 watts.

P. ULTIMATE FILTER, G22

The ULTIMATE FILTER supplies attenuation of in box signals to prevent them from appearing at the RF OUTPUT.

Q. DEMODULATOR, G23

The DEMODULATOR provides an attenuated POWER DETECTOR, G21, output at the DETECTED PULSE MONITOR. The DEMODULATOR 50% LEVEL DETECTOR section detects the 50% level of the pulse output of the POWER DETECTOR, G21. The PULSE PEAK DETECTOR section provides a DC voltage output which is directly related to the peak amplitude of the POWER DETECTOR, G21, output pulse. This voltage is used in the computation of the peak RF power.

R. FREQUENCY MONITOR, G19

The MIXER section generates the difference frequency between the FREQUENCY GENERATOR output and the DME or TRANSPONDER under test. This frequency is nominally 63 MHz for DME and 60 MHz for TRANSPONDER. After amplification, this signal is mixed with the output of the 60/63 MHz OSCILLATOR. Filtering, amplification, and additional filtering to provide a beat frequency output to the FREQUENCY MONITOR. If the FREQUENCY GENERATOR is operated in the UNCAL mode, a near zero beat frequency can be made to appear at the FREQUENCY MONITOR and by the use of the ΔF READOUT the operating frequency of the DME or TRANSPONDER under test may be determined.

THEORY OF OPERATION

MODULATOR, G18, THEORY

PURPOSE:

To generate outputs to the RF MODULATOR, G10, which cause the RF output to vary in accordance with various inputs to the MODULATOR, G18.

To provide an output to the VIDEO OUTPUT MONITOR which is derived from the output of the LEVELING DETECTOR, G17.

To provide a MODULATOR 50% LEVEL PULSE output which is derived from the output of the LEVELING DETECTOR, G17.

OPERATION:

A. DME MODE

1. DME PULSE SHAPE GENERATOR

When a negative pulse appears on the DME PULSE WIDTH CONTROL line; G18-31, transistor Q9 shuts off. The waveform shown appears at the collector of Q9 and after filtering, by LPF, C3, L1 and C4, appears at reduced amplitude at the input to the DME PULSE/CW LEVEL COMPARATOR. Diode CR4 serves as a damping diode on the output of the LPF to prevent ringing. When CR4 is conducting, transistor Q10 is turned on which causes the waveform shown to appear on the collector of Q12. This waveform causes the minus input to the DME PULSE/CW LEVEL COMPARATOR to be biased so as to definitely cause the RF LEVEL diode, CR1, in the RF MODULATOR, G10, to be forward biased.

The amplitude of the waveform on the collector of Q9 is dependent on the voltage present on the emitter of Q8. This voltage is determined by the output of either the MAIN PULSE LEVEL SWITCH or the ECHO PULSE LEVEL SWITCH. Thus the amplitude of the pulses present on the input to the DME PULSE/CW LEVEL COMPARATOR may be caused to vary.

2. DME PULSE/CW LEVEL COMPARATOR

When the voltage on the minus input to I5, Pin 2, is caused to exceed that on the plus input, the voltage on the anode of RF LEVELING diode, CR1, in the RF MODULATOR, G10, is caused to decrease. This is due to the decreased voltage on the base of Q15 which causes a decreased voltage on the emitter of Q16. Q17 provides rapid decrease when needed. This causes decreased attenuation of the RF signal level by CR1 and results in an increase in the output level of the LEVELING DETECTOR, G17. This level is the input to the plus input I5, Pin 1. Should the plus input level exceed that of the minus input, the voltage on CR1 is increased causing increased attenuation of the RF signal. Thus the output of the LEVELING DETECTOR, G17, is caused to vary as the input to the DME PULSE/CW LEVEL COMPARATOR.

3. MAIN PULSE LEVEL SWITCH

A "1" is present on the MAIN PULSE CONTROL line, G18-30, input to the MAIN PULSE LEVEL switch at all times except when the pulse to be generated is an echo pulse. This "1" causes Q2 and Q3 to be turned on, thus causing the voltage on the emitter of Q8 to be determined by the setting of the MAIN LEVEL pot, R2. If an echo pulse is to be generated, the negative pulse on the MAIN PULSE CONTROL line causes Q2 and Q3 to shut off.

4. ECHO PULSE LEVEL SWITCH

The ECHO PULSE CONTROL line, G18-32, input is always at a "0" except when an echo pulse is to be generated. The positive pulse present causes Q5 and Q6 to turn on, thus the voltage on the emitter of Q8 to be determined by the setting of the ECHO INJECTION SUPPRESSION control.

5. RF SWITCH DRIVER

The negative pulse present on the RF SWITCH DRIVER CONTROL line, G18-14, causes the voltage on the RF SWITCH diodes, CR2, CR3 and CR4, in the RF MODULATOR, G10, to go to -5V. These negative pulses are present when there are pulses present on the DME PULSE CONTROL line, G18-31, and are synchronous with them. The negative pulses cause Q26, Q27 and Q29, to be turned on. Q28 is turned on when the RF SWITCH CONTROL line is at a "1" thus causing the RF SWITCH diodes to be forward biased with the result being that the RF signal is greatly attenuated.

6. MODULATOR 50% LEVEL DETECTOR

The output of the LEVELING DETECTOR, G17, appears at reduced amplitude on the base of Q14 and then at the plus input to the VOLTAGE COMPARATOR, Pin 2 of I3. VOLTAGE COMPARATOR, I3, and diode CR9 generate a voltage level which is equal to the peak voltage of the pulse present at Pin 2 of I3. The voltage present at the plus input to the VOLTAGE COMPARATOR Pin 2 of I4, is directly related to voltage output of I3 and CR9. The voltage present at the minus input to Pin 3 of I4, is the same as is present at I3, Pin 2, but is 2 usec delayed. When the voltage on I4, Pin 3, exceeds that on I4, Pin 2, the COMPARATOR output I4, Pin 6, goes to a "0". Thus the negative going edges of the pulses present on the MODULATOR 50% LEVEL PULSE line, G18-34, are caused to occur 2 usec delayed from the 50% point of the pulse output of the LEVELING DETECTOR, G17.

B. TRANSPONDER MODE

1. P1 COMPARATOR/LEVEL CONTROL

The output of the LEVELING DETECTOR, G17, appears at the plus input to the voltage comparator, I6, Pin2, at reduced amplitude. During the interval that the TRANSPONDER P1 RF pulse is being generated the P1 COMPARE line, G18-9, is at a "0" thus causing the voltage at the minus input of I6, Pin 3 to be determined by the output of the TRANSPONDER P1

B. 1. Cont'd

LEVEL pot, R61. When the amplitude of the signal present at I6, Pin 2, exceeds that of I6, Pin 3, the output, Pin 7 of I6, goes high causing transistor Q18 to charge capacitor C20. Thus should the amplitude of the TRANSPONDER P1 RF pulse exceed that called for by the TRANSPONDER P1 LEVEL pot, C20 is charged to a higher voltage. This results in the RF LEVEL diode, CR1, in the RF MODULATOR, G10, to be more forward biased resulting in increased attenuation of the RF signal and thus a decrease in the amplitude of the pulse output of the LEVELING DETECTOR, G17.

2. P2 COMPARATOR/LEVEL CONTROL

Same as P1 COMPARATOR/LEVEL CONTROL except the comparison is during the TRANSPONDER P2 RF pulse interval.

3. P3 COMPARATOR/LEVEL CONTROL

Same as P1 COMPARATOR/LEVEL CONTROL except the comparison is during the TRANSPONDER P3 RF pulse interval.

4. P1 LEVEL SWITCH

When the P1 LEVEL line, G18-17, goes to a "1" during the TRANSPONDER P1 RF pulse interval, the voltage on the base of Q19 is allowed to go to that on C20. Thus the voltage on the RF LEVEL diode, CR1, in the RF MODULATOR, G10, is caused to be determined by that voltage on C20.

5. P2 LEVEL SWITCH

Same as P1 LEVEL switch, except operation occurs during TRANSPONDER P2 RF pulse intervals.

6. P3 LEVEL SWITCH

Same as P1 LEVEL switch, except operation occurs during TRANSPONDER P3 RF pulse interval.

7. LEVEL SWITCH BUFFER

Transistor Q25 provides buffering between the P1, P2 and P3 LEVEL switch and the RF LEVEL diode, CR1, in the RF MODULATOR, G10.

8. RF SWITCH DRIVER

The negative pulses present on the RF SWITCH DRIVER CONTROL line, G18-14, cause the output, the RF SWITCH CONTROL line, G18-20, to go to -5V due to the turning on of Q26, Q27 and Q29. The fall and rise time of the pulse on the RF SWITCH CONTROL line determines the rise and fall time of the TRANSPONDER RF pulses. The duration of the pulse on the RF SWITCH CONTROL line determines the duration of the TRANSPONDER RF pulses.

9. LEVELING DETECTOR BIAS DETECTOR

Should the voltage on the plus input to I12, Pin 3, become less than that on the minus input, I12, Pin 2, the output Pin 6 of I12, goes negative resulting in a more negative voltage on C29 and the minus input, I12, Pin 2. Thus there is a voltage present on C29 which varies with the most negative value of the output of the LEVELING DETECTOR, G17.

C. CW MODE

1. CW OUTPUT SWITCH

When the TACAN MOD/CW OUTPUT CONTROL is placed in the CW OUTPUT position, the "0" appearing on the CW OUTPUT line, G18-13, causes Q7 to be turned on. This results in a voltage level appearing on the minus input to I5, Pin 2, in the DME PULSE/CW LEVEL COMPARATOR. Current flow thru R18 and CR3 cause Q9 to always be turned on, thus preventing any pulses from appearing on the collector of Q9.

2. RF SWITCH DRIVER

The "0" on the CW OUTPUT line, G18-13, causes Q26, Q27, and Q29 to be turned on resulting in -5V on the RF SWITCH diodes, CR2, CR3 and CR4, in the RF MODULATOR, G10.

RF MODULATOR, G10, THEORY

PURPOSE:

To attenuate the RF signal in accordance with input signals.

OPERATION:

A. RF SWITCH

Diodes, CR2, CR3 and CR4, are PIN diodes and have the characteristic of providing a shunt impedance which varies as the current flow thru the diode varies. Increased current causes a lower shunt impedance thus providing attenuation of the RF signal. CR2, CR3 and CR4 are used in a RF switching mode and are either strongly forward biased or reverse biased.

B. RF LEVEL

Diode CR1 is a PIN diode and is used to control the level of the RF signal during the interval that the RF SWITCH is "CLOSED". Increased current thru CR1 causes increased attenuation of the RF signal.

FREQUENCY MONITOR, G19, THEORY

PURPOSE:

To generate a beat frequency between the FREQUENCY GENERATOR frequency \pm 60/63 MHz and the input signal from the DME or TRANSPONDER under test.

OPERATION:

The FREQUENCY MONITOR MIXER INJECTION and the FREQUENCY MONITOR MIXER PULSE INJECTION signals are mixed in mixer diode, CR1. The difference frequency is amplified by the 63 MHz AMPLIFIER, I1 and I2. The difference frequency is nominally 63 MHz for DME and 60 MHz for TRANSPONDER operation. This signal is mixed in diode CR2 with the output of the 60/63 MHz CRYSTAL OSCILLATOR. The difference frequency after filtering by the LPF, consisting of L3, L4 and various capacitors, is amplified by I3. The output of I3, after being filtered by the LPF, consisting of L5, L6 and various capacitors, is the signal present at the FREQUENCY MONITOR output.

The selection of either the 60 MHz or 63 MHz crystal is made by causing the saturation of either Q3 or Q2 respectively.

By operating the test set in the UNCAL mode the ΔF control may be used to cause the signal on the FREQUENCY MONITOR output to approach a zero beat.

DEMODULATOR, G23, THEORY

PURPOSE:

To derive from the pulses present on the DEMODULATED PULSE input line:

- a. Pulses on the DEMODULATOR SYNC PULSE line which occur at the very beginning of the input pulses.
- b. Pulses on the DEMODULATOR 50% LEVEL line which occur 2 usec delayed from the 50% level of the input pulses.
- c. A voltage level on the PULSE PEAK LEVEL line which varies directly as the peak of the input pulses vary. This voltage is used in the computation of peak power.

OPERATION:

A. DEMODULATOR PULSE DETECTOR

When the DEMODULATED PULSE input, G23-9, appears, the minus input voltage to I4, Pin 3, exceeds the plus input and the output, I4, Pin 7, is caused to go to "0". This causes the output of I3C, Pin 10, and the DEMODULATOR SYNC PULSE line, G23-2, to go to a "0".

B. DEMODULATOR 50% LEVEL DETECTOR

When the DEMODULATED PULSE input, G23-9, appears, a pulse appears at reduced amplitude at the plus input to I1, Pin 2. The purpose of CR1 and the VOLTAGE COMPARATOR I1, is to generate a voltage on the DEMODULATOR 50% LEVEL pot, R9, which is equal to the peak voltage of the pulse at I1, Pin 2. This pulse appears at the minus input of I2, Pin 3, after being delayed 2 usec by DL1. DEMODULATOR 50% LEVEL pot, R9, is set to cause the voltage on the plus input, I2, Pin 2, to be approximately half of that on C2. Thus the 50% point of the pulse on I2, Pin 3, causes the output of VOLTAGE COMPARATOR I2, Pin 7 to go to a "0". This "0" causes a "1" on the DEMODULATOR 50% LEVEL PULSE line, G23-4.

C. PULSE PEAK DETECTOR

VOLTAGE COMPARATOR, I6, CR2, Q2, and OPERATION AMPLIFIER, I7, operate together to cause a voltage to be generated on C6 which is equal to the peak voltage of the pulses appearing at the plus input to I6, Pin 2. If this voltage exceeds that on the minus input, I6, Pin 3, the output, I6, Pin 7, goes high causing Q2 to increase the voltage on C5. OPERATIONAL AMPLIFIER I7 causes the voltage on C6 to be that on C5. Thus the voltage on I6, Pin 3, and the PULSE PEAK LEVEL output, G23-5, is increased.

So long as the interval between DEMODULATED PULSES is less than 0.4 sec I5 is continually retriggered and the \bar{Q} output, I5, Pin 6, remains at a "0" and Q3 remains turned off. If the interval is longer than 0.4 sec, the \bar{Q} output of I5, Pin 6, goes to a "1" and Q3 is turned on causing C5 to be discharged thus causing the voltage on the PULSE PEAK LEVEL line, G23-5, to be near zero volts.

CALIBRATIONS

1. CW OUTPUT LEVEL

- a. Place CW OUTPUT/TACAN MODULATOR switch in the CW OUTPUT position.
- b. Place MODE SELECT switch in DME mode
- c. Adjust CW OUTPUT LEVEL pot, R19, on MODULATOR, G18, to obtain -10dbm at test set RF OUTPUT. Check across frequency range for optimum centering of RF level.

2. DME ECHO RF PULSE LEVEL

All pots on MODULATOR, G18

- a. Reduce SQUITTER RATE to zero by placing the RANGE switch in the OFF position.
- b. Place SYNC OUTPUT switch in TD position.
- c. Place EQUALIZING PULSE/ANALOG P.P. switch in the ANALOG P.P. position
- d. Place ECHO INJECTION ON/OFF switch in ON position.
- e. Set test set DISTANCE to 29Nmi. This should allow observation on scope, attached to VIDEO OUTPUT MONITOR, of both the MAIN RF pulses and the INJECTED ECHO RF pulses.
- f. With the ECHO SUPPRESSION control set to 0db, set the DME PULSE LEVEL pot, R26, to cause the echo RF pulse peaks to coincide with the CW OUTPUT LEVEL which may be obtained by placing the TACAN MOD/CW OUTPUT control in the CW OUTPUT position.
- g. Change the ECHO INJECTION SUPPRESSION control to the desired calibration level, such as -6db, and adjust the ECHO LINEARITY pot, R103, to cause the echo RF pulses to be 6db below the 0db level.
- h. Repeat f and g until calibration is achieved.

3. DME MAIN RF PULSE LEVEL

- a. Select SQUITTER position of SYNC OUTPUT switch and observe the VIDEO OUTPUT MONITOR on a scope.
- b. Adjust the SQUITTER RATE control for 2700 PPS.
- c. Adjust the MAIN LEVEL pot, R2, so the RF pulse peaks coincide with the CW OUTPUT level.

4. TRANSPONDER P1, P2 and P3 RF PULSE LEVEL

All pots located on MODULATOR, G18.

- a. Establish a reference level of the CW OUTPUT level on scope. Be sure to do this in the DME mode.
- b. Select TO position of the SYNC OUTPUT switch and TRANSPONDER MODE of the MODE SELECT switch.
- c. Observe the VIDEO OUTPUT MONITOR on scope.
- d. Adjust the output of the TRANSPONDER P1 LINEARITY pot, R58, for 7.1V. Adjust the TRANSPONDER P1 LEVEL pot, R61, so the peak of the TRANSPONDER P1 RF pulse coincides with the CW OUTPUT level.
- e. Set the TRANSPONDER P2 SUPPRESSION control for 0 db and adjust the TRANSPONDER P2 LEVEL pot, R72, so the peak of the TRANSPONDER P2 RF pulse coincides with the CW OUTPUT level.
- f. Change the TRANSPONDER P2 SUPPRESSION control to the desired calibration level, such as -6db, and adjust the TRANSPONDER P2 LINEARITY pot, R73, to cause the TRANSPONDER P2 RF pulses to be 6db below the 0 db level.
- g. Repeat e and f until calibration is achieved.
- h. Set TRANSPONDER P3 SUPPRESSION control for 0db and adjust the TRANSPONDER P3 LEVEL pot, R83, so that the peak of the TRANSPONDER P3 RF pulse coincides with the CW OUTPUT level.
- i. Change the TRANSPONDER P3 SUPPRESSION control to the desired calibration level, such as -6db, and adjust the TRANSPONDER P3 LINEARITY pot, R84, to cause the TRANSPONDER P3 RF pulses to be 6db below the CW OUTPUT level.
- j. Repeat h and i until calibration is achieved.

ZERO MILE CALIBRATION

1. DEMODULATOR 50% LEVEL DETECTOR

- a. Set SYNC OUTPUT control to TO and attach scope to DETECTED PULSE MONITOR. This will allow observation of DME INTERROGATION pulse.
- b. Attach scope probe to the DEMODULATOR 50% LEVEL PULSE line, G23-4.

1. Cont'd

- c. While the DME is interrogating the test set adjust the DEMODULATOR 50% LEVEL pot, R9, on DEMODULATOR, G23, to position the leading edge of the positive pulse observed by the scope probe to be 2.0 usec delayed from the 50% point of the leading edge of the INTERROGATION pulse as observed at the DETECTED PULSE MONITOR.

2. MODULATOR 50% LEVEL DETECTOR

- a. Set the SCOPE SYNC control to SQUITTER and attach scope to VIDEO OUTPUT MONITOR. This will allow observation of the SQUITTER pulses generated by the test set.
- b. Attach scope probe to the MODULATOR 50% LEVEL PULSE line, G18-34.
- c. Adjust the SQUITTER RATE to a value such as 2700 PP/S.
- d. Adjust the MODULATOR 50% LEVEL pot, R40, of the MODULATOR, G18, to position the leading edge of the negative pulse observed by the scope probe to be 2.0 usec delayed from the 50% point of the leading edge of the SQUITTER pulse observed at the VIDEO OUTPUT MONITOR.

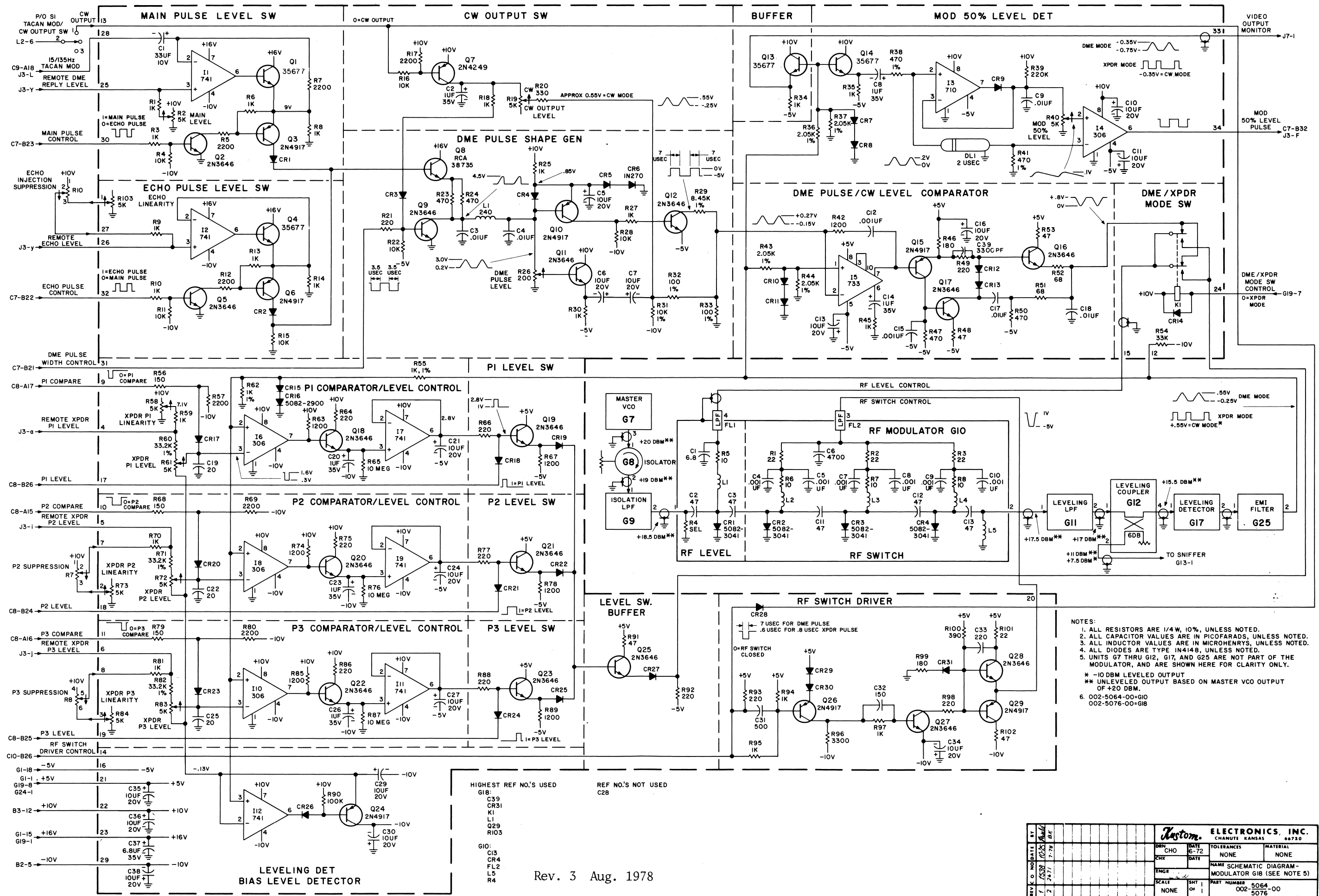
3. ZERO MILE DELAY

- a. A time interval counter attached to the points that scope probes were attached in parts 1 & 2, should indicate the time interval, between the leading edges, is 50.0 usec in X MODE and 56.0 usec in Y MODE.

This delay is digitally arrived at in the test set and is not sensitive to environmental changes.

POWER CALIBRATION

1. While subjecting the test set to a known amount of power adjust the POWER CALIBRATION pot, R14, of the DEMODULATOR, G23, to obtain the proper reading on the READOUT with the READOUT SELECTION switch in the POWER position.
2. Should there be a discrepancy between input power and the READOUT indication when the power level is changed from the calibration level, the Power Meas Δ T Generator Calibration should be made. (See Video Section.)



NOTES:
1. ALL RESISTORS ARE 1/4W, 10%, UNLESS NOTED.
2. ALL CAPACITOR VALUES ARE IN PICOFARADS, UNLESS NOTED.
3. ALL INDUCTOR VALUES ARE IN MICROHENRYS, UNLESS NOTED.
4. ALL DIODES ARE TYPE IN4148, UNLESS NOTED.
5. UNITS G7 THRU G12, G17, AND G25 ARE NOT PART OF THE MODULATOR, AND ARE SHOWN HERE FOR CLARITY ONLY.
* -10 DBM LEVELED OUTPUT
** UNLEVELED OUTPUT BASED ON MASTER VCO OUTPUT OF +20 DBM.
6. 002-5064-00=G10
002-5076-00=G18

HIGHEST REF NO.'S USED
G18:
C39
CR31
K1
L1
Q29
R103
G10:
C13
CR4
FL2
L5
R4

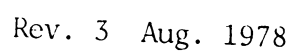
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C28

Rev. 3 Aug. 1978

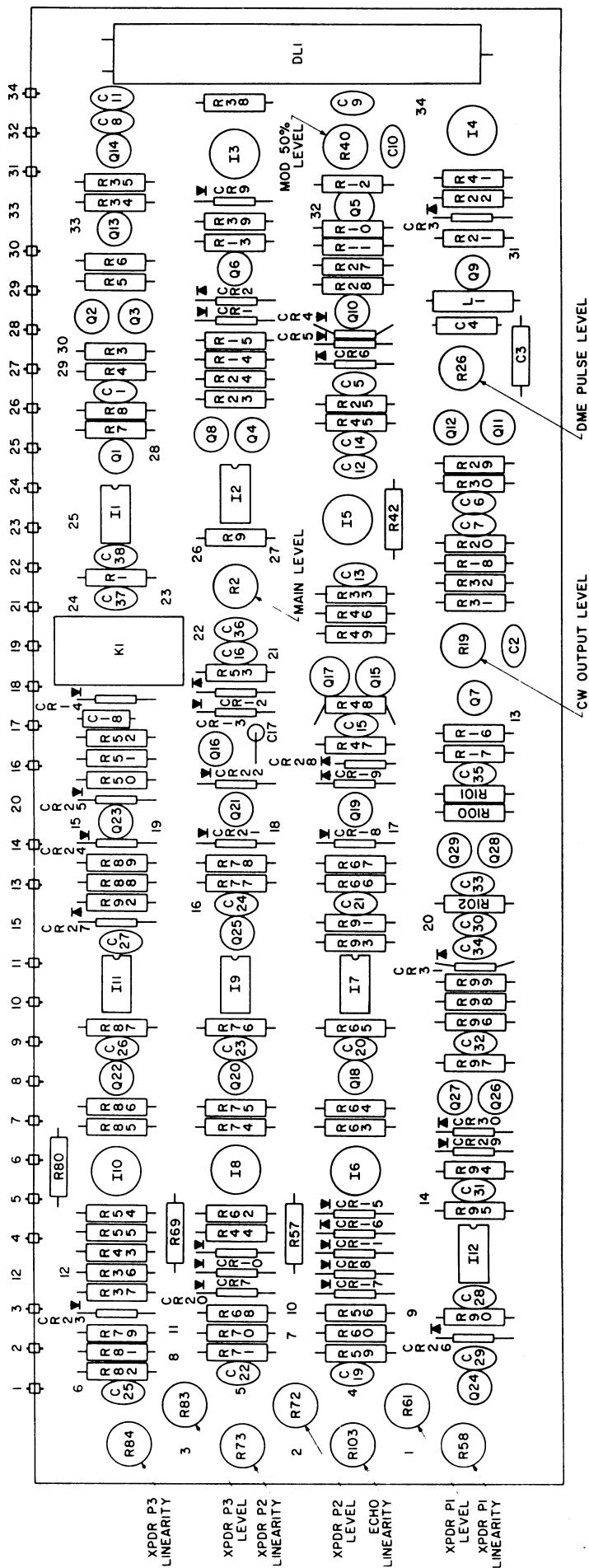
BY		DATE		TOLERANCES		MATERIAL	
CHK		DATE		NONE		NONE	
ENGR		DATE		NAME		SCHEMATIC DIAGRAM - MODULATOR G18 (SEE NOTE 5)	
SCALE		SHT		PART NUMBER		002-5064-00	
REV		DATE		SHT		OF	
1		6-72		1		1	
2		7-78		1		1	

Kustom.
ELECTRONICS, INC.
CHANUTE, KANSAS 66720

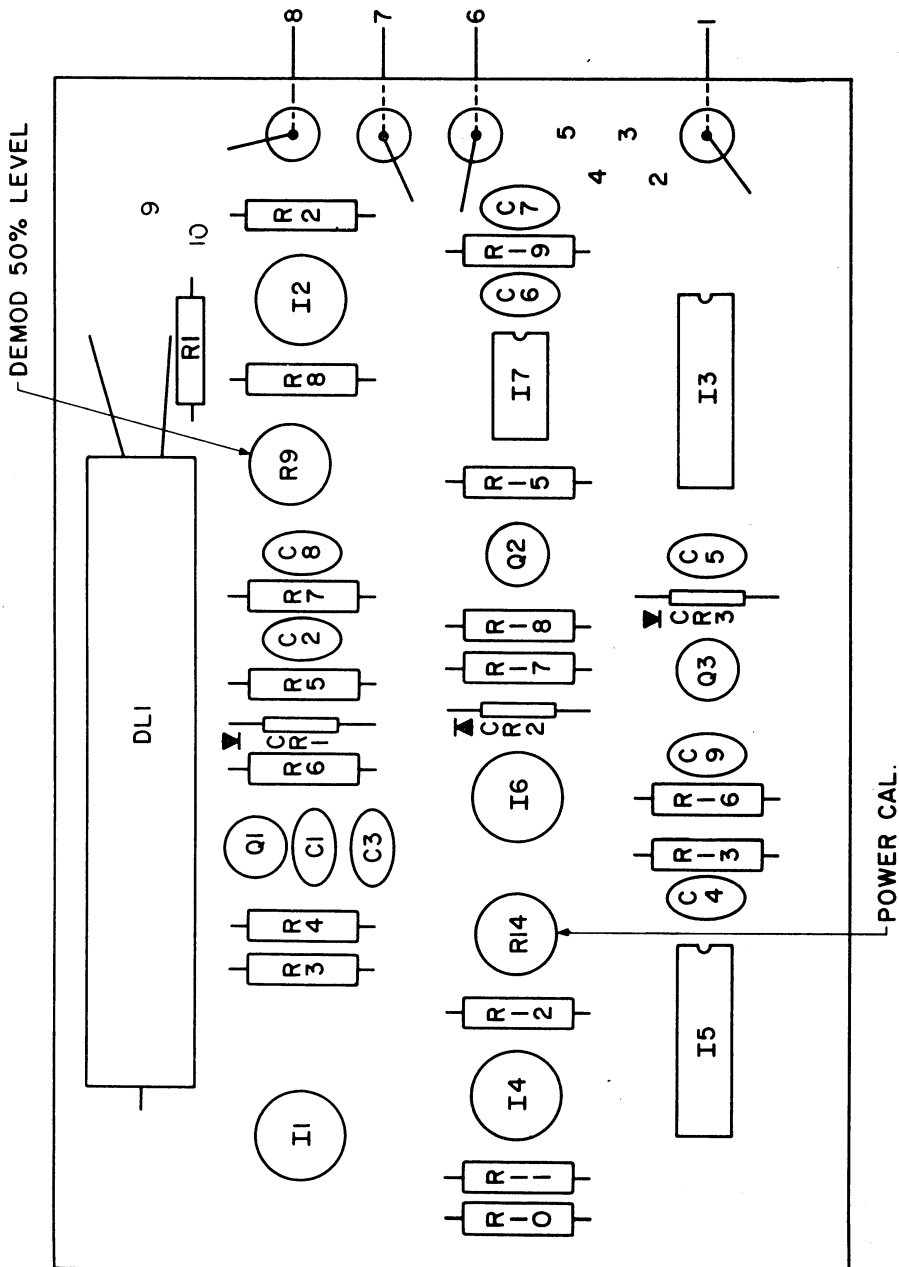
002-5064-00
5076



ENCLOSURE



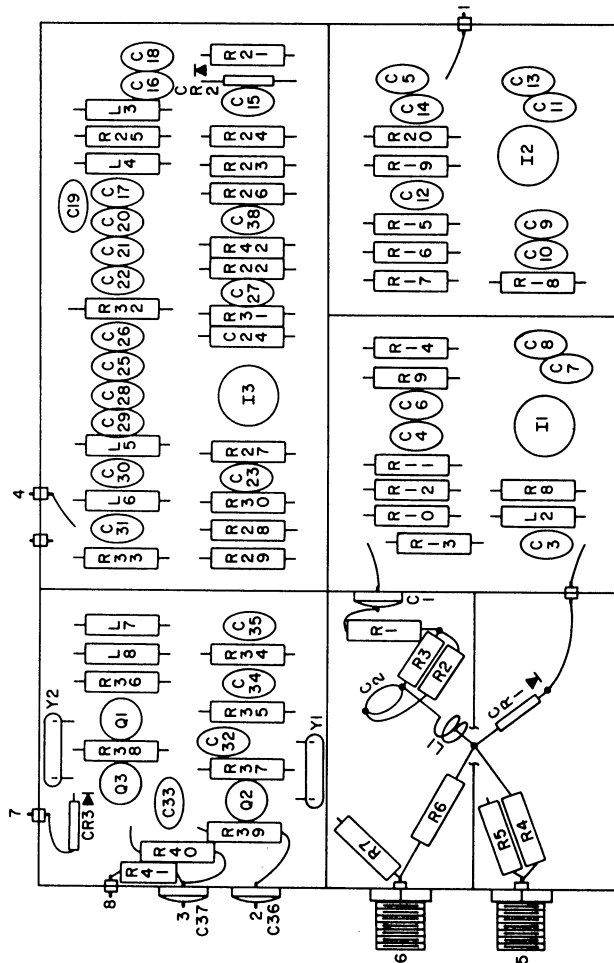
Custom. ELECTRONICS INC. CHANDLER KANSAS		DATE 6-72		JLS		TOLERANCES		NONE		MATERIALS		NONE	
MODULATOR, G18													
300-5076-00													



Rev. 3 Aug. 1978

REV. 3 AUG. 1978

CUSTOMER'S NAME		DATE		TOLERANCES		MATERIAL	
ELECTRONICS, INC.		6-72		NONE		NONE	
CHANUTE, KANSAS 66720		DATE		NAME			
				DEMODULATOR, G23			
REV. 3		SCALE		PART NUMBER			
1/1325		NONE		300-5073-00			



JUL 7-72		DATE		TOLERANCES		MATERIAL	
NONE		NONE		NONE		NONE	
JUL 7-72		DATE		NAME		FREQ. MONITOR, G19	
NONE		NONE		NONE		300-5080-00	
REV		K O NO DATE		SCALE		GHT OF	
1		1		1		1	

ELECTRONICS INC
HARTFORD, CT 06183

PARTS LIST

ASSEMBLY NO: 200-5076-00
 DESCRIPTION: MODULATOR BD SUB-ASSY (G18)
 ASSY DWG NO: 300-5076-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C2	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C3	CAPACITOR MLR .01 UF 80V 10%	105-0031-08
C4	CAPACITOR MLR .01 UF 80V 10%	105-0031-08
C5	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C6	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C7	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C8	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C9	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C10	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C11	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C12	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C13	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C14	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C15	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C16	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C17	CAPACITOR MLR .01 UF 80V 10%	105-0031-08
C18	CAPACITOR MLR .01 UF 80V 10%	105-0031-08
C19	CAPACITOR D/C 20 PF NPD 5%	110-2000-04
C20	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C21	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C22	CAPACITOR D/C 20 PF NPD 5%	110-2000-04
C23	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C24	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C25	CAPACITOR D/C 20 PF NPD 5%	110-2000-04
C26	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C27	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C29	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C30	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C31	CAPACITOR D/C 500 PF X5F 10%	109-5010-35
C32	CAPACITOR D/C 150 PF X5F 10%	109-1510-35
C33	CAPACITOR D/C 220 PF X5F 10%	109-2212-35
C34	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C35	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C36	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C37	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C38	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
CR1-CR5	DIODE 1N4146	007-6016-00
CR6	DIODE GERMANIUM 1N270	007-6020-00
CR7-CR15	DIODE 1N4148	007-6016-00
CR16	DIODE 5082-2900	007-6022-00
CR17-CR31	DIODE 1N4148	007-6016-00
DL1	DELAY 2 US	015-0007-00
I1	IC N5741V UT	007-7042-01
I2	IC N5741V UT	007-7042-01
I3	VT IC N5710T	007-7046-01
I4	VT IC LM306H	007-7044-01
I5	VT IC LM733CH	007-7082-01
I6	VT IC LM306H	007-7044-01

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
I7	IC N5741V UT	007-7042-01
I8	VT IC LM306H	007-7044-01
I9	IC N5741V UT	007-7042-01
I10	VT IC LM306H	007-7044-01
I11	IC N5741V UT	007-7042-01
I12	IC N5741V UT	007-7042-01
K1	RELAY DPDT	032-0000-00
L1	INDUCTOR RF 240 UH	019-2015-47
Q1	TRANSISTOR 35677	007-0008-00
Q2	TRANSISTOR 2N3646	007-0025-00
Q3	TRANSISTOR 2N4917	007-0027-00
Q4	TRANSISTOR 35677	007-0008-00
Q5	TRANSISTOR 2N3646	007-0025-00
Q6	TRANSISTOR 2N4917	007-0027-00
Q7	TRANSISTOR 2N4249	007-0009-00
Q8	TRANSISTOR 38735	007-0002-00
Q9	TRANSISTOR 2N3646	007-0025-00
Q10	TRANSISTOR 2N4917	007-0027-00
Q11	TRANSISTOR 2N3646	007-0025-00
Q12	TRANSISTOR 2N3646	007-0025-00
Q13	TRANSISTOR 35677	007-0008-00
Q14	TRANSISTOR 35677	007-0008-00
Q15	TRANSISTOR 2N4917	007-0027-00
Q16-Q23	TRANSISTOR 2N3646	007-0025-00
Q24	TRANSISTOR 2N4917	007-0027-00
Q25	TRANSISTOR 2N3646	007-0025-00
Q26	TRANSISTOR 2N4917	007-0027-00
Q27	TRANSISTOR 2N3646	007-0025-00
Q28	TRANSISTOR 2N3646	007-0025-00
Q29	TRANSISTOR 2N4917	007-0027-00
R1	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R2	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R3	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R4	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R5	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R6	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R7	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R8	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R9	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R10	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R11	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R12	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R13	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R14	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R15	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R16	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R17	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R18	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R19	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R20	RESISTOR F/C 330 OHM 1/4W 10%	130-0331-25
R21	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R22	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R23	RESISTOR F/C 470 OHM 1/4W 10%	130-0471-25

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
R24	RESISTOR F/C 470 OHM 1/4W 10%	130-0471-25
R25	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R26	RESISTOR POT 200 OHM 10% 1 TURN	133-0042-03
R27	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R28	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R29	RESISTOR PREC 8.45K 1/8W 1%	125-8451-01
R30	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R31	RESISTOR PREC 10K 1/8W 1%	125-1002-01
R32	RESISTOR PREC 100 OHM 1%	125-1000-01
R33	RESISTOR PREC 100 OHM 1%	125-1000-01
R34	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R35	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R36	RESISTOR PREC 2.05K 1/8W 1%	125-2051-01
R37	RESISTOR PREC 2.05K 1/8W 1%	125-2051-01
R38	RESISTOR PREC 470 OHM 1/8W 1%	125-4700-01
R39	RESISTOR F/C 220K 1/4W 10%	130-0224-25
R40	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R41	RESISTOR PREC 470 OHM 1/8W 1%	125-4700-01
R42	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R43	RESISTOR PREC 2.05K 1/8W 1%	125-2051-01
R44	RESISTOR PREC 2.05K 1/8W 1%	125-2051-01
R45	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R46	RESISTOR F/C 180 OHM 1/4W 10%	130-0181-25
R47	RESISTOR F/C 470 OHM 1/4W 10%	130-0471-25
R48	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R49	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R50	RESISTOR F/C 470 OHM 1/4W 10%	130-0471-25
R51	RESISTOR F/C 68 OHM 1/4W 10%	130-0680-25
R52	RESISTOR F/C 68 OHM 1/4W 10%	130-0680-25
R53	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R54	RESISTOR F/C 33K 1/4W 10%	130-0333-25
R55	RESISTOR PREC 1K 1%	125-1001-01
R56	RESISTOR F/C 150 OHM 1/4W 10%	130-0151-25
R57	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R58	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R59	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R60	RESISTOR PREC 33.2K 1/8W 1%	125-3322-01
R61	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R62	RESISTOR PREC 1K 1%	125-1001-01
R63	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R64	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R65	RESISTOR F/C 10 MEG 1/4W 10%	130-0106-25
R66	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R67	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R68	RESISTOR F/C 150 OHM 1/4W 10%	130-0151-25
R69	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R70	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R71	RESISTOR PREC 33.2K 1/8W 1%	125-3322-01
R72	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R73	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R74	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R75	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R76	RESISTOR F/C 10 MEG 1/4W 10%	130-0106-25
R77	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
R78	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R79	RESISTOR F/C 150 OHM 1/4W 10%	130-0151-25
R80	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R81	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R82	RESISTOR PREC 33.2K 1/8W 1%	125-3322-01
R83	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R84	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R85	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R86	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R87	RESISTOR F/C 10 MEG 1/4W 10%	130-0106-25
R88	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R89	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R90	RESISTOR F/C 100K 1/4W 10%	130-0104-25
R91	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R92	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R93	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R94	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R95	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R96	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R97	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R98	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R99	RESISTOR F/C 180 OHM 1/4W 10%	130-0181-25
R100	RESISTOR F/C 390 OHM 1/4W 10%	130-0391-25
R101	RESISTOR F/C 22 OHM 1/4W 10%	130-0220-25
R102	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R103	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
	MODULATOR BOARD	009-5076-00

ASSEMBLY NO:	200-0190-00
DESCRIPTION:	RF MODULATOR SUB-ASSY (G10)
ASSY DWG NO:	300-5064-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR D/C 6.8 PF NPO 10%	110-0680-05
C2	CAPACITOR CER 47 PF	106-0003-00
C3	CAPACITOR CER 47 PF	106-0003-00
C4	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
C5	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
C6	CAPACITOR MLR .0047 UF 200V 5%	105-0030-02
C7-C10	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
C11-C13	CAPACITOR CER 47 PF	106-0003-00
CR1	DIODE 5082-3529 S/N	007-6030-00
CR2-CR4	DIODE 5082-3041	007-6023-00
FL1	FILTER EMI	017-0002-00
FL2	FILTER EMI	017-0002-00
L1-L5	INDUCTOR 4T #22 BUSS .136	019-2014-00
R1-R3	RESISTOR F/C 22 OHM 1/4W 10%	129-0220-25
R4	RESISTOR F/C 150 OHM 1/4W 10%	130-0151-25
R5-R8	RESISTOR F/C 10 OHM 1/4W 10%	129-0100-25
	GND TERMINAL #2X.531	008-0017-02
	LUG #2	008-0018-00
	PC BD RF SW	009-5064-00
	TERMINAL STANDOFF	010-0007-00
	RECEPTACLE PANEL JACK	030-0012-00
	ENCLOSURE RF SWITCH	047-5026-01
	SCREW PHP 2-56X3/16	089-5054-03
	WASHER INT TOOTH #2	089-8500-00

ASSEMBLY NO:	200-0195-00
DESCRIPTION:	FREQ MONITOR SUB-ASSY (G19)
ASSY DWG NO:	300-5080-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR F/T 470 PF	106-0002-00
C2	CAPACITOR D/C .001 UF Z5V 20%	109-1021-16
C3	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C4	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C5	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C6	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C7	CAPACITOR D/C .001 UF Z5V 20%	109-1021-16
C8	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C9	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C10	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C11	CAPACITOR D/C .001 UF Z5V 20%	109-1021-16
C12-C14	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C15	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C16	CAPACITOR D/C 10 PF NPD 5%	110-1000-04
C17	CAPACITOR D/C 27 PF X5F 10%	109-2700-35
C18	CAPACITOR D/C 220 PF X5F 10%	109-2210-35
C19	CAPACITOR D/C 270 PF X5F 10%	109-2710-35
C20	CAPACITOR D/C 220 PF X5F 10%	109-2210-35
C21	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C22	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C23	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C24	CAPACITOR MLR .01 UF 80V 10%	105-0031-08
C25	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C26	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C27	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C28	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C29	CAPACITOR D/C 33 PF X5F 10%	109-3300-35
C30	CAPACITOR D/C 75 PF X5F 10%	109-7502-35
C31	CAPACITOR D/C 33 PF X5F 10%	109-3300-35
C32	CAPACITOR D/C 47 PF N750 10%	110-4700-35
C33	CAPACITOR D/C 150 PF X5F 10%	109-1510-35
C34	CAPACITOR D/C .001 UF Z5V 20%	109-1021-16
C35	CAPACITOR D/C .001 UF Z5V 20%	109-1021-16
C36	CAPACITOR F/T 470 PF	106-0002-00
C37	CAPACITOR F/T 470 PF	106-0002-00
C38	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
CR1	DIODE 5082-2900	007-6022-00
CR2	DIODE 5082-2900	007-6022-00
CR3	DIODE 1N4148	007-6016-00
I1-I3	VT IC LM733CH	007-7082-01
L1	INDUCTOR 2T #22 BUSS .136	019-2013-00
L2	INDUCTOR MOLD 1 UH 10%	019-2016-10
L3	INDUCTOR RF .22 UH	019-2016-02
L4	INDUCTOR RF .22 UH	019-2016-02
L5	INDUCTOR 18 UH	019-2015-21
L6	INDUCTOR 18 UH	019-2015-21
L7	INDUCTOR RF .22 UH	019-2016-02
L8	INDUCTOR .47 UH	019-2016-06

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
Q1	TRANSISTOR MPS-H81	007-0077-00
Q2	TRANSISTOR 35677	007-0008-00
Q3	TRANSISTOR 35677	007-0008-00
R1	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R2	RESISTOR F/C 390 OHM 1/4W 10%	130-0391-25
R3	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R4	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R5	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R6	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R7	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R8	RESISTOR F/C 180 OHM 1/4W 10%	130-0181-25
R9	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R10	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R11	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R12	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R13	RESISTOR F/C 270 OHM 1/4W 10%	130-0271-25
R14	RESISTOR F/C 1K 1/4W 10%	129-0102-25
R15-R18	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R19	RESISTOR F/C 270 OHM 1/4W 10%	130-0271-25
R20	RESISTOR F/C 1K 1/4W 10%	129-0102-25
R21	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R22	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R23	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R24	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R25	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R26	RESISTOR F/C 180 OHM 1/4W 10%	130-0181-25
R27	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R28	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R29	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R30	RESISTOR F/C 1.2K 1/4W 10%	129-0122-25
R31	RESISTOR F/C 270 OHM 1/4W 10%	130-0271-25
R32	RESISTOR F/C 1K 1/4W 10%	129-0102-25
R33	RESISTOR F/C 1K 1/4W 10%	129-0102-25
R34	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R35	RESISTOR F/C 3.9K 1/4W 10%	130-0392-25
R36	RESISTOR F/C 6.8K 1/4W 10%	130-0682-25
R37	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R38	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R39	RESISTOR F/C 1K 1/4W 10%	129-0102-25
R40	RESISTOR F/C 1K 1/4W 10%	129-0102-25
R41	RESISTOR F/C 390 OHM 1/4W 10%	130-0391-25
R42	RESISTOR F/C 390 OHM 1/4W 10%	130-0391-25
Y1	XTAL 63 MHZ	044-0005-00
Y2	XTAL 60 MHZ	044-0004-00
	GND TERMINAL #2X.468	008-0017-00
	PC BD FREQ MONITOR	009-5080-00
	TERMINAL STANDOFF	010-0007-00
	TERMINAL FEEDTHRU	010-0008-00
	JACK STRAIGHT BULKHEAD	030-0014-00
	ENCLOSURE FREQ MONITOR	047-0213-01
	NUT 2-56	089-2004-21
	CLIP CRYSTAL	090-0106-03
	RIVET BUTTON HEAD	092-0012-22

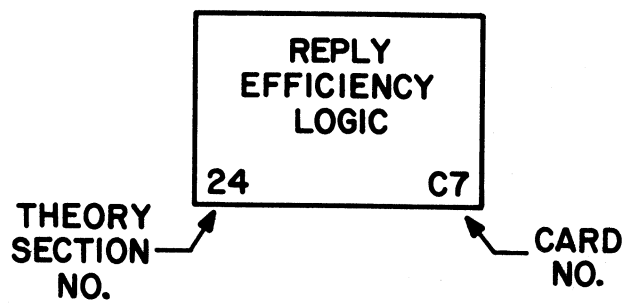
ASSEMBLY NO:	200-5073-00
DESCRIPTION:	DEMODULATOR BD SUB-ASSY (G23)
ASSY DWG NO:	300-5073-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C2	CAPACITOR D/C .01 UF 25V 20%	109-1030-46
C3	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C4	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C5	CAPACITOR TANT 2.2 UF 35V 20%	096-1007-26
C6	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C7	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C8	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C9	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C10-C13	CAPACITOR F/T 470 PF	106-0002-00
CR1	DIODE 1N4148	007-6016-00
CR2	DIODE GERMANIUM 1N270	007-6020-00
CR3	DIODE GERMANIUM 1N270	007-6020-00
DL1	DELAY 2 US	015-0007-00
I1	VT IC N5710T	007-7046-01
I2	VT IC N5710T	007-7046-01
I3	VT IC SN7402	007-7048-01
I4	VT IC N5710T	007-7046-01
I5	VT IC 9601	007-7070-01
I6	VT IC LM306H	007-7044-01
I7	IC N5741V UT	007-7042-01
Q1	TRANSISTOR 2N3646	007-0025-00
Q2	TRANSISTOR 2N3646	007-0025-00
Q3	TRANSISTOR 35677	007-0008-00
R1	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R2	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R3	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R4	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R5	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R6	RESISTOR PREC 470 OHM 1/8W 1%	125-4700-01
R7	RESISTOR F/C 220K 1/4W 10%	130-0224-25
R8	RESISTOR PREC 470 OHM 1/8W 1%	125-4700-01
R9	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R10	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R11	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R12	RESISTOR PREC 1K 1%	125-1001-01
R13	RESISTOR F/C 47K 1/4W 10%	130-0473-25
R14	RESISTOR POT 1K 4 TURN CERM	133-0063-02
R15	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R16	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R17	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R18	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R19	RESISTOR F/C 1K 1/4W 10%	130-0102-25
	PC BD DEMODULATOR	009-5073-00

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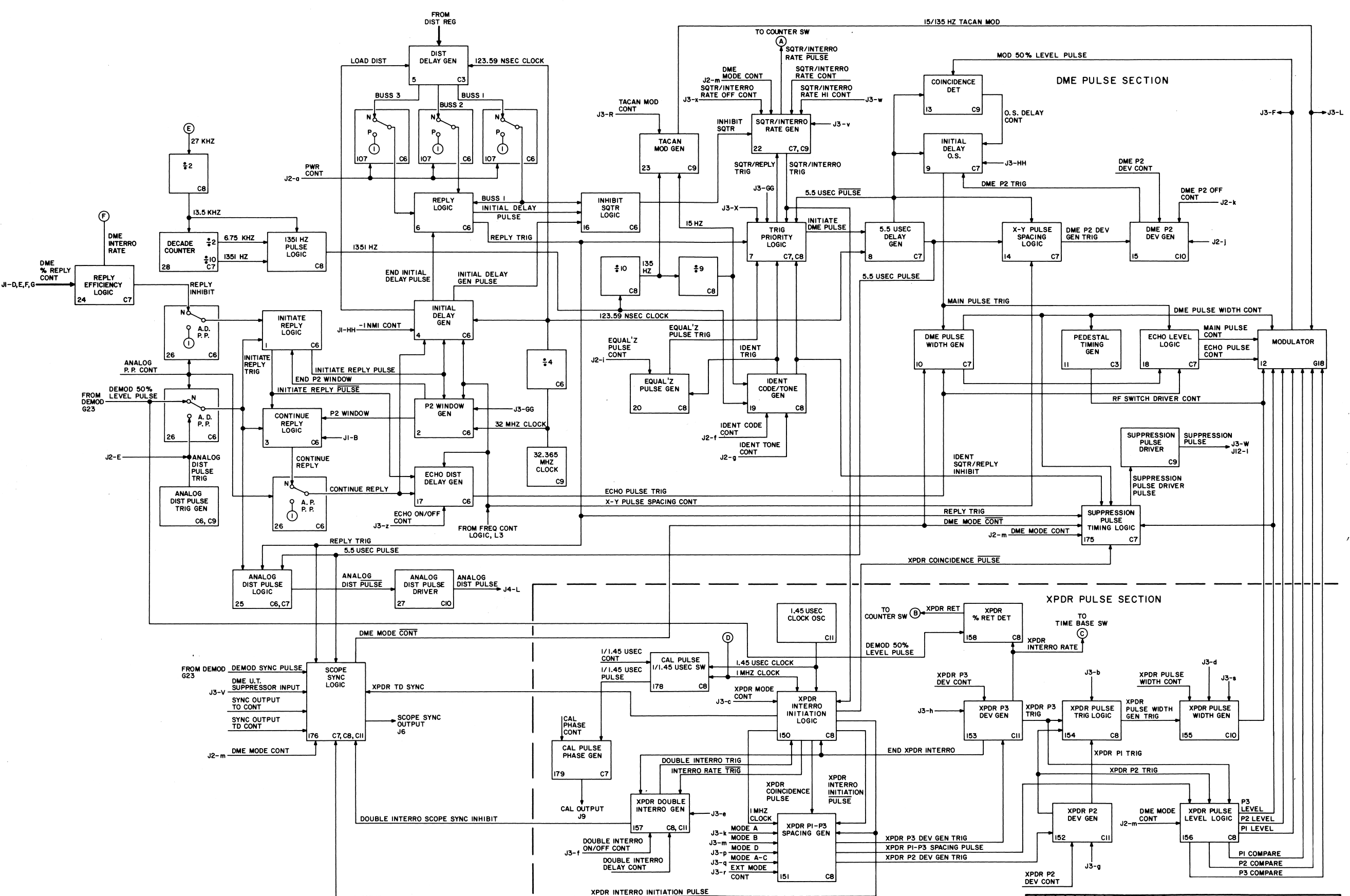


Shown above is a typical example of a section of the VIDEO BLOCK DIAGRAM with a brief description of the NOMENCLATURE in each block.

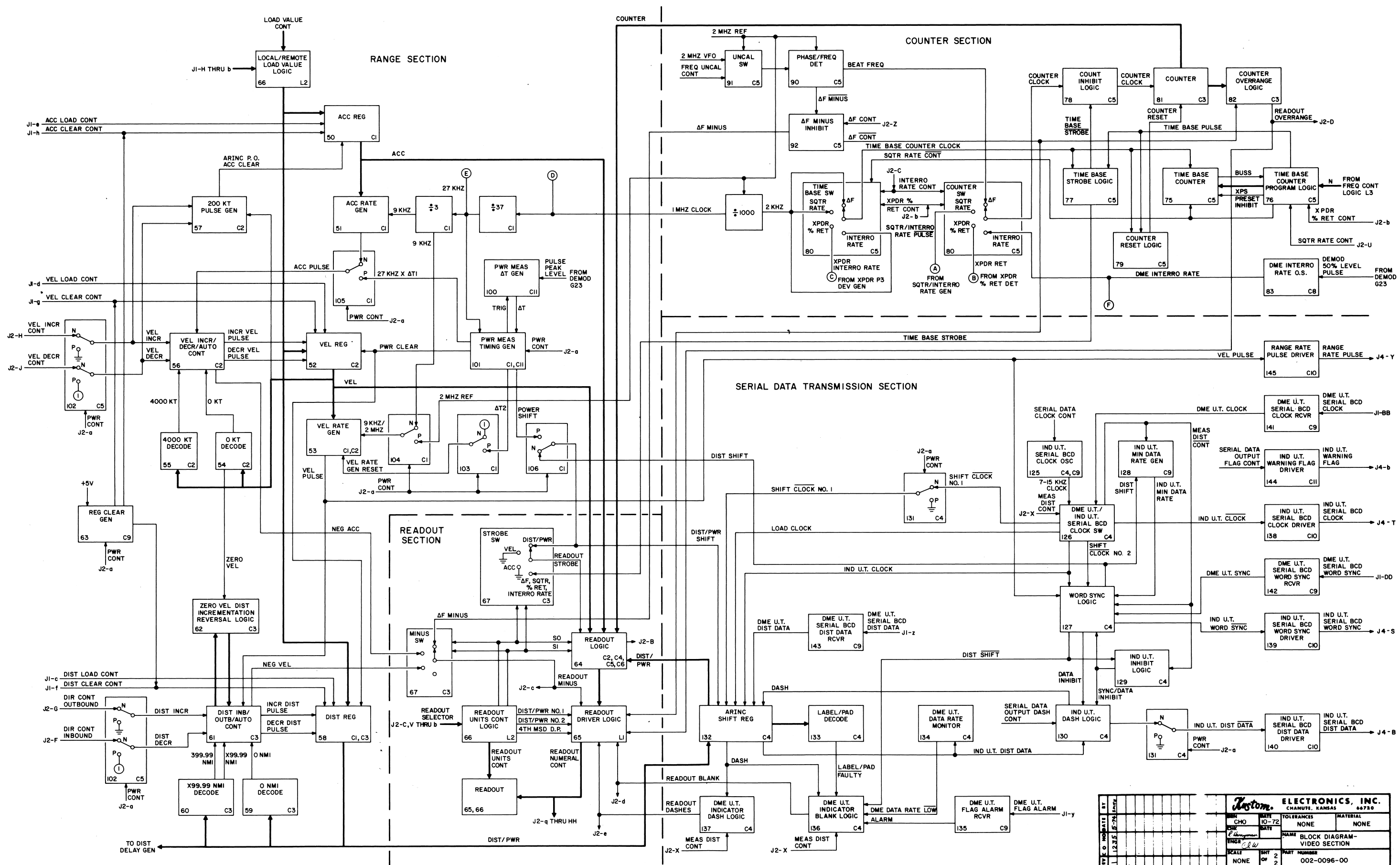
Below is a list of the theory sections which have been omitted for revisions or additions.

THEORY SECTION NUMBERS OMITTED:

21	108 thru 124
28 thru 49	146 thru 149
68 thru 74	159 thru 174
84 thru 89	177
93 thru 99	



BY		DATE	CHK	DATE	SCALE	SHT	OF	PART	NUMBER	ELECTRONICS, INC.		CHAMUTE, KANSAS	66720
1		12-22-72	1	10-72	NONE	1	2	002-0096-00		BLOCK DIAGRAM - VIDEO SECTION			



Revision History			
REV	NO	DATE	DESCRIPTION
1	1	12-22-64	INITIAL
2	2	1-15-65	REVISED

CUSTOMER INFORMATION			
NAME		ADDRESS	
U.S. AIR FORCE		WALLINGFORD, VERMONT	
PROJECT NO.		PROJECT NAME	
10-72		BLOCK DIAGRAM - VIDEO SECTION	
SCALE		PART NUMBER	
NONE		002-0096-00	

ELECTRONICS, INC.			
CHANDLER, KANSAS 66720			
DATE	BY	CHKD	APP'D
10-72	12-22-64	1-15-65	1-15-65
TOLERANCES: NONE			
MATERIAL: NONE			

VIDEO

BLOCK DIAGRAM THEORY

A. DME PULSE SECTION

A reply to a DME U.T. INTERROGATION is initiated by the appearance of a pulse pair on the DEMODULATOR 50% LEVEL PULSE line input to a NORMAL/ANALOG P.P. switch. This pulse pair normally appears on the INITIATE REPLY TRIGGER line and causes the INITIATE REPLY LOGIC to initiate a reply by causing the INITIAL DELAY GENERATOR and the P2 WINDOW GENERATOR to begin operation, providing the REPLY EFFICIENCY LOGIC allows a reply to occur at this time. If the output of the P2 WINDOW GENERATOR, the P2 WINDOW line, occurs when the second pulse of the pulse pair on the INITIATE REPLY TRIGGER line occurs, the CONTINUE REPLY LOGIC output, the CONTINUE REPLY line, allows the INITIAL DELAY GENERATOR to continue operation allowing, on the REPLY TRIGGER line, a pulse which causes a REPLY pulse pair to be generated. If the DISTANCE REGISTER contents are not zero, the DISTANCE DELAY GENERATOR causes the REPLY TRIGGER line signal to be further delayed beyond the delay of the INITIAL DELAY GENERATOR.

TRIGGER PRIORITY LOGIC determines which trigger source shall cause initiation of the next DME pulse. The order of precedence is REMOTE TRIGGER, IDENT TRIGGER, REPLY TRIGGER, and SQUITTER TRIGGER. The TRIGGER PRIORITY LOGIC output, or INITIATE DME PULSE line, causes the 5.5 usec DELAY GENERATOR to begin operation which in turn causes the triggering of the INITIAL DELAY O.S. This causes the MAIN PULSE TRIGGER line to trigger the DME PULSE WIDTH GENERATOR. The output of the DME PULSE WIDTH GENERATOR, the DME PULSE WIDTH CONTROL line, causes the MODULATOR to generate a DME RF pulse.

The MODULATOR 50% LEVEL PULSE line output of the MODULATOR is compared for coincidence with the 5.5 usec PULSE output of the 5.5 usec GENERATOR in the COINCIDENCE DETECTOR. If the MODULATOR 50% LEVEL PULSE precedes the 5.5 usec PULSE the COINCIDENCE DETECTOR output, the O.S. DELAY CONTROL line, causes the INITIAL DELAY O.S. DELAY to increase causing the coincidence of the two signals.

The outputs of the 5.5 usec DELAY GENERATOR, the 5.5 usec PULSE and the 5.5 usec PULSE lines cause the X-Y PULSE SPACING GENERATOR to generate an output on the DME P2 DEVIATION GENERATOR TRIGGER line which triggers the DME P2 DEVIATION GENERATOR. The DME P2 DEVIATION GENERATOR produces a variable delay which is determined by the DME P2 DEVIATION control, after which the output, the DME P2 TRIGGER line, retriggers the INITIAL DELAY O.S. causing a second pulse to be generated.

The PEDESTAL TIMING GENERATOR, which is triggered by the DME PULSE WIDTH CONTROL line, generates an output on the RF SWITCH DRIVER CONTROL line and causes the MODULATOR to generate the required RF on/off ratio.

The ECHO DISTANCE DELAY GENERATOR produces an output on the ECHO PULSE TRIGGER line which triggers the DME PULSE WIDTH GENERATOR and the ECHO LOGIC, thus causing the MODULATOR to generate an RF ECHO pulse.

The SQUITTER/INTERROGATION RATE GENERATOR produces a pulse output with a PRF which is controlled by the SQUITTER/INTERROGATION RATE control. The pulse spacing in the DME mode is very random while in the TRANSPONDER mode it is very regular.

The INHIBIT SQUITTER LOGIC output, the INHIBIT SQUITTER line, prevents SQUITTER pulses from appearing for at least 50 usec prior to a REPLY.

The IDENTIFICATION TONE/CODE GENERATOR generates a 1350 Hz tone or a code of KID with a 5 sec interval. The EQUALIZATION PULSE GENERATOR causes a second pulse pair to appear 100 usec after the identification pulse pair.

The SUPPRESSION PULSE TIMING LOGIC operates off the REPLY TRIGGER line and the DME PULSE WIDTH CONTROL line to cause the SUPPRESSION PULSE DRIVER output to be coincident with the REPLY RF pulses. In the TRANSPONDER MODE of operation the TRANSPONDER COINCIDENCE PULSE line and the P3 LEVEL inputs cause the SUPPRESSION PULSE to be coincident with the TRANSPONDER INTERROGATION RF pulses.

The TACAN MODULATION GENERATOR filters the pulses on the 15 Hz and 135 Hz input lines, combines them and causes this signal to appear on the 15/135 Hz TACAN MOD line when the TACAN MODULATION is called for.

The SCOPE SYNC LOGIC selects one of the various inputs to cause a pulse on the SCOPE SYNC OUTPUT line. This selection is controlled by the SYNC OUTPUT To control and the SYNC OUTPUT Td control inputs.

B. RANGE SECTION

The contents of the DISTANCE REGISTER is determined either by the LOAD VALUE control or the VELOCITY PULSE incrementation. The DISTANCE REGISTER is incremented to either greater or lesser values by the VELOCITY pulse in accordance with the DISTANCE INBOUND/OUTBOUND/AUTO control. In the AUTO mode, each time the DISTANCE REGISTER content becomes 0 NMI or X99.99 NMI the direction of incrementation is reversed.

The VELOCITY PULSE PRF is determined by the contents of the VELOCITY REGISTER.

The contents of the VELOCITY REGISTER is determined by either the LOAD VALUE CONTROL or the ACCELERATION PULSE incrementation. The VELOCITY REGISTER is incremented to either greater or lesser values by the ACCELERATION pulse in accordance with the VELOCITY INCREASE/DECREASE/ARINC P.O. control. In the ARINC P.O. mode the direction of incrementation is reversed each time the VELOCITY REGISTER content becomes zero and when the VELOCITY REGISTER 200 kt line goes to a "1" the ACCELERATION REGISTER contents are cleared to zero.

The contents of the ACCELERATION REGISTER is determined by the LOAD VALUE control which in turn determines the ACCELERATION PULSE PRF. The contents of the ACCELERATION REGISTER are cleared to zero in the VELOCITY ARINC P.O. mode when the VELOCITY REGISTER 200 kt line goes to a "1".

In the POWER MEASUREMENT mode the POWER MEASUREMENT ΔT GENERATOR generates a pulse of a time interval which varies directly with the voltage on the PULSE PEAK LEVEL line. The POWER MEASUREMENT TIMING GENERATOR utilizes the ΔT input to generate the 27 KHz $\times \Delta T_1$ output which increments the VELOCITY REGISTER. The ΔT input is also utilized to generate the ΔT_2 interval which causes the DISTANCE REGISTER to be incremented. Following ΔT_2 the POWER SHIFT line causes the contents of the DISTANCE REGISTER to be strobed into the READOUT LOGIC after which the contents of the VELOCITY REGISTER and the DISTANCE REGISTER are cleared to zero by the POWER CLEAR line. Thus a digital squaring operation is performed to compute the PEAK POWER from the PULSE PEAK LEVEL since the VELOCITY RATE GENERATOR output PRF and the interval in which the DISTANCE REGISTER is clocked are both proportional to the interval ΔT .

C. TRANSPONDER PULSE SECTION

A test set TRANSPONDER INTERROGATION is initiated by a pulse on the SQUITTER/INTERROGATION TRIGGER line input to the TRANSPONDER INTERROGATION INITIATION LOGIC. As soon as there has been coincidence between 1.45 usec CLOCK and the 1 MHz CLOCK, the TRANSPONDER INTERROGATION INITIATION PULSE and the TRANSPONDER INTERROGATION INITIATION PULSE lines change state causing the TRANSPONDER P1-P3 GENERATOR to begin operation and generate pulses of the proper duration on the TRANSPONDER P2 and TRANSPONDER P3 DEVIATION GENERATOR TRIGGER lines. The duration of the pulse on the TRANSPONDER P3 DEVIATION line is determined by the state of the MODE A, B, C, D and A-C input lines. The triggering of the TRANSPONDER P2 and TRANSPONDER P3 DEVIATION GENERATORS cause pulses on the TRANSPONDER P1 TRIGGER, the TRANSPONDER P2 TRIGGER and the TRANSPONDER P3 TRIGGER lines which are combined in the TRANSPONDER PULSE TRIGGER LOGIC and result in an output on the TRANSPONDER PULSE WIDTH TRIGGER line which triggers the TRANSPONDER PULSE WIDTH GENERATOR. The duration of the pulse on the

RF SWITCH DRIVER CONTROL output line of the TRANSPONDER PULSE WIDTH GENERATOR is determined by the TRANSPONDER PULSE WIDTH CONTROL and determines the duration of the TRANSPONDER INTERROGATION RF PULSES. The delay between trigger inputs to the TRANSPONDER P2 and P3 DEVIATION GENERATOR and the pulse on the outputs is determined by the TRANSPONDER P2 and P3 DEVIATION CONTROL and the TRANSPONDER P1-P2 and P1-P3 pulse spacing. The TRANSPONDER PULSE LEVEL LOGIC which is triggered by the TRANSPONDER P1-P3 SPACING PULSE, and the TRANSPONDER P2 and TRANSPONDER P3 TRIGGER inputs, causes the P1, P2 and P3 LEVEL and the P1, P2 and P3 COMPARE output lines to change state in such a manner as to cause the MODULATOR to cause the TRANSPONDER INTERROGATION RF PULSES to be the proper amplitude.

The TRANSPONDER DOUBLE INTERROGATION GENERATOR, which is triggered by the END TRANSPONDER INTERROGATION line, generates a delay determined by the DOUBLE INTERROGATION control after which the TRANSPONDER INTERROGATION INITIATION LOGIC is retriggered and a second TRANSPONDER INTERROGATION is generated.

The CALIBRATION PULSE 1/1.45 USEC SWITCH selects either the 1 MHz CLOCK or the 1.45 usec CLOCK to appear at the CALIBRATION OUTPUT. The CALIBRATION PULSE PHASE GENERATOR causes the phase of the CALIBRATION OUTPUT pulses to vary as determined by the CALIBRATE PHASE control.

D. SERIAL DATA TRANSMISSION SECTION

The SERIAL DATA TRANSMISSION SECTION operates in three modes.

1. INDICATOR U.T. MODE (TEST DISTANCE)

The test distance is loaded into the ARINC SHIFT REGISTER and shifted out to an INDICATOR U.T.

2. DME U.T. MODE (MEASURED DISTANCE)

The data from a DME U.T. is shifted into the ARINC SHIFT REGISTER and caused to appear at READOUT.

3. POWER MODE

The contents of the DISTANCE REGISTER, which is the computed peak power of the DME OR TRANSPONDER U.T., is loaded into the ARINC SHIFT REGISTER and caused to appear at the READOUT.

INDICATOR U.T. MODE

The 14-30 KHz CLOCK output of the INDICATOR U.T. SERIAL BCD CLOCK OSCILLATOR is selected as the source of the clock for the WORD SYNCHRONIZATION LOGIC and the ARINC SHIFT REGISTER. When the WORD SYNCHRONIZATION LOGIC is triggered by either a VELOCITY pulse or INDICATOR U.T.

MINIMUM DATA RATE pulse, the INDICATOR U.T. WORD SYNC output line causes the INDICATOR U.T. SERIAL BCD WORD SYNC DRIVER to generate on the SERIAL BCD WORD SYNC line the proper waveform and the ARINC SHIFT REGISTER to shift out on the INDICATOR U.T. DISTANCE DATA line a distance determined by the contents of the DISTANCE REGISTER. The INDICATOR U.T. SERIAL BCD DISTANCE DATA DRIVER causes the proper levels to be generated on the SERIAL BCD DISTANCE DATA line.

DME U.T. MODE

The DME U.T. CLOCK is selected by the DME U.T./INDICATOR U.T. SERIAL BCD CLOCK SWITCH as the source of the clock for the WORD SYNCHRONIZATION LOGIC and the ARINC SHIFT REGISTER. When triggered by the DME U.T. SYNC input, the WORD SYNCHRONIZATION LOGIC causes the ARINC SHIFT REGISTER to shift in the data on the DME U.T. DISTANCE DATA line and cause this distance to appear at the READOUT.

If DASHES are to be displayed, the READOUT is BLANKED and DASHES caused to appear. If the DME U.T. FLAG ALARM line is low the READOUT is caused to BLANK.

POWER MODE

Each time there is a pulse on the POWER SHIFT line, the ARINC SHIFT REGISTER is caused to load the contents of the DISTANCE REGISTER which is the computed PEAK POWER output of the DME or TRANSPONDER U.T. This value is caused to appear at the readout.

E. COUNTER SECTION

The time base period for the COUNTER is determined by the TIME BASE COUNTER and the TIME BASE COUNTER PROGRAM LOGIC. The COUNT interval is caused to vary according to the state of the % RETURN CONTROL, the SQUITTER RATE CONTROL, the N input from the FREQUENCY CONTROL LOGIC, and the DME INTERROGATION RATE CONTROL inputs. The PHASE/FREQUENCY DETECTOR generates a beat frequency which is the difference between the 2 MHz REFERENCE and the 2 MHz VFO and is used to derive the ΔF READOUT.

F. READOUT SECTION

The READOUT LOGIC selects the data which is to appear at the READOUT via the READOUT DRIVER LOGIC. The selection is made by the S0 and S1 inputs which are controlled by the READOUT SELECTOR. The UNITS which appear at the READOUT are also controlled by the READOUT SELECTOR. The MINUS SWITCH selects the proper input to the READOUT MINUS line.

THEORY OF OPERATION

1. INITIATE REPLY LOGIC (C6)

PURPOSE:

To initiate the test set reply to the DME U.T. INTERROGATION and to vary the reply efficiency as determined by the output of the REPLY EFFICIENCY LOGIC (C7).

OPERATION:

When the DME U.T. interrogates the test set the interro pulses appear on the INITIATE REPLY TRIGGER line via the DEMODULATOR 50% LEVEL PULSE line or the ANALOG DISTANCE PULSE TRIGGER line. This triggering of I1 causes pulses to appear on the INITIATE REPLY PULSE and INITIATE REPLY PULSE lines providing the REPLY INHIBIT line is at a "1". Pin 12 of I1, is set by the negative pulse on the END P2 WINDOW line.*

2. P2 WINDOW GENERATOR (C6)

PURPOSE:

To generate a positive pulse window on the P2 WINDOW line to use as a GO-NO GO test for the DME U.T. P1-P2 pulse spacing. If the P1-P2 spacing is not within ± 0.5 usec of nominal, the test set will not reply.

OPERATION:

When the INITIATE REPLY PULSE line goes to a "0" I11, I12, I13 and I14 are released so they may be clocked. Pins 1,2,4,5 and 6 of AND gate I5 decode the 990 state of I12, I13 and I14 thus causing the P2 WINDOW line to go to a "1" approximately 11.5 usec after the counter release in X mode and 35.5 usec in Y mode. Pins 1,2,14 and 15 of NAND gate I19 decode the 998 state of I12, I13 and I14 thus causing the P2 WINDOW line to go to a "0" approximately 1 usec after it went to a "1".*

3. CONTINUE REPLY LOGIC (C6)

PURPOSE:

To allow the test set to generate a reply if the DME U.T. P1-P2 pulse spacing is within ± 0.5 usec of nominal, by causing the CONTINUE REPLY line to be at a "1".

OPERATION:

When the P1 pulse of the DME U.T. interro appears on the INITIATE REPLY TRIG line the P2 WINDOW line is at a "0" thus causing the Q output of I1, pin 5 to be a "0" immediately following the P1 trigger. If the P2 WINDOW line is at a "1" when the P2 pulse appears on the INITIATE REPLY TRIGGER line, the Q output of I1, pin 5 is triggered to a "1". This causes the Q output of I2, pin 5 to be triggered to a "1" by the INITIATE REPLY PULSE line at the end of the P2 window. Thus a "1" is present on the CONTINUE REPLY line if the pulse spacing is within specifications.*

* See timing diagram shown in figure 1.

4. INITIAL DELAY GENERATOR (C6)

PURPOSE:

To generate the required initial delays which, when added to the delay of the 5.5 usec DELAY GENERATOR (C7), give the required Zero NMi delay. In the X mode the delay generated is 44.48 usec or 360 counts of the 123.59 nsec CLOCK. In the Y mode the delay is 50.55 usec or 409 counts.

OPERATION:

The INITIATE REPLY PULSE line indirectly causes the INITIAL DELAY GENERATOR PULSE line to go to a "1" which causes the release of I15, I16, I17 and the appearance of the 123.59 nsec CLOCK at the clock input of I15. When AND gate I6, pins I0, I1, I2, I4 and I5, decodes the 909 state of I15, I16 and I17, a "1" appears on the END INITIAL DELAY PULSE line which causes the INITIAL DELAY GENERATOR PULSE line to go to a "0" which causes I15, I16 and I17 to be preset and the 123.59 nsec CLOCK to be removed from the clock input to I15.*

5. DISTANCE DELAY GENERATOR (C3)

PURPOSE:

To generate the required distance delay to simulate the distance programmed into the test set.

OPERATION:

During the initial delay period the "0" on the LOAD DISTANCE line causes the DISTANCE DELAY GENERATOR to be preset to a value which is determined by the contents of the DISTANCE REGISTER and appearing at the inputs of I21, I22, I23, I24 and I25, PINS 5, I1, I4 and 2. At the end of the initial delay period the LOAD DISTANCE line goes to a "1" thus allowing the generator to be clocked down to the "0" state by the 123.59 nsec CLOCK. As the DISTANCE DELAY GENERATOR is clocked down to "0", BUSS 1, BUSS 2 and BUSS 3 take on "1" values.*

6. REPLY LOGIC (C6)

PURPOSE:

To generate a negative pulse on the REPLY TRIGGER line at the end of the distance delay period.

OPERATION:

When the END INITIAL DELAY PULSE appears, the INITIAL DELAY PULSE line is triggered to a "1" by the next 123.59 nsec CLOCK pulse.

When the DISTANCE DELAY GENERATOR is clocked into the "zero" state BUSS 3 goes to a "1". Since both the INITIAL DELAY PULSE line and BUSS 1 are at a "1", the REPLY TRIGGER line goes to a "0" for one period of the 123.59 usec CLOCK.*

* See timing diagram shown in figure 1.

7. TRIGGER PRIORITY LOGIC (C7) (C8)

PURPOSE:

To allow the test set to have the following order of signal priorities; Remote trigger inputs over Ident, over Reply, over Squitter.

OPERATION:

REMOTE PRIORITY

When the REMOTE DME INBOX SIGNAL INHIBIT line is at a "0" the INHIBIT SQUITTER/REPLY line is at a "0". This prevents the INITIATE DME PULSE line from being triggered to a "1" by the SQUITTER/REPLY TRIGGER line.

If the REMOTE DME PULSE PAIR TRIGGER line goes to a "0", the REMOTE/IDENT TRIGGER line goes a "0" thus causing the INITIATE DME PULSE line to be set to a "1".

IDENT PRIORITY

If the IDENT SQUITTER/REPLY INHIBIT line is a "0", the INHIBIT SQUITTER/REPLY line is a "0" and the INITIATE DME PULSE line is prevented from being triggered to a "1" by the SQUITTER/REPLY TRIGGER line. Falling edges on the IDENT TRIGGER line cause negative pulses on the REMOTE/IDENT TRIGGER line causing the INITIATE DME PULSE line to be set to a "1".

REPLY PRIORITY

Prior to the appearance of the negative pulse on the REPLY TRIGGER line the INHIBIT SQUITTER line input to the SQUITTER/INTERRO RATE GENERATOR is a "0" thus preventing the INITIATE DME PULSE line from being triggered to a "1" by a pulse originating from the SQUITTER/INTERRO RATE GENERATOR.

8. 5.5 USEC. DELAY GENERATOR (C7)

PURPOSE:

To generate a 5.56 usec delay which is used to reference the output of the MODULATOR 50% LEVEL pulse against. This allows the reply pulse to be stabilized against a crystal controlled delay.

OPERATION:

When the INITIATE DME PULSE line goes to a "1" the 5.5 usec PULSE line is triggered to a "1" by the next 123.59 nsec CLOCK pulse. This allows counters I15 and I16 to be clocked by the 123.59 nsec CLOCK. AND gate I13, pins 10, 11, 12, 14 and 15, decodes the 99 state of the counter which causes the 5.5 usec PULSE line to be triggered to a "0".*

9. INITIAL DELAY O.S. (C7)

PURPOSE:

To generate a delay interval, which is controlled by the output of a COINCIDENCE DETECTOR that causes the falling edge of the MODULATOR 50% LEVEL PULSE to be coincident with the rising edge of the 5.5 usec PULSE.

* See timing diagram shown in figure 2

9. INITIAL DELAY O.S. (C7) (Cont'd)
OPERATION:
The O.S. pulse width is controlled by the state of the O.S. DELAY INTERVAL line. The state of this line controls the voltage on C6 and hence the pulse width of the O.S., I27, pin 6.*
10. DME PULSE WIDTH GENERATOR (C7)
PURPOSE:
To control the DME RF pulse width which should be 3.5 usec nominal.

OPERATION:
The pulse on the MAIN PULSE TRIGGER line causes the DME PULSE WIDTH CONTROL line to be triggered to a "0" for 3.5 usec.*
11. PEDESTAL TIMING GENERATOR (C3)
PURPOSE:
To generate a 7 usec pulse on the RF SWITCH DRIVER CONTROL line which causes a RF pedestal to be formed by the RF SWITCH section of the RF MODULATOR to cause the necessary RF on/off ratio to be generated.

OPERATION:
The negative pulse on the DME PULSE WIDTH CONTROL line causes the Q output of O.S., I20, pin 6, to be triggered to a "1" for 0.5 usec which then causes a 7 usec pulse to appear on the RF SWITCH DRIVER CONTROL line.
12. MODULATOR (G18)
PURPOSE:
To cause RF pulses to be formed and to detect the 50% level point of the leading edge of the P1 pulse.

OPERATION:
The DME PULSE WIDTH CONTROL line pulse causes the RF pulse to be formed. The detected envelope of the RF pulse is fed into the 50% LEVEL DETECTOR which generates a negative going pulse 2.0 usec delayed from the 0.5 amplitude point of the leading edge of the detected RF pulse.
13. COINCIDENCE DETECTOR (C7)
PURPOSE:
To cause the O.S. DELAY INTERVAL line to be at the proper state to cause coincidence of the 5.5 usec pulse and the MODULATOR 50% LEVEL PULSE.

* See timing diagram shown in figure 2.

13. COINCIDENCE DETECTOR (C7) (Cont'd)

OPERATION:

If the MODULATOR 50% LEVEL PULSE is lagging the 5.5 usec PULSE the O.S. DELAY INTERVAL line is triggered to a "1" which causes the INITIAL DELAY O.S. pulse width to be reduced.

14. X-Y PULSE SPACING LOGIC (C7)

PURPOSE:

To add the 18 usec delay necessary to cause the P1-P2 spacing to be correct in the Y mode.

OPERATION:

In the X mode the 5.5 usec PULSE appears inverted on the DME P2 DEVIATION GENERATOR TRIGGER line.

In the Y mode the \bar{Q} output of I25, pin 7 appears inverted on the DME P2 DEVIATION GENERATOR TRIGGER line. The \bar{Q} output is triggered to a "0" for 18 usec.

In each case the DME P2 DEVIATION GENERATOR is triggered by the falling edge on the DME P2 DEVIATION GENERATOR line.

15. DME P2 DEVIATION GENERATOR (C10)

PURPOSE:

To allow the P1-P2 spacing to be varied over a range of ± 6 usec of nominal.

OPERATION:

The falling edge of the pulse on the DME P2 DEVIATION GENERATOR TRIGGER line causes the \bar{Q} output of I3B, pin 8 to be triggered to a "0" which causes Q5 to cease conducting and C9 to charge due to current flow thru R43. When the voltage on I9, pin 3 exceeds that on I9, pin 2 the output of the comparator, I9, pin 7, goes to a "0" which causes the \bar{Q} output of I3B, pin 8 to be reset to a "1". Thus a positive pulse is formed on the DME P2 TRIGGER line. The width of the pulse depends on the voltage on pin 2 of I9, which is controlled by the DME P2 DEVIATION control.

16. INHIBIT SQUITTER LOGIC (C6)

PURPOSE:

To cause the squitter output to be inhibited, a minimum of approximately 45 usec prior to a reply output.

OPERATION:

When Buss 1 and Buss 2 are at a "1" and either the INITIAL DELAY GENERATOR PULSE line or the INITIAL DELAY PULSE is at a "1" the INHIBIT SQUITTER line is a "0".

16. INHIBIT SQUITTER LOGIC (C6) (Cont'd)

The INHIBIT SQUITTER line is at a "0" a minimum of approximately 45 usec in the X mode or 50 usec in Y mode but may be as much as 100 usec when the DISTANCE DELAY GENERATOR is programmed for 3.99 Nmi.*

17. ECHO GENERATOR (C6)

PURPOSE:

To cause an echo to occur at approximately 30 Nmi.

OPERATION:

Providing the ECHO INJECTION SWITCH is in the ON position, the INITIATE REPLY PULSE causes pulses on the ECHO TRIGGER line due to the triggering of either I22 or I25 and I27. I25 is triggered in the X mode and I22 in the Y mode.

18. ECHO LEVEL LOGIC (C7)

PURPOSE:

To cause the MODULATOR to form RF pulses of either the main level or the echo level.

OPERATION:

A pulse on the ECHO PULSE TRIGGER line, triggers the Q output of I20, pin 6 to a "1" providing the MAIN PULSE TRIGGER has not triggered the Q output of I20, pin 9 to a "0".

19. IDENT CODE/TONE GENERATOR (C8)

PURPOSE:

To generate the Ident Code, KID

OPERATION:

The Ident Code is generated at the QA output of I10, pin 5, in the following manner provided the IDENT CODE line is at a "0" which allows the counter to be clocked at the C1 input I10, pin 10.

As I10 is clocked, its QA output, pin 5, goes from a "0" to "1" to "0" with each clock. When the QA output is at a "1" the 1351 Hz pulse appears at AND gate I17, pin 10 and AND gate I18, pin 12, located in the TRIGGER PRIORITY LOGIC. When the QA output is "0" the 1351 Hz pulse is inhibited.

The QA, QB, QC and QD outputs of I10, which is a $\div 16$ counter, are connected to the A,B,C, D inputs of I19 and I20 which are BCD to One of Ten Decoders. Observation of the schematic shows that when I10 is in either 1,5,6,10 or 11 state, the output of NAND gate I25, pin 6 is a "1". This "1" causes the C1 input to I10, pin 10 to change from a 7.5 Hz. pulse to 2.5 Hz pulse. Thus when the "1" is present either a dash or a space between code letters is generated.

* See timing diagram shown in figure 1.

19. IDENT CODE/TONE GENERATOR (C8) (Cont'd)
The Ident. Code is KID

K - . -
I . .
D - . .

Thus the code is generated as follows:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
-	.	.	.	-	-

When the 15 decode, I19 pin 9, goes to a "1" on the sixteen count, the O.S., I24 pin 12 is triggered. The "0" on I24, pin 9 acting on the R input of I10, pin 15, resets I10 and inhibits it from being clocked until the "0" is removed.

In order to generate the ident tone, it is necessary for the IDENT CODE line to be at a "1" and the IDENT TONE line to be at a "0". The "0" then present at the DS input of I10, pin 1 causes the "1" present at I10, pin 4 to appear at the QA output of I10, pin 5. This "1" allows the 1351 Hz pulse to trigger the TRIGGER PRIORITY LOGIC.

If the REMOTE DME INBOX SIGNAL INHIBIT line were at a "0", both the ident code and the ident tone are blocked from appearing at the output of AND gate I17, pin 10.

20. EQUALIZATION PULSE GENERATOR (C8)

PURPOSE:

To allow the PRF of the RF pulse pair to be changed from 1350 to 2700 during the IDENT CODE/TONE interval.

OPERATION:

If the EQUALIZING PULSE CONTROL line is at a "0" then each time the DME PRIORITY LOGIC is triggered by the IDENT TRIGGER line, O.S. I29, pin 6 is also triggered to a "1". The return of the Q output, I29, pin 6 to "0" 100 usec. later, causes the TRIGGER PRIORITY LOGIC to be triggered.

22. SQUITTER/INTERROGATION RATE GENERATOR (C7, C9)

PURPOSE:

To generate the required PRF of the DME squitter and XPDR interrogation pulses. Also to prevent the squitter pulse spacing from being less than 60 usec.

22. SQUITTER/INTERROGATION RATE GENERATOR (C7, C9) (Cont'd)
OPERATION:

The noise generated by CR3, after being amplified by Q12, appears at the minus input of I5, pin 3. Each time the noise voltage is less than the voltage on the plus input of I5, pin 2, a positive pulse is generated on the GENERATOR OUTPUT line. This positive pulse causes a negative pulse on the SQUITTER/INTERRO TRIGGER line and a positive pulse on the SQUITTER/REPLY TRIGGER line. This positive pulse causes the INITIATE DME PULSE line to be triggered to a "1" and the \bar{Q} outputs of O.S. I23, pins 7 and 9 to be triggered to a "0". This causes the SQUITTER/INTERRO RATE PULSE line to go to a "0" thus blocking any pulse on the GENERATOR OUTPUT line for the duration of the O.S. pulse width. The positive pulse appearing on the SQUITTER/INTERRO RATE PULSE line is integrated by C9 I4 and associated circuitry thus generating a voltage on C11 which is proportional to the squitter rate. As the SQUITTER/INTERROGATION RATE control is varied, the voltage on the plus input to I4, pin 2 is varied. Thus the bias voltage for the plus input to I5, pin 2 is generated.

In the XPDR mode of operation the noise voltage input to I5, pin 3 is removed. Each time there is a pulse on the SQUITTER/INTERRO RATE PULSE line, Q10 is caused to saturate and discharge the voltage across C9. Again the voltage on the plus input to I4, pin 2 and the integrated pulse on the SQUITTER/INTERRO RATE PULSE line determines the voltage on C11 and hence the PRF.

23. TACAN MODULATION GENERATOR (C9)

PURPOSE:

To generate a composite 15 Hz and 135 Hz signal to be applied to the MODULATOR (G18) to cause the DME RF pulses to be amplitude modulated in a manner to simulate TACAN modulation.

OPERATION:

The 15 Hz pulse is filtered by I7, an active bandpass filter, to produce a 15 Hz sine wave. The 135 Hz pulse is filtered by I8, also an active bandpass filter, which produces a 135 Hz sine wave. The 15 Hz and 135 Hz signals are combined and amplified by I9 and appear on the 15/135 Hz TACAN MODULATION line provided the TACAN MODULATION CONTROL line is at a "0".

24. REPLY EFFICIENCY LOGIC (C7)

PURPOSE:

To generate a signal, which, applied to the INITIATE REPLY LOGIC (C6), causes the test set to not reply so as to vary the percent return.

24. REPLY EFFICIENCY LOGIC (C7) (Cont'd)

OPERATION:

The REPLY EFFICIENCY LOGIC is digitally controlled by a BCD code in 10% steps.

I3 is a decade rate multiplier. That is, the output, Pin 6, enables DME returns for N-of-Ten interrogations of the DME under test, where "N" corresponds to the setting of S23, DME % reply switch. Negative true logic is used at S23, and I1A, D, E, F make it positive true. I3's internal logic works for S23 settings from 0 through 90%, while I2C contributes the 100% logic. I2A, B, D cause I3 to be clocked at the end of the DME Interro Rate pulse.

25. ANALOG DISTANCE PULSE LOGIC (C6, C7)

PURPOSE:

To generate the necessary input to the ANALOG DISTANCE PULSE DRIVER to cause the analog distance pulses to appear at the proper time.

OPERATION:

A pulse on the INITIATE REPLY TRIGGER line causes the sequence of events shown in the timing diagram shown on figure 3.

26. ANALOG DISTANCE SWITCH (C6)

PURPOSE:

To allow the test set to generate analog distance pulses without the necessity of having DME U.T. to interrogate it.

OPERATION:

If the ANALOG P.P. line is at a "0" the Quad Multiplexer, I21, causes the following changes.

- A. A pulse from the ANALOG DISTANCE PULSE TRIGGER GENERATOR is substituted for a pulse from the DEMODULATOR 50% LEVEL PULSE line.
- B. A "1" is substituted for the output of the REPLY EFFICIENCY LOGIC.
- C. A "1" is substituted for the output of the CONTINUE REPLY LOGIC.

27. ANALOG DISTANCE PULSE DRIVER (C10)

PURPOSE:

To generate a pulse on the ANALOG DISTANCE PULSE line which has the proper levels and rise/fall time.

OPERATION:

The negative pulse on the ANALOG DISTANCE PULSE line causes a level change on the ANALOG DISTANCE PULSE line. The rate of change is determined by the INTEGRATOR consisting of I7, C7, R67 and R31. The Hi level is determined by the ANALOG DISTANCE PULSE HI LEVEL pot, R32. The Lo level is determined by the ANALOG DISTANCE PULSE LO LEVEL pot, R36. Q4 serves as a buffer.

28. DECADE DIVIDER

PURPOSE:

To divide 13.5 KHz signal by ten.

OPERATION:

I4 is a 7490 BCD decade counter, counting in the classic BCD sequence. Outputs are taken from both the "A" (divide by two) and "D" (divide by ten) outputs.

50. ACCELERATION REGISTER (C1)

PURPOSE:

To store the acceleration rate the test set has been programmed for.

OPERATION:

When the ACCELERATION LOAD CONTROL line is at a "0" the outputs of I6, I7 and I8 correspond to the input values. The inputs are determined by the REGISTER LOAD VALUE Control.

Should the ACCELERATION CLEAR CONTROL line or the ARINC P.O. ACCELERATION CLEAR line be at a "0" the contents of the ACCELERATION REGISTER are cleared to zero.

The outputs of the ACCELERATION REGISTER connect to the ACCELERATION RATE GENERATOR and to the READOUT LOGIC.

51. ACCELERATION RATE GENERATOR (C1)

PURPOSE:

To generate a string of pulses with a PRF which varies in accordance with the contents of the ACCELERATION REGISTER. The pulses cause the VELOCITY REGISTER contents to be incremented.

OPERATION:

If the ACCELERATION REGISTER were programmed for 200, there would be a "1" present at the input of NAND gate I24, pin 3. Since the \bar{Q} output of I27, pin 10, is a "1" every other trigger pulse on the ACCELERATION RATE GENERATOR TRIGGER line, the output of I24, pin 6, would be "0" every other trigger pulse or 200 times for every 400 trigger pulses. The presence of the trigger pulse at the input of I24, pin 4, is to cause the negative pulse at I24, pin 6, to be a very narrow one. This pulse in turn would produce a positive pulse at the output of NAND gate I26, pin 6, 200 times for 400 trigger pulses.

If the ACCELERATION REGISTER contained 100, then by the same reasoning the output of NAND gate, I26, pin 10, would have a negative pulse present 100 times for 400 trigger pulses. Again this pulse would produce a positive pulse at the output of NAND gate I26, pin 6, 100 times for every 400 trigger pulses.

If the ACCELERATION REGISTER were to contain 300, the 100 pulses for every 400 trigger pulses and the 200 pulses for every 400 trigger pulses add to produce 300 pulses for every 400 pulses.

The rest of the ACCELERATION RATE GENERATOR operates in a similar manner.

51. ACCELERATION RATE GENERATOR (C1) (Cont'd)

If the ACCELERATION REGISTER contained 001, the output of NAND gate I13, pin 6, would have a negative pulse present once for every 400 trigger pulses.

If the ACCELERATION REGISTER contained 010, the output of NAND gate I25, pin 6, would have a negative pulse present 10 times for every 400 trigger pulses.

The output of NAND gate, I26, pin 6, is the input of the $\div 38$ counter consisting of I28 and I29. The purpose of the $\div 38$ is two-fold. First, the $\div 38$ causes the sometimes highly irregular pulse spacing of the pulses out of NAND gate, I26, pin 6, to be much more regular. Secondly, the $\div 38$ causes the PRF of the ACCELERATION PULSE input to the VELOCITY REGISTER to be that required to correspond to the programmed acceleration.

52. VELOCITY REGISTER (C2)

PURPOSE:

To store the velocity rate that the test set has been programmed for.

OPERATION:

If the VELOCITY LOAD CONTROL line is at "0", the VELOCITY REGISTER consisting of I3, I4, I5 and I6 is loaded to a value determined by the REGISTER LOAD VALUE CONTROL.

If the VELOCITY CLEAR CONTROL line is at a "0", the VELOCITY REGISTER is cleared to zero.

When pulses are present at I3, pin 5, and a "1" is present at I3, pin 4, the VELOCITY REGISTER increments to a greater value at a rate determined by PRF of the ACCELERATION PULSE. If pulses are present at I3, pin 4 and a "1" present at I3, pin 5, the VELOCITY REGISTER increments to a lesser value.

The PRF of the pulses present at I4, pin 5 or I4, pin 4 is 1/10 the PRF present at I3, pin 5 or I3, pin 4.

53. VELOCITY RATE GENERATOR (C1 & C2)

PURPOSE:

To generate a string of pulses with a PRF which varies in accordance with the contents of the VELOCITY REGISTER. The pulses cause the contents of the DISTANCE REGISTER to be incremented.

OPERATION:

The operation of the VELOCITY RATE GENERATOR is very similar to that of the ACCELERATION RATE GENERATOR. The only differences being that the rate generator is a decade more complex, a $\div 81$ circuit is used instead of a $\div 38$, the rate generator will put out 4000 pulses for

53. VELOCITY RATE GENERATOR (C1 & C2) (Cont'd)
every 4000 trigger pulses, and that the rate generator and the ÷81 are reset and preset respectively for suitable operation in the POWER measurement mode by the VELOCITY RATE GENERATOR RESET line.
54. ZERO KNOTS DECODE (C2)
PURPOSE:
To cause the VELOCITY REGISTER to cease being incremented to lesser values when the contents are zero.

OPERATION:
Observation of the schematic shows that the output of inverter I18, pin 2, would go to a "0" only when the VELOCITY REGISTER content is zero.
55. 4000 KNOTS DECODE (C2)
PURPOSE:
To cause the VELOCITY REGISTER to cease being incremented to greater values when the contents become 4000.

OPERATION:
Observation of the schematic shows that the output of inverter I11, pin 14, would be a "0" only when the VELOCITY REGISTER contents are 4000.
56. VELOCITY INCREASE/DECREASE/ARINC P.O. CONTROL (C2)
PURPOSE:
To cause the contents of the VELOCITY REGISTER to be incremented to greater or lesser values in accordance with the selection of INCREASE or DECREASE . If the ARINC P.O. mode is selected the contents are automatically caused to be incremented to greater values after being incremented to zero.

OPERATION:
If the VELOCITY DECREASE CONTROL line is at a "0", the output of NOR gate I1, pin 1, is a "0" thus blocking any pulses on the ACCELERATION PULSE line from appearing at I3, pin 5, and a "1" to be present. There is under these conditions a "0" present at the output of NAND gate I17, pin 10, except for when the VELOCITY REGISTER contents are zero. This "0" allows the ACCELERATION PULSE to appear at I3, pin 4, causing the VELOCITY REGISTER to increment to a lesser value.

Due to the connections of I17, pin 6 to I17, pin 11 and I17, pin 10 to I17, pin 5, these two NAND gates operate as a R-S Flip Flop and tend to remain in a state even though the "0" is removed from the VELOCITY DECREASE or VELOCITY INCREASE line.

56. VELOCITY INCREASE/DECREASE/ARINC P.O. CONTROL (C2) (Cont'd)

Operation is similar to the above when the VELOCITY INCREASE CONTROL line is at "0" with the exception that the ACCELERATION PULSES appear at I3, pin 5 instead of I3, pin 4.

When the ARINC P.O. mode is selected and the VELOCITY REGISTER contents are zero, the "0" on the output of the ZERO KNOTS DECODE, present at the input of NAND gate I17, pin 12, causes the R-S Flip-Flop to change state with the result that the VELOCITY REGISTER is caused to increment to a greater value.

If the output of 4000 KNOTS DECODE becomes a "0" the R-S Flip-Flop changes state and the VELOCITY REGISTER increments to a lesser value.

57. 200 KNOTS PULSE GENERATOR (C2)

PURPOSE:

To generate a pulse, when the contents of the VELOCITY REGISTER become 200, which is used to Clear the contents of the ACCELERATION REGISTER.

OPERATION:

If both the VELOCITY DECREASE CONTROL line and the VELOCITY INCREASE CONTROL line are at a "1", I20, pin 4 and I20, pin 5 are at a "1". Under these conditions each time the 200 KTS. OUTPUT line of the VELOCITY REGISTER I5, pin 2, goes to a "1" from a "0", a negative pulse is caused to appear at the output of NAND gate I20, pin 10 on the ARINC P.O. CLEAR line which causes the ACCELERATION REGISTER to be cleared to zero.

58. DISTANCE REGISTER (C1 & C3)

PURPOSE:

To store the distance that the test set is programmed for.

OPERATION:

Operation of the DISTANCE REGISTER is identical to that of the VELOCITY REGISTER.

The outputs of the DISTANCE REGISTER are connected to the ZERO NMI. DECODE, the X99.99 NMI DECODE and the ARINC SHIFT REGISTER.

59. ZERO NMI DECODE (C3)

PURPOSE:

To prevent the DISTANCE REGISTER from being incremented to a lesser value when the contents are zero and to cause

59. ZERO NMi DECODE (C3) (Cont'd)
the incrementation of the DISTANCE REGISTER from lesser to greater values when the contents has been incremented to zero in the AUTO INBOUND/OUTBOUND mode.

OPERATION:

Examination of the schematic shows that the output of Inverter I28, pin 6, would be a "0" only when the DISTANCE REGISTER content is zero.

60. X99.99 NMi DECODE (C3)
PURPOSE:

To generate an output, when the contents of the DISTANCE REGISTER becomes X99.99, which may be used to cause the incrementation of the DISTANCE REGISTER to change from greater to lesser values when in the AUTO INBOUND/OUTBOUND mode. Also to prevent incrementation to greater values when the contents becomes 399.99.

OPERATION:

Examination of the schematic shows that the output of NAND gate I14, pin 10, would be a "0" only when the DISTANCE REGISTER contained X99.99. This would cause the output of NAND gate I15, pin 13, to be a "1" only when the DISTANCE REGISTER contained X99.99.

If the DISTANCE REGISTER contained 399.99, the output of NAND gate I14, pin 6 would be a "0".

61. DISTANCE INBOUND/OUTBOUND/AUTO CONTROL (C3)
PURPOSE:

To provide control of the incrementation of the DISTANCE REGISTER. In the INBOUND mode, incrementation is to lesser values until the contents become zero. In the OUTBOUND mode incrementation is to greater values until the contents become 399.99. In the AUTO INBOUND/OUTBOUND mode, the incrementation direction changes each time the contents become zero or X99.99.

OPERATION:

If the DISTANCE INBOUND CONTROL line were at a "0", any pulses present on the VELOCITY PULSE line are blocked from appearing at the output of NOR gate I27, pin 12, and a "1" is caused to be present at I15, pin 5, of the DISTANCE REGISTER (C1). There is under these conditions a "0" present on the output of NAND gate I16, pin 6, except when the DISTANCE REGISTER contents are zero. This "0" present on the input of NOR gate, I27, pin 14, allows the VELOCITY PULSE to appear at C1, I16, pin 4, of the DISTANCE REGISTER and thus cause the DISTANCE REGISTER to be incremented to a lesser value. Should the output of Inverter I28, pin 6, go to a "0", due to the DISTANCE REGISTER contents being zero, the "1" appearing at the input to NOR gate I27, pin 14, would prevent any VELOCITY PULSES from further incrementing the DISTANCE REGISTER.

61. DISTANCE INBOUND/OUTBOUND/AUTO CONTROL (C3) (Cont'd)

Operation when the OUTBOUND line is a "0", is very similar to the above. When the DISTANCE REGISTER contents are 39999, the "0" appearing at the input of NAND gate I16, pin 14 causes a "1" at the input of NOR gate I27, pin 10, thus preventing the DISTANCE REGISTER from being incremented to a larger value.

When neither the OUTBOUND or the INBOUND line is a "0", the DISTANCE INBOUND/OUTBOUND/AUTO CONTROL logic has control of the direction of incrementation. Each time the DISTANCE REGISTER contents are zero the "0" appearing at the input of NAND gate I16, pin 4, causes the R-S Flip Flop consisting of I16 to change state and hence the direction of incrementation of the DISTANCE REGISTER. Each time the DISTANCE REGISTER contains X99.99 the "0" appearing at the input of NAND gate I16, pin 15, causes the R-S Flip Flop to change state and hence cause the DISTANCE REGISTER to be incremented to a lesser value.

62. ZERO VELOCITY DISTANCE INCREMENTATION REVERSAL LOGIC (C3)
PURPOSE:

To generate a pulse, each time the contents of the VELOCITY REGISTER becomes zero, which is used to cause the direction of incrementation of the DISTANCE REGISTER to reverse.

OPERATION:

Each time the VELOCITY REGISTER contents become zero there is a falling edge generated on the ZERO VELOCITY line which causes the \bar{Q} output of either O.S. I26, pin 7, or I26, pin 9, to go to a "0". The O.S. with a "1" present at the R input is triggered. The negative pulse generated by the \bar{Q} output causes the R-S Flip-Flop, consisting of I16 of the DISTANCE OUTBOUND/INBOUND/AUTO CONTROL to change state and hence the direction of incrementation of the DISTANCE REGISTER.

63. REGISTER CLEAR GENERATOR (C9)
PURPOSE:

To cause the contents of the ACCELERATION, VELOCITY AND DISTANCE REGISTER to be cleared to zero each time power is applied to the test set and at the end of the POWER MEASUREMENT MODE of operation.

OPERATION:

Each time the +5V line goes to 5V, Q22, Q23 and Q24 are turned on thus causing the ACCELERATION CLEAR CONTROL, VELOCITY CLEAR CONTROL and the DISTANCE CLEAR CONTROL lines to go to zero, thus clearing these REGISTERS.

Each time the POWER CONTROL line goes to a "1" Q22, Q23 and Q24 are again turned on and hence the ACCELERATION, VELOCITY AND DISTANCE REGISTERS are cleared.

64. READOUT LOGIC (C2,C4,C5,C6)

PURPOSE:

To select the proper data to be displayed by the READOUT as determined by the READOUT SELECTOR and store this data in the latches.

OPERATION:

The READOUT LOGIC is scattered over C2, C4, C5 and C6. The operation will be explained for that portion located on C6 which is typical of all the rest.

The data to be displayed is selected by the Quad Multiplexers I7 and I8 which are controlled by the S0 and S1 lines. The states of the S0 and S1 lines are controlled by the READOUT SELECTOR.

The table below relates the data displayed to the states of the S0 and S1 lines.

	S0	S1
Output of Counter located on C3 - XPDR % Return, ΔF , Squitter Rate and Interro Rate	0	0
Acc. Register Contents	1	0
Vel. Register Contents	0	1
Output of ARINC Shift Register located on C4- Test Distance Register Contents, Measured Distance and Power	1	1

65. READOUT DRIVER LOGIC, L1 AND READOUT

PURPOSE:

To cause the readout to:

- A. Display the correct numerals.
- B. Display a decimal point in the proper position when called for.
- C. Ripple blank in the proper manner.
- D. Blank upon command.
- E. Display dashes upon command.
- F. Display a minus sign at the 1st MSD upon command.
- G. Display an overrange sign upon command.

OPERATION:

A. CORRECT NUMERALS

The 5th MSD A,B,C & D inputs to I8, pins 1,2,6 and 7 are converted to the proper seven segment code to cause the 5th MSD to display the number called for.

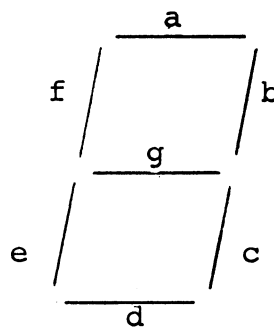
65. READOUT DRIVER LOGIC, L1 AND READOUT (Cont'd)

See table below.

Decimal	INPUTS				OUTPUTS						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	1	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	1	1	0	0

When an output line is at a "0" that particular segment of the LED display lights.

See below for the LED display segment layout:



B. DECIMAL POINT DISPLAY

A decimal point is displayed in accordance with the table below:

Decimal Point Position	Mode	Control Line
X.XX	Test Distance Meas. Distance	4th MSD D.P. =1
X.XXB	ΔF	$\Delta F \overline{\text{Control}}=1$

C. RIPPLE BLANK

The READOUT RIPPLE BLANKS in accordance with the following table:

Digits that may Ripple Blank	Mode	Control Line
1st MSD 2nd MSD	Test Dist. Meas. Distance Power	
* 2nd MSD 3rd MSD 4th MSD	Vel. Acc. Interro Rate Squitter Rate XPDR % Return	Dist/Pwr #2 allows 3rd and 4th MSD to Ripple Blank
* **	ΔF	ΔF Control

- * 1st MSD is blanked by the DISTANCE/POWER #1 line.
- ** 5th MSD is blanked by the ΔF CONTROL line.

D. BLANK

The READOUT BLANKS in accordance with the following table:

Digit	Mode	Control Line
1st MSD	All Modes except Test Dist and Meas. Dist.	Dist/Pwr #1
All	Meas. Dist.	Readout Blank
5th MSD	ΔF	ΔF Control

E. DISPLAY DASHES

When the READOUT DASHES line becomes a "1" the "a,b,c,d,e,g" outputs of I6, pins 9,10,12,13 and 14 go to a "0". Since they are wired in parallel with the g outputs of I3, I4, I5, I7, I8, pin 14, the READOUT displays DASHES.

F. MINUS SIGN

When the READOUT MINUS line is at a "1" the "g" segment of the 1st MSD is turned on. The MINUS sign is displayed only in the ACCELERATION, VELOCITY, or ΔF modes. The 1st MSD Driver, I3, is blanked during these modes.

G. OVERRANGE SIGN

When the READOUT OVERRANGE line is at a "1" the "a" segment of the 1st MSD is turned on. This occurs only in the ΔF mode.

66. LOCAL/REMOTE CONTROL LOGIC, LOCAL/REMOTE LOAD VALUE LOGIC, READOUT UNITS LOGIC, L2 AND READOUT PURPOSE:

A. LOCAL/REMOTE CONTROL LOGIC,

To allow the remoting of many of the switch controls on the front panel by the removal of a "0" on the switch common.

B. LOCAL/REMOTE LOAD VALUE LOGIC

To allow the ACCELERATION, VELOCITY, and DISTANCE REGISTERS to be loaded by remote means.

C. READOUT UNITS CONTROL LOGIC

1. To cause the appropriate UNITS to appear at the READOUT as determined by the READOUT SELECTOR switch.
2. To generate control inputs to the READOUT DRIVER LOGIC, L1, to cause proper operation of the READOUT as determined by the READOUT SELECTOR switch.
3. To cause the S0 and SI output lines to have the proper states.

OPERATION:

A. LOCAL/REMOTE CONTROL LOGIC

When the REMOTE-LOCAL switch is placed in the ALL REMOTE position, the outputs of the inverters assume a "1" unless a REMOTE CONTROL input line places them at a "0".

B. LOCAL/REMOTE LOAD VALUE LOGIC

The ACCELERATION, VELOCITY and DISTANCE REGISTER LOAD VALUES are determined by the "1" on the outputs of the NAND gates. In the LOCAL CONTROL mode, the

LOAD VALUE CONTROL places a "0" on the inputs to obtain a "1" on the outputs. In the REMOTE CONTROL mode the LOAD VALUE CONTROL switch commons are at "1" allowing the REMOTE CONTROL inputs to determine the LOAD VALUES.

C. READOUT UNITS CONTROL LOGIC

The READOUT SELECTOR places a "0" on the appropriate inverter input causing the associated transistor to saturate causing the proper units to be displayed by the READOUT. The table below gives the UNITS vs. the mode.

MODE	UNITS
XPDR % Return	%
ΔF	MHz
Squitter Rate	PPS
Interro Rate	PPS
Acc.	FPS
Vel.	KTS
Test Dist.	NMi
Meas. Dist.	NMi
Power	WTS

The outputs to the READOUT DRIVER LOGIC, L1, are listed below vs. mode.

OUTPUT LINE	MODE
4th MSD D.P.	At "1" in Test Dist. and Meas. Distance only
Dist./Pwr #1	May or may not be "1" in Test Dist., Meas. Dist. or Power Modes. At "0" all other modes
Dist./Pwr #2	At "1" in Test Dist., Meas. Dist. and Power Modes only.

The table below relates the position of the Readout Selector to the state of the S0 and S1 lines.

	S0	S1
XPDR %Return, ΔF , Squitter Rate, Interro. Rate	0	0
Acceleration	1	0
Velocity	0	1
Test Distance, Meas. Dist., Power	1	1

67. STROBE/MINUS SW. (C3)

PURPOSE:

To select the proper input to the Readout Minus line, ΔF Minus, Negative Acceleration or Negative Velocity. Also to select the proper input to the READOUT STROBE line, Dist. PWR SHIFT, TIME BASE STROBE or a "0".

OPERATION:

The STROBE/MINUS switch is controlled by the S0 and S1 input lines.

The table below relates the input to the READOUT STROBE line to the states of the S0 and S1 lines.

	S0	S1
Time Base Strobe-XPDR % Return, ΔF , Squitter Rate and Interro Rate	0	0
"0"	1	0
"0"	0	1
Dist./PWR Shift	1	1

The table below relates the input to the READOUT MINUS line to the states of the S0 and S1 lines.

	S0	S1
ΔF Minus	0	0
Negative Acceleration	1	0
Negative Velocity	0	1
"0"	1	1

75. TIME BASE COUNTER (C5)

PURPOSE:

To generate the correct time base for the COUNTER. The TIME BASE COUNTER is controlled by the TIME BASE COUNTER PROGRAM LOGIC.

OPERATION:

The TIME BASE COUNTER is made up of 3 programmable, cascadable, modulo-N down counters. The method of cascading them is to connect the BUSS outputs, pin 12, together and driving the CLOCK input, pin 6, of each succeeding counter by the Q3 output, pin 1, of the preceeding counter.

Their operation is such that when cascaded they count down to 0000,0000,0000 state. At that time the "BUSS" line goes to a "1". When the counter clock goes to a "0" the counter is then preset to that value determined by the state of the preset inputs, P0,P1,P2,P3, at which time the BUSS line goes to "0".

The programming of the TIME BASE COUNTER is controlled by the TIME BASE COUNTER PROGRAM LOGIC. This program N is 101 for the % RETURN mode, varies from 990 to 999 for the SQUITTER RATE mode, and is determined by FREQUENCY CONTROL LOGIC, L3, in the ΔF mode. This is further explained in the description of the TIME BASE COUNTER PROGRAM LOGIC operation.*

76. TIME BASE COUNTER PROGRAM LOGIC (C5)

PURPOSE:

To generate the proper programming of the TIME BASE COUNTER as determined by the various inputs.

OPERATION:*

% RETURN MODE

In the % RETURN mode the TIME BASE COUNTER is programmed to $\div 101$ and is accomplished in the following manner. The "0" on the % RETURN CONTROL line causes a "0" to appear on the R input to I2, pin 6, and on an input to AND gate I25, pin 12 which causes the XPS CONTROL line and the PS CONTROL line to be a "0". These "0"'s cause the outputs of AND gates, I3, pins 6, 10, and 13 and I4, pin 3, 6, 10 and 13 to be at a "0".

The "0" present on the % RETURN line also causes a "1" to appear at the emitter of Q4 which causes Q2 to saturate producing a "0" on the outputs of I8, Pins 3, 6, 10 and 13 and I9, pins 3 and 6. The "1" present on the emitter of Q4 causes the P0 input to I7, Pin 5 and I5, pin 5, to be a "1". Thus since all other P0, P1, P2 and P3 inputs to I5, I6, and I7 are at a "0" the TIME BASE COUNTER is programmed to $\div 101$.

*See figure 8.

76. TIME BASE COUNTER PROGRAM LOGIC (C5) (Cont'd)

Since the input to AND gate I3, pin 1, is at a "1" all pulses present on the "BUSS" line of the TIME BASE COUNTER appear on the TIME BASE PULSE line.

SQUITTER RATE MODE AND DME INTERRO. RATE MODE.

In the SQUITTER RATE mode and the INTERRO RATE mode the TIME BASE COUNTER is programmed in the following manner.

The "0" present on the SQUITTER RATE CONTROL line causes a "1" to appear on the P3 input to I7, pin 2, and at the emitter of Q3 and a "1" to always be present on the \overline{MR} inputs of I6 AND I7, Pin 10.

The "1" present on the emitter of Q3 causes Q2 to saturate thus causing the outputs of I8, pins 3,6,10 and 13 and I9, pins 3 and 6 to be at a "0". This "1" causes the P0 and P3 inputs to I5 and I6, pins 5 and 2, and P0 of I7, pin 5, to be at a "1". Thus I6 and I7, are programmed to 9. The situation at the P0, P1, P2 and P3 inputs to I5, pins 5,11,14 and 2, is somewhat more complicated. While the P0 and P3 inputs are always at a "1", the P1 and P2 inputs may at sometime see a "1". This is because as the \overline{Q} and Q outputs of I2A, pins 10 and 11, alternate from "1" to "0" the outputs of I3, pins 10 and 13, and I4, pins 6 and 10, may or may not be a "1" depending on the values on their inputs, I3, pins 1, 11 and 15, and I4, pins 4 and 11, which are determined by the frequency the RF Generator is channelled to. However, when the \overline{Q} output of I2A, pin 10, is a "1" I5 may be programmed to 0,2 or 9, and when the Q output is a "1" programmed to 2,6 or 9. Thus the TIME BASE COUNTER may be programmed to 990, 992, or 999 in one instance and 992,996 or 999 in the other. Since there is a pulse on the TIME BASE PULSE line generated at the output of I3, pin 3, only when the \overline{Q} output of I2A, pin 10, is a "1", the TIME BASE COUNTER is effectively programmed to $\div 990 + 992 = 1982$ as a lower limit to $\div 999 + 999 = 1998$ as the upper. Since the desired spacing of the TIME BASE COUNTER is 1 sec and the worst case error is $1982/2000$ sec, which is 1 sec-.0018 sec, the error is quite small.

Δ F MODE

In the Δ F mode the TIME BASE COUNTER is programmed in the following manner.

Since neither the % RETURN CONTROL line nor the SQUITTER RATE CONTROL line is at a "0" the programming of I6 and I7 is determined by the FREQUENCY CONTROL LOGIC.

The programming of I5 is more complicated in that as the \overline{Q} and Q outputs of I2A, pins 10 and 11, alternate between "1" and "0" the state of the XPS CONTROL line and the PS CONTROL line

△F MODE CONTINUED

alternates between "1" and "0". Thus the programming of I5 alternates between that determined by the XPS 4 and XPS 8 inputs and the PS1, PS2, PS4 and PS8 inputs.

When the \bar{Q} output of I2A, pin 10 is a "0" there is a "0" present at the \overline{MR} inputs to I6 and I7, pin 10, which causes these counters to be preset to 0000. Thus when I5 counts down to 0000 the BUSS line rises. When the counter clock goes to a "0" the BUSS line falls triggering the \bar{Q} output of I2A, pin 10, to a "1" which allows I6 and I7 to be programmed. The result is that the TIME BASE COUNTER counts down to 0000,0000,0000 from the programming as determined by the PS inputs, programs to 0000,0000,XXXX as determined by the XPS inputs and counts down to 0000,0000,0000 and then repeats. Since the TIME BASE PULSE only appears when the \bar{Q} output of I2A, pin 10, is a "1" the effective programming of the TIME BASE COUNTER is $\div(\text{PS INPUTS} + \text{XPS INPUTS} + 1)$.

77. TIME BASE STROBE LOGIC (C5)

PURPOSE:

To generate a STROBE PULSE which is used to strobe the latches in the READOUT LOGIC.

OPERATION:

When the TIME BASE PULSE first appears the TIME BASE COUNTER CLOCK is a "1". These "1"'s present at the inputs to AND gate I25, pins 1 and 2 cause a "0" on the TIME BASE STROBE line. The width of this negative pulse is the width of the positive clock pulse.

78. COUNT INHIBIT LOGIC (C5)

PURPOSE:

To inhibit the count input to the COUNTER during the TIME BASE STROBE interval.

OPERATION:

During the interval that the TIME BASE STROBE line is a "0", a "1" is present at the input to NOR gate I26, pin 14. This "1" causes the COUNTER CLOCK line to go to a "1". Since the COUNTER operates on a falling edge there are no further changes in the COUNTER state during the TIME BASE STROBE interval.

79. COUNTER RESET LOGIC (C5)

PURPOSE:

To generate a reset pulse which is used to reset the COUNTER immediately following the strobe.

79. COUNTER RESET LOGIC (C5) (Cont'd)
OPERATION:

In the interval that the TIME BASE PULSE is still a "1" and the TIME BASE COUNTER CLOCK is a "0", a "1" is generated at the output of AND gate, I25, pin 6 which causes the R-S F/F consisting of NOR gates I15, pins 10, 11 and 12 and I15, pins 13, 14 and 15 to change state thus generating a "0" on the COUNTER RESET line. When the TIME BASE COUNTER CLOCK goes to a "1" again the R-S F/F changes state again and causes a "1" to appear on the COUNTER RESET line.

80. TIME BASE/COUNTER SWITCH (C5)
PURPOSE:

To select the proper input for the TIME BASE COUNTER CLOCK line and the COUNTER CLOCK line.

OPERATION:

The input to the TIME BASE COUNTER CLOCK line and the COUNTER CLOCK line is selected by means of a DUAL 4 CHANNEL DATA SELECTOR, I17, which is controlled by the SQUITTER RATE CONTROL line, the % RETURN CONTROL line and the DME INTERROGATION RATE line. The ΔF mode is selected if none of the above three is selected. See table below for mode vs. input selected.

MODE	TIME BASE COUNTER CLOCK	COUNTER CLOCK
ΔF	2KHz	The output of the PHASE/FREQ. DET - the BEAT FREQ.
SQUITTER RATE	2KHz	SQUITTER/INTERRO. RATE PULSE
% RETURN	XPDR INTERRO RATE	XPDR RETURN
DME INTERRO. RATE	2KHz	DME INTERRO RATE

81. COUNTER (C3)
PURPOSE:

To count either the output rate of the SQUITTER RATE GENERATOR in the SQUITTER RATE mode, the XPDR returns in the % RETURN mode, the DME INTERROGATION RATE in the INTERROGATION RATE mode, or the BEAT FREQUENCY in the ΔF mode.

81. COUNTER (C3) (Cont'd)

OPERATION:

The COUNTER consists of I4, I5, I6, and I7. The COUNTER is clocked by the COUNTER CLOCK line and RESET by a "0" on the COUNTER RESET line.

The output of the counter, I4, I5, I6 and I7, pins 2,5,11 and 14 are connected to the READOUT LOGIC.

82. COUNTER OVERRANGE LOGIC (C3)

PURPOSE:

To store a "1" on the COUNTER OVERRANGE line when the COUNTER has been clocked past its maximum value of 9999.

OPERATION:

If the contents of the COUNTER are clocked from 9999 to 0000, I3 is clocked. The "1"'s appearing on the outputs of I3, pins 5, 11, 14 and 2 are strobed into I2 by the READOUT STROBE. The "1" then appearing on the OVERRANGE line causes the OVERRANGE segment to light on the READOUT.

83. DME INTERROGATION RATE O.S. (C8)

PURPOSE:

To generate a single pulse for each DME U.T. INTERROGATION PULSE PAIR.

OPERATION:

The pulse on the DEMODULATOR 50% LEVEL PULSE line causes the Q output of I24, pin 6, to be triggered to a "1". The pulse width of the O.S. is long enough to prevent the forming of two pulses by the DME U.T. INTERROGATION PULSE PAIR.

90. PHASE/FREQUENCY DETECTOR (C5)

PURPOSE:

To cause the frequency difference between the 2 MHz REFERENCE and the 2 MHz VFO to appear at the output of NOR gate I26, pin 6, the BEAT FREQUENCY line. Also to cause a "0" to appear at the output of I24, pin 13, the ΔF Minus line if the 2 MHz VFO frequency is less than the 2 MHz reference frequency.

OPERATION:

The purpose of the PULSE GENERATOR block in the PHASE/FREQUENCY DETECTOR is to generate a positive pulse of approximately 50 nsec duration each time there is a falling edge present at the PULSE GENERATOR input. These pulses are the inputs to the PHASE/FREQUENCY DETECTOR.

The pulses generated by the PULSE GENERATOR are the inputs to the PHASE/FREQUENCY DETECTOR.

The operation of the PHASE/FREQUENCY DETECTOR is such that when the PRF of the pulses present at I24, pin 1 is greater than the PRF of those present at I24, pin 11, the output of I24, pin 13 becomes a "0" and there are pulses present at the output of I24, pin 6 which appear at the output of NOR gate I13, pin 13. See Fig. 1.3 in the FREQUENCY GENERATOR section. These pulses vary in duty cycle from essentially 0 to 100% at a rate which is equal to the difference between the PRF's present at I24, pin 1 and I24 pin 11. The varying duty cycle pulses are filtered by the LOW PASS FILTER leaving a sawtooth pulse which is squared by NOR gates I26, pins 1,2,3,4,5 and 6. Thus a pulse is generated on the BEAT FREQUENCY line with a PRF which is the difference frequency between the 2 MHz REFERENCE and the 2 MHz VFO frequencies.

91. UNCAL SWITCH (C5)

PURPOSE:

To select as the input to PULSE GENERATOR #2 either the 2 MHz VFO in the UNCAL mode or the 2 MHz REFERENCE in the CAL mode.

Since in the CAL mode the inputs to PULSE GENERATOR #1 and #2 are both the 2 MHz REFERENCE the difference frequency on the BEAT FREQUENCY line is 0.

OPERATION:

When the FREQ. UNCAL line is at a "1", the 2 MHz REFERENCE frequency is blocked from appearing at the input to NOR gate I22, pin 12, whereas the 2 MHz VFO frequency is allowed to appear at the input to NOR gate I22 pin 11.

92. ΔF MINUS INHIBIT (C5)

PURPOSE:

To prevent the READOUT from displaying a MINUS when the READOUT mode is other than the ΔF mode.

OPERATION:

If there is not a "1" present on the ΔF line, the output of Inverter, I28, pin 4, inhibits a "1" from appearing on the ΔF MINUS line should the PHASE/FREQUENCY DETECTOR indicate that it should.

This prevents the MINUS segment from lighting in any but the ΔF mode due to a "1" on the ΔF MINUS line. When the ΔF mode is selected, the "0" on the ΔF CONTROL line allows the ΔF MINUS line to assume a "1" should the ΔF MINUS input to Q1 be a "0".

100. POWER MEASURE ΔT GENERATOR (C11)

PURPOSE:

To generate a time interval, ΔT , proportional to the DC voltage on the PULSE PEAK LEVEL line.

OPERATION:

The source of the voltage present at I3, pin 2, is the PULSE PEAK LEVEL line and is generated by the PULSE PEAK DETECTOR located on the DEMODULATOR, G23.

Each time the PUT OSCILLATOR Q3, generates a falling edge at the C input of I4, pin 5, the \bar{Q} output, I4, pin 8 is triggered to a "0" which causes Q2 to shut off allowing C4 to be charged by the current from the constant current source consisting of Q1 and I1. When the voltage at I2, pin 3 and I3, pin 3 exceeds that present at I3, pin 2, a "0" is generated at the R input to I4, pin 6, which causes a "1" to appear at the \bar{Q} output of I4, pin 8. Thus a positive pulse is generated at the Q output of I4, pin 9, on the ΔT line. The pulse width is directly proportional to the voltage present on the PULSE PEAK LEVEL line.

101. POWER MEASURE TIMING GENERATOR (C11, C1)

PURPOSE:

To generate the necessary timing of the pulses on the T1, T2, ΔT , POWER SHIFT, and POWER CLEAR lines to cause the VELOCITY REGISTER, VELOCITY RATE GENERATOR, and DISTANCE REGISTER to compute the power level by a digital means.

OPERATION:

Each time the PUT OSCILLATOR Q3, generates a negative edge at the C input to I4B, the T1 and T2 lines change state.

In the T2=1 interval the falling edge generated at the input to O.S. I5, pin 5, at the end of the ΔT period triggers the \bar{Q} output of I5A to a "0" thus generating a negative pulse on the POWER SHIFT line.

The falling edge present at the input to I5, pin 11, at the end of the POWER SHIFT period, generates a falling edge at the Q output of I5B, after the O.S. period. This falling edge at the input to O.S. I6, pins 1 and 2, generates a positive pulse on the POWER CLEAR line.

The output of AND gate, I10, pin 3 of C1, the ΔT_1 line, is a "1" only during the ΔT interval in the T1 period.

The output of AND gate I10, pin 6, the ΔT_2 line is a "1" only during the ΔT interval in the T2 period.

101. POWER MEASURE TIMING GENERATOR (C11, C1) (Cont'd)

During the interval that $\Delta T_1=1$ the 27 KHz present at the input of AND gate I10, pin 12, appears on the 27 KHz $X\Delta T_1$ line. Due to the switching provided by the NORMAL/POWER SWITCH, this 27KHz appears on the ACC.PULSE line and is applied to the count up input to the VELOCITY REGISTER.

During the interval that $\Delta T_2=1$ the reset inputs of the VELOCITY RATE GENERATOR are released by the VELOCITY RATE GENERATOR RESET line and the DISTANCE REGISTER is clocked up to a value proportional to the $(\Delta T)^2$ since the output of the VELOCITY RATE GENERATOR is proportional to ΔT and the length of time the DISTANCE REGISTER is clocked is proportional to ΔT .

Following the ΔT_2 interval the POWER SHIFT pulse is generated which causes the contents of the DISTANCE REGISTER to be stored in the READOUT LOGIC and displayed. The POWER CLEAR pulse is generated which resets the VELOCITY REGISTER and the DISTANCE REGISTER to zero.

102. NORMAL/POWER SWITCH (C5)

PURPOSE:

To remove control of the VELOCITY REGISTER and DISTANCE REGISTER from the VELOCITY INCREASE/DECREASE CONTROL and the DISTANCE INBOUND/OUTBOUND CONTROL and cause these REGISTERS to always be incremented to greater values.

OPERATION:

Obvious.

103. NORMAL/POWER SWITCH (C1, I9, PINS 2,3 and 4)

PURPOSE:

To cause the reset inputs in the VELOCITY RATE GENERATOR, the VELOCITY RATE GENERATOR RESET line to be controlled by the ΔT_2 pulse. The use of the reset inputs to control the count input to the DISTANCE REGISTER causes the VELOCITY RATE GENERATOR to start from the same initial conditions each time.

OPERATION:

Obvious.

104. NORMAL/POWER SWITCH (C1, I9, PINS 12, 13 and 14)

PURPOSE:

To cause the clock input to the VELOCITY RATE GENERATOR, the 9KHz/2MHz line to change from 9KHz in the NORMAL mode to 2 MHz in the POWER mode.

OPERATION:

Obvious.

105. NORMAL/POWER SWITCH (C1, I9, PINS 5, 6, AND 7)

PURPOSE:

To cause the clock input to the VELOCITY REGISTER, the ACCELERATION PULSE line, to change from the output of the ACCELERATION RATE GENERATOR in the NORMAL mode to the burst of 27KHz during the ΔT_1 interval in the POWER mode.

OPERATION:

Obvious.

106. NORMAL/POWER SWITCH (C1, I9, PIN 9, 10, AND 11)

PURPOSE:

To cause the DISTANCE/POWER SHIFT line input to the ARINC SHIFT REGISTER to be the DISTANCE SHIFT line in the NORMAL mode and the POWER SHIFT line in the POWER mode. When the READOUT SELECTOR is in the TEST DISTANCE, MEASURE DISTANCE or the POWER position, the DISTANCE/POWER SHIFT line is the input to the READOUT STROBE.

OPERATION:

Obvious.

107. NORMAL/POWER SWITCH (C6)

PURPOSE:

To disconnect the BUSS 1, BUSS 2, BUSS 3 outputs of the DISTANCE DELAY COUNTER from the REPLY LOGIC and the INHIBIT SQUITTER LOGIC and cause "1"'s to be present.

Thus in the POWER mode the REPLY is generated at the end of the INITIAL DELAY, hence causing the DME U.T. to lock at 0 NMi.

OPERATION:

Obvious.

125. INDICATOR U.T. SERIAL BCD CLOCK OSCILLATOR (C9, C4)

PURPOSE:

To generate pulses with a PRF variable between 7 and 15 KHz by means of the SERIAL DATA CLOCK control to be used as the source of the INDICATOR U.T. SERIAL BCD CLOCK output.

OPERATION:

As the voltage on resistor, R83 of Card 9, is varied by means of the SERIAL DATA CLOCK control the PRF of the pulse on the 14-30 KHz CLOCK varies.

The 14-30 KHz CLOCK line is divided by I21, pin 15 so as to generate a 7-15 KHz CLOCK output with a 50% duty cycle pulse.

126. DME U.T./INDICATOR U.T. SERIAL BCD CLOCK SWITCH (C4)

PURPOSE:

To cause the source of pulses on the SHIFT CLOCK No. 1 and SHIFT CLOCK No. 2 lines to change from the 7-15 KHz CLOCK line to the DME U.T. CLOCK line in the MEASURE DISTANCE mode.

Also to cause the INDICATOR U.T. CLOCK line to be at a "1" in MEASURE DISTANCE mode.

OPERATION:

Obvious.

127. WORD SYNCHRONIZATION LOGIC (C4)

PURPOSE:

INDICATOR U.T. (TEST DISTANCE) MODE

Upon the command of the INDICATOR U.T. MINIMUM DATA RATE GENERATOR or a VELOCITY PULSE cause.

1. An INDICATOR U.T. SYNC PULSE
2. The ARINC SHIFT REGISTER to shift out the TEST DISTANCE in SERIAL BCD form.

DME U.T. (MEASURE DISTANCE) MODE

Upon command of the DME U.T. SYNC PULSE cause the ARINC SHIFT REGISTER to shift in the SERIAL BCD DISTANCE DATA from the DME U.T.

OPERATION:

See TIMING DIAGRAM shown in figure 7. The SHIFT START PULSE is shown for the case of initiation of a shift due to a VELOCITY PULSE. This pulse will be of varying width when initiation is due to a pulse on the INDICATOR U.T. MINIMUM DATA RATE line. All other events follow.

127. WORD SYNCHRONIZATION LOGIC (C4) (Cont'd)

The SHIFT CLOCK No. 2 pulses are numbered for both the INDICATOR U.T. mode and DME U.T. mode. SHIFT CLOCK No. 2 is the INDICATOR U.T. CLOCK or the DME U.T. CLOCK in the respective modes.

The VELOCITY PULSE causes the SHIFT START PULSE line to be triggered to a "1" which causes the DISTANCE SHIFT line to be triggered to a "0". This allows the counter consisting of I24 and I17 to be clocked by SHIFT CLOCK No. 2. At the start of SHIFT CLOCK No. 2 pulse 32 the SHIFT STOP PULSE line becomes a "1" which causes the DISTANCE SHIFT line to be triggered to a "1" upon the 33rd SHIFT CLOCK No. 2 pulse which resets the counter, I24 and I17 to zero.

128. INDICATOR U.T. MINIMUM DATA RATE GENERATOR (C9)

PURPOSE:

To cause the transmission of the TEST DISTANCE DATA at a rate not less than 5 times a second.

OPERATION:

In all modes, except MEASURE DISTANCE mode, the MEASURE DISTANCE CONTROL line is at a "0" which allows Q17 to shut off. If no VELOCITY PULSES are present, when the anode voltage of Q16 exceeds that of the gate, a negative pulse is generated on the INDICATOR U.T. MINIMUM DATA RATE line. If VELOCITY PULSES are present, pulses on the DISTANCE SHIFT line cause Q17 to discharge C22.

129. INDICATOR U.T. INHIBIT LOGIC (C4)

PURPOSE:

To cause the INDICATOR U.T. SYNC and the INDICATOR U.T. DISTANCE DATA to be inhibited in the DME U.T. (MEASURE DISTANCE) mode.

OPERATION:

When the MEASURE DISTANCE CONTROL line is at a "1" the DISTANCE SHIFT line is prevented from causing the SYNC/ DATA INHIBIT line from becoming a "1" during the shift cycle.

130. INDICATOR U.T. DASH LOGIC (C4)

PURPOSE:

To prevent the TEST DISTANCE DATA from appearing on the INDICATOR U.T. DISTANCE DATA line when the SERIAL DATA OUTPUT control is in the DASH position.

OPERATION:

The "1" on the DASH line, I26, pin 11, causes the output I26, pin 10, to become a "0" when the DATA INHIBIT line I26, pin 12, becomes a "1" thus preventing the data on the INDICATOR U.T. DISTANCE DATA line, I18, pin 5, from appearing on the INDICATOR U.T. DISTANCE DATA line.

131. NORMAL/POWER SWITCH (C4)

PURPOSE:

To eliminate an output on the INDICATOR U.T. DISTANCE DATA line and to cause the SHIFT CLOCK No. 1 line to be "0" in the POWER mode.

OPERATION:

Obvious.

132. ARINC SHIFT REGISTER (C4)

PURPOSE:

INDICATOR U.T. (TEST DISTANCE) MODE

To cause the transmission of the LABEL, PAD, DISTANCE DATA and, when called for, the DASH command on the INDICATOR U.T. DISTANCE DATA line.

DME U.T. (MEASURE DISTANCE) MODE

To cause the reception of the LABEL, PAD, DISTANCE DATA and, when present, the DASH command present on the DME U.T. DISTANCE DATA line.

OPERATION:

The table below gives the conditions for the various control lines of the ARINC SHIFT REGISTER and the resulting action.

LOAD/ SHIFT CONTROL P6	PARALLEL LOAD CLOCK P10	SHIFT CLOCK No. 1 P11	RESULT
1	Pulses present in all modes except MEAS. DIST.	X	Parallel loading of the contents of the Dist. Register.
1	1 present in MEAS. DISTANCE	X	No Change
0	X	Shift Pulses	Shift. Either the shifting out of the TEST DIST. to the Ind. U.T. or the shifting in of the DME U.T. DIST. DATA

133. LABEL/PAD DECODE (C4)

PURPOSE:

To decode the LABEL and PAD of the DME U.T. for correctness.

133. LABEL/PAD DECODE (C4) (Cont'd)

OPERATION:

The DME U.T. DISTANCE DATA is inverted by I12, pins 12 and 13, with the result that the all voltages on the anodes of diodes I14, pins 1 thru 16, must be at a "1" for the LABEL and PAD to be correct. If they are not, a "0" appears on the LABEL/PAD FAULTY line after the shift.

134. DME U.T. DATA RATE MONITOR (C4)

PURPOSE:

To cause the READOUT to BLANK in the DME U.T. (MEASURE DISTANCE) mode if the data transmission rate is not at least 5 transmissions per second.

OPERATION:

Each time the ARINC SHIFT REGISTER shifts, pulses on the INDICATOR U.T. DISTANCE DATA line triggers the Q output of I27, pin 10 to a "1". If the "1" is not present, the readout blanks in the DME U.T. (MEASURE DISTANCE) mode.

135. DME FLAG ALARM RECEIVER (C9)

PURPOSE:

To cause the READOUT to BLANK in the DME U.T. (MEASURE DISTANCE) mode when the DME U.T. FLAG ALARM line becomes less than 1.0 volt.

OPERATION:

When the DME U.T. FLAG ALARM line becomes 1.0 volt or less, Q5 and Q6 turn on causing the ALARM line to go to "0".

136. DME U.T. INDICATOR BLANK LOGIC (C4)

PURPOSE:

To cause, in the DME U.T. (MEASURE DISTANCE) mode only, the READOUT to BLANK if:

1. The LABEL/PAD is faulty
2. The data transmission rate is low
3. The DME U.T. FLAG ALARM line is low
4. If the display of DASHES is called for

OPERATION:

If either of the LABEL/PAD FAULTY, the DME DATA RATE LOW, the ALARM or the DISPLAY DASHES lines are low, a "1" appears on the READOUT BLANK line causing the READOUT to BLANK.

137. DME U.T. INDICATOR DASH LOGIC (C4)

PURPOSE:

To cause, in the DME U.T. (MEASURE DISTANCE) mode only, the READOUT to display DASHES upon the command of the DME U.T.

137. DME U.T. INDICATOR DASH LOGIC (C4) (Cont'd)
OPERATION:
If after the end of the shift cycle a "0" is present on the DISPLAY DASHES line a "1" appears on the READOUT DASH line causing the READOUT to display DASHES.
138. INDICATOR U.T. SERIAL BCD CLOCK DRIVER (C10)
PURPOSE:
To generate pulses of the proper amplitude with correct rise and fall times on the INDICATOR U.T. SERIAL BCD CLOCK line upon command of the INDICATOR U.T. CLOCK line.

OPERATION:
The low CLOCK pulse level is determined by the CLOCK LO LEVEL pot, R22, while the high CLOCK pulse level is determined by the CLOCK HI LEVEL pot, R18. The rise and fall times of each pulse is determined by the INTEGRATOR consisting of I5, C5, R17 and R65.
139. INDICATOR U.T. SERIAL BCD WORD SYNC DRIVER (C10)
PURPOSE:
Same as for INDICATOR U.T. SERIAL BCD CLOCK DRIVER.

OPERATION:
Very similar to that of the SERIAL BCD CLOCK DRIVER.
140. INDICATOR U.T. SERIAL BCD DISTANCE DATA DRIVER (C10)
PURPOSE:
Same as for INDICATOR U.T. SERIAL BCD CLOCK DRIVER.

OPERATION:
Very similar to that of the INDICATOR U.T. SERIAL BCD CLOCK DRIVER.
141. DME U.T. SERIAL BCD CLOCK RECEIVER (C9)
PURPOSE:
To translate the DME U.T. SERIAL BCD CLOCK levels to TTL levels and to determine if the DME U.T. SERIAL BCD CLOCK pulse levels are proper.

OPERATION:
As the output of I3, pin 7 alternates between "1" and "0" Q3 is turned on and off causing the minus input to I3, pin 3 to be at either 5.0 volts or 0.5 volts. Thus the DME U.T. SERIAL BCD CLOCK line must exceed 10 volts at the high pulse level and be less than 1 volt at the low level for proper operation of the RECEIVER.

142. DME U.T. SERIAL BCD WORD SYNC RECEIVER (C9)
PURPOSE:
Same as for the DME U.T. SERIAL BCD CLOCK RECEIVER.

OPERATION:
Very similar of that for the DME U.T. SERIAL BCD CLOCK RECEIVER.
143. DME U.T. SERIAL BCD DISTANCE DATA RECEIVER (C9)
PURPOSE:
Same as for the DME U.T. SERIAL BCD CLOCK RECEIVER.

OPERATION:
Very similar of that for the DME U.T. SERIAL BCD CLOCK RECEIVER.
144. INDICATOR U.T. WARNING FLAG DRIVER (C11)
PURPOSE:
To cause the INDICATOR U.T. to display the WARNING FLAG upon command of the SERIAL DATA OUTPUT control.

OPERATION:
When the SERIAL DATA OUTPUT CONTROL is placed in the FLAG position the INDICATOR U.T. WARNING FLAG line goes low to a level of approximately 1 volt. When the FLAG is not called for, the INDICATOR U.T. WARNING FLAG line is at a level determined by the WARNING FLAG LEVEL pot, R21, which is normally 18 volts.
145. RANGE RATE PULSE DRIVER (C10)
PURPOSE:
To generate pulses of the proper amplitude with correct rise and fall times on the RANGE RATE PULSE line upon command of the VELOCITY PULSE line.

OPERATION:
The pulse on the VELOCITY PULSE line triggers the \bar{Q} output of I11, pin 6 to a "0" for 7 usec. This negative pulse on the input to the INTEGRATOR, consisting of I12, C13, R55 and R69, causes a pulse on the RANGE RATE PULSE line which has the proper rise and fall times. The pulse low level is determined by the RANGE RATE LO LEVEL pot, R60, while the high level is determined by the RANGE RATE HI LEVEL pot, R56.

150. TRANSPONDER INTERROGATION INITIATION LOGIC (C8)

PURPOSE:

To cause the TRANSPONDER INTERROGATION to be initiated by the SQUITTER/INTERROGATION TRIGGER and to be synchronous with the 1.45 usec CLOCK and the 1 MHz CLOCK. Also to cause a DOUBLE INTERROGATION to be generated when desired.

OPERATION:

The operation is best understood by referring to the timing diagram shown in figure 5. The right half portion occurs only when a DOUBLE INTERROGATION is present.

The SQUITTER/INTERROGATION TRIGGER causes a pulse on the TRANSPONDER COINCIDENCE PULSE line due to the release on the SET input to I7, pin 4 and coincidence of the 1.45 usec Pulse and the 1 MHz CLOCK edge. The TRANSPONDER COINCIDENCE PULSE allows the TRANSPONDER INTERROGATION INITIATION PULSE line to be triggered low by the 1 MHz CLOCK allowing the TRANSPONDER P1-P3 SPACING GENERATOR to shift thus causing the P1, P2 and P3 TRIGGER pulses and the END TRANSPONDER INTERROGATION pulse to appear which causes the TRANSPONDER INTERROGATION INITIATION PULSE line to go to a "1".

When a DOUBLE INTERROGATION TRIGGER is present the TRANSPONDER COINCIDENCE PULSE is generated immediately and the TRANSPONDER INTERROGATION INITIATION PULSE upon the next 1MHz CLOCK edge.

151. TRANSPONDER P1-P3 SPACING GENERATOR (C8)

PURPOSE:

To generate the P1-P3 pulse spacing necessary for operation in the A, B, C and D modes. Also to cause the interlacing of the A and C, P1-P3 pulse spacing for operation in the A-C mode.

OPERATION:

After the TRANSPONDER INTERROGATION INITIATION PULSE and TRANSPONDER INTERROGATION INITIATION PULSE lines change state the TRANSPONDER P1-P3 SPACING PULSE is generated which causes the P1, P2 and P3 TRIGGER pulses to be generated. The width of the TRANSPONDER P1-P3 SPACING PULSE varies with the mode of operation being 6 usec in A mode, 15 usec in B mode, 19 usec in C mode and 23 usec in the D mode or 2 usec less than the nominal P1-P3 pulse spacing.

Operation in the A-C mode depends on I16 causing 1 out of 4 interrogations to be C mode. In the A-C mode the MR and PE inputs to I16 releases allowing I16, pins 4 and 6 to be clocked by the TRANSPONDER COINCIDENCE PULSE. I16 is programmed for $\div 4$. When the 0000 state is reached the "BUSS"

151. TRANSPONDER P1-P3 SPACING GENERATOR (C8) (Cont'd)
output of I16, pin 12 becomes a "1" which allows the C mode interrogation to occur. The TRANSPONDER INTERROGATION INITIATION PULSE is OR'd with the TRANSPONDER COINCIDENCE PULSE to prevent the "BUSS" from changing state during the generation of the TRANSPONDER P1-P3 SPACING PULSE.
152. TRANSPONDER P2 DEVIATION GENERATOR (C11)
PURPOSE:
To generate a variable delay which determines the TRANSPONDER INTERROGATION P1-P2 pulse spacing.
- OPERATION:
The TRANSPONDER P2 DEVIATION GENERATOR TRIGGER line causes the \bar{Q} output of I7B, pin 8 to be triggered to a "0" causing Q7 to shut off allowing C12 to be charged by current flowing thru R30. When the voltage on I9, pin 3 exceeds that on I9, pin 2 the output of I9, pin 7 goes to a "0" causing the \bar{Q} output of I7B, pin 8 to be reset to a "1". The voltage on I9, pin 2 is controlled by the setting of the TRANSPONDER P2 DEVIATION control.
153. TRANSPONDER P3 DEVIATION GENERATOR (C11)
PURPOSE:
To generate a variable delay which when added to the TRANSPONDER P1-P3 SPACING GENERATOR delay determines the TRANSPONDER INTERROGATION P1-P3 pulse spacing.
- OPERATION:
Very similar to that of the TRANSPONDER P2 DEVIATION GENERATOR.
154. TRANSPONDER PULSE TRIGGER LOGIC (C8)
PURPOSE:
To AND together the P1 TRIGGER, P2 TRIGGER and P3 TRIGGER to form the TRANSPONDER PULSE WIDTH GENERATOR TRIGGER. Also to allow the P2 pulse to be eliminated.
- OPERATION:
Obvious.*
155. TRANSPONDER PULSE WIDTH GENERATOR (C10)
PURPOSE:
To generate a pulse of variable width which determines the width of the TRANSPONDER INTERROGATION RF PULSES. The pulse width is controlled by the TRANSPONDER PULSE WIDTH CONTROL.

*See timing diagrams shown in figures 5 and 6.

155. TRANSPONDER PULSE WIDTH GENERATOR (C10) (Cont'd)

OPERATION:

The TRANSPONDER PULSE WIDTH TRIGGER causes the triggering of O.S. I4A and O.S. I4B. The \bar{Q} output of I3A, is triggered to a "0" which causes C2 to charge until the voltage on I2, pin 3 exceeds that of I2, pin 2 whereupon the output of I2, pin 7 goes to a "0" causing the \bar{Q} output of I3A, pin 13 to be reset to a "1". The voltage on I2, pin 2 is determined by the TRANSPONDER PULSE WIDTH CONTROL.

The purpose of O.S. I4A and O.S. I4B is to cause the \bar{Q} output of I3A, to be reset to "1" when the TRANSPONDER PULSE WIDTH exceeds the TRANSPONDER P1-P2 spacing.*

156. TRANSPONDER PULSE LEVEL LOGIC (C8)

PURPOSE:

To cause the P1, P2 and P3 LEVEL lines and the P1, P2 and P3 COMPARE lines to be at the proper levels to cause the MODULATOR, G18, to form the TRANSPONDER RF PULSES properly.

OPERATION:

Obvious.*

157. DOUBLE INTERROGATION GENERATOR (C11, C8)

PURPOSE:

To cause the test set to DOUBLE INTERROGATE the TRANSPONDER U.T. at a variable time delay after the initial interrogation.

OPERATION:**

The END TRANSPONDER INTERROGATION line triggers the \bar{Q} output of I12B, P8 to a "0" causing C21 to charge. When the voltage on I13, pin 3 exceeds that of I13, pin 2 the output I13, pin 7, goes to a "0" causing the TRANSPONDER INTERROGATION INITIATION LOGIC to initiate a TRANSPONDER INTERROGATION. When the END TRANSPONDER INTERROGATION pulse occurs after the DOUBLE INTERROGATION the \bar{Q} output of I12B, P8 is triggered to a "1".

The pulse which occurs on the DOUBLE INTERROGATION ENABLE line causes proper phasing of the \bar{Q} output of I12B. The "0" which is present when the DOUBLE INTERROGATION ON/OFF control is in the OFF position prevents the triggering of the \bar{Q} output of I12B.

158. TRANSPONDER % RETURN DETECTOR (C8)

PURPOSE:

To generate an output when the TRANSPONDER U.T. replies to a test set interrogation.

* See timing diagram shown in figure 6.

** See timing diagram shown in figure 5.

158. TRANSPONDER & RETURN DETECTOR (C8)

OPERATION:

The TRANSPONDER INTERROGATION RATE line resets the \bar{Q} output of I9, P10 to a "1". If a pulse occurs on the DEMODULATOR 50% LEVEL PULSE line the \bar{Q} output is triggered to a "0".

175. SUPPRESSION PULSE TIMING LOGIC (C7)

PURPOSE:

To generate the proper timing of the SUPPRESSION PULSE DRIVER PULSE line to cause the SUPPRESSION PULSE to be synchronous with the DME REPLY PULSES or the TRANSPONDER INTERROGATION PULSES.

OPERATION:

In the DME mode the \bar{Q} output of I9B, P15 is triggered to a "0" by the REPLY TRIGGER line. The \bar{Q} output of O.S. I8A, P7 is also triggered to a "0" which prevents O.S. I8B, pin 10 from being triggered by the DME PULSE WIDTH CONTROL line during the P1 pulse. When the P2 pulse is generated on the DME PULSE WIDTH CONTROL line the Q output of O.S. I8, P10 is triggered to a "1". When it returns to a "0" after 12 μ sec the negative pulse generated at I9B, pin 2 causes the \bar{Q} output of I9B, P15 to be reset to a "1" thus ending the negative pulse on the SUPPRESSION PULSE DRIVER PULSE line.

In the TRANSPONDER mode the TRANSPONDER COINCIDENCE $\overline{\text{PULSE}}$ line triggers the \bar{Q} output of I9A, P10 to a "0". When the pulse on the P3 LEVEL line returns to "0" the \bar{Q} output is reset to a "1". Thus a negative pulse is generated on the SUPPRESSION PULSE DRIVER PULSE line.

176. SCOPE SYNC LOGIC (C7, C8, C11)

PURPOSE:

To generate a negative pulse on the SCOPE SYNC OUTPUT which is synchronous with that pulse as selected by the SYNC OUTPUT switch and the MODE SELECT control.

OPERATION:

The table below shows the various sync parameters vs the SYNC OUTPUT switch and the MODE SELECT control.

SYNC OUTPUT SWITCH	DME MODE	TRANSPONDER MODE
TO	DME U.T. SUPPRESSION PULSE OR INTERRO PULSE	INTERRO P1
SQUITTER	SQUITTER, IDENT OR REPLY	INTERRO P1
TD	REPLY	INTERRO P3

178. CALIBRATION PULSE 1/1.45 usec SWITCH (C8)

PURPOSE:

To cause the CALIBRATION OUTPUT to have 1 usec or 1.45 usec pulses as selected by the CALIBRATE 1 usec/1.45 usec switch.

OPERATION:

Obvious.

179. CALIBRATION PULSE PHASE GENERATOR (C7)

PURPOSE:

To cause the phase of the pulses at the CALIBRATION OUTPUT to vary in phase in accordance with the CALIBRATION PHASE CONTROL.

OPERATION:

As the CALIBRATION PHASE control is varied the pulse width on the \bar{Q} output of I5A, P7 varies thus generating a variable delay or phase.

CALIBRATIONS

1. SQUITTER/INTERROGATION RATE GENERATOR CALIBRATION (C7) (C9)

1. By means of selection of resistor R33, position 24-1/16 adjust the pulse on the \bar{Q} output of I23, P7 for a duration of 60 ± 5 usec.
2. By means of selection of resistor R32, position 24-3/14 adjust the pulse on the \bar{Q} output of I23, P9 for a duration of 600 ± 50 usec.
3. By means of the SQUITTER/INTERRO MAX RATE pot, R51 on card 9, adjust the squitter rate to 9500 ± 250 PPS with the SQUITTER/INTERROGATION RATE control full CW and the HI range selected.

2. POWER MEAS. TIMING GENERATOR CALIBRATION (C11)

1. By means of selection of resistor, R15, adjust the pulse on the Q output of I5A, P6, for a duration of 3.5 ± 1 msec.
2. By means of selection of resistor, R16, adjust the pulse on the Q output of I5B, P10, for a duration of 35 ± 10 usec.
3. By means of selection of resistor, R17, adjust the pulse on the Q output of I6, P8, for a duration of 35 ± 10 usec.

3. POWER MEAS. ΔT GENERATOR CALIBRATION (C11)

1. a. Place 3.16 volts on the PULSE PEAK LEVEL line by means of a power supply or some other voltage source.
b. By means of the POWER LINEARITY HI pot, R3, adjust the readout for 2000 ± 5 watts.
2. a. Place 0.316 volts on the PULSE PEAK LEVEL line.
b. By means of the POWER LINEARITY LO pot, R5, adjust the readout for 20 watts.
3. Repeat steps 1 and 2 as there is interaction.
4. With 1.00 volts on the PULSE PEAK LEVEL line the readout should indicate 200 ± 1 watts.

4. SUPPRESSION PULSE TIMING LOGIC CALIBRATION (C7)

1. By means of selection of resistor R12 position 7-2/15 adjust the pulse on the \bar{Q} output of I8, P7 for a duration of 6.5 ± 1.0 usec.
2. By means of selection of resistor R7 position 7-4/13 adjust the pulse on the Q output of I8, P10 for a duration of 11.5 ± 1.0 usec.

5. SUPPRESSION PULSE DRIVER CALIBRATION (C9)

1. By means of the SUPPRESSION PULSE LEVEL pot, R33, adjust the pulse level on the SUPPRESSION PULSE line to 18.5 ± 0.2 volts.

6. CALIBRATION PULSE PHASE GENERATOR CALIBRATION (C7)

1. By means of selection of R38 position 6-5/12 adjust the positive pulse on the Q output of I5, P10 for a duration of 0.725 ± 0.025 usec.
2. a. Select the TRANSPONDER mode and 1.45 usec calibration pulses.

b. By means of selection of resistor R36 position 6-3/14 adjust the pulse width on the \bar{Q} output of I5, P7 so as the CALIBRATION PHASE control is fully rotated the phase of the pulses at the CAL OUTPUT vary so that any point may be overlaid by either a rising or falling edge.

NOTE: Sync scope to SCOPE SYNC OUTPUT with the SYNC OUTPUT switch in any position to determine phase variation of 1.45 usec calibration pulses.

7. SCOPE SYNC LOGIC CALIBRATION (C7)

1. By means of selection of resistor R6 position 24-6/11 adjust the pulse on the \bar{Q} output of I25, P9 for a duration of 31 ± 3 usec.

8. INITIAL DELAY O.S. (C7)

1. a. Short the base of Q2 position 28-6/7/10 to ground.

b. By means of selection of resistor R19 position 30-7/10 adjust the pulse on the Q output of I27, P6 for a duration of 750 ± 50 nsec.
2. a. Short the collector of Q2 position 28-6/7/10 to ground.

b. By means of selection of resistor R18 position 28-3/14 adjust the pulse on the Q output of I27, P6 for a duration of 225 ± 50 nsec.

9. ECHO LEVEL LOGIC CALIBRATION (C7)

1. By means of selection of resistor R28 position 30-3/14 adjust the pulse on the \bar{Q} output of I20, P9 for a duration of 6 ± 0.5 usec.
2. By means of selection of resistor R27 position 30-1/16 adjust the pulse on the \bar{Q} output of I20, P6 for a duration of 6 ± 0.5 usec.

10. DME PULSE WIDTH GENERATOR CALIBRATION (C7)

1. By means of the DME PULSE WIDTH CAL pot, R26-3/6/8, adjust the pulse on the \bar{Q} output of I27, P9 for a duration of 3.5 ± 0.1 usec.

11. PEDESTAL TIMING GENERATOR CALIBRATION (C3)

1. By means of selection of resistor R11 position 30-3/14 adjust the pulse on the \bar{Q} output of I20, P6 for a duration of 0.5 ± 0.025 usec.
2. By means of selection of resistor R12 position 30-1/16 adjust the pulse on the \bar{Q} output of I20, P9 for a duration of 7 ± 0.25 usec.

12. DME P2 DEVIATION GENERATOR CALIBRATION (C10)

1. a. Place the DME P2 DEVIATION control in the +5 usec position. Select X-Mode pulse spacing.
b. By means of the DME P2 DEVIATION CALIBRATION pot, R42, adjust the DME P1-P2 RF pulse spacing as observed at the VIDEO OUTPUT MONITOR, for a spacing of 17 ± 0.3 usec.
2. a. Place the DME P2 DEVIATION control in the -5 usec position.
b. By means of the DME P2 DEVIATION LINEARITY pot, R41, adjust the DME P1-P2 RF pulse spacing for a spacing of 7 ± 0.3 usec.
3. Repeat steps 1 and 2 as there is interaction.

NOTE: Use 0.5 amplitude point of the rising edges of the RF pulses to determine the spacing.

13. X-Y PULSE SPACING LOGIC CALIBRATION (C7)

1. DME P2 DEVIATION GENERATOR calibration must be performed prior to this calibration.
2. Place the DME P2 DEVIATION control in the 0 usec position. Select Y-Mode pulse spacing.
3. By means of the Y-Mode P1-P2 SPACING pot, R34 position 26-9/11/14 adjust the RF P1-P2 pulse spacing as observed at the VIDEO OUTPUT MONITOR for a spacing of 30 ± 0.1 usec.

NOTE: Use the 0.5 amplitude points of the rising edges of the RF pulses to determine the P1-P2 spacing.

14. ECHO DISTANCE DELAY GENERATOR CALIBRATION (C6)

1. X-Mode
 - a. By means of the X-MODE ECHO P1-P2 SPACING pot R10 position 24-3/6/8 adjust the pulse on the Q output of I25, pin 10 for a duration of 12 ± 0.1 usec.
 - b. By means of the X-MODE ECHO DISTANCE pot R9 position 24-9/11/14 adjust the pulse on the \bar{Q} output of I25, pin 7 for a duration of 415 usec.
2. Y-Mode
 - a. By means of the Y-MODE ECHO P1-P2 SPACING pot R7 position 23-3/6/8 adjust the pulse on the Q output of I22, pin 10 for a duration of 30 ± 0.1 usec.
 - b. By means of the Y-MODE ECHO DISTANCE pot, R6 position 23-9/11/14 adjust the pulse on the \bar{Q} output of I22, P7 for a duration of 421 usec.

NOTE: To accurately set a 30 NMi echo distance it is necessary to cause a DME to lock on to the echo and readout this distance.

15. TACAN MODULATION GENERATOR CALIBRATION (C9)

1. 15 Hz Calibration
 - a. Reduce the 135 Hz component by means of the 135 Hz LEVEL pot, R61.
 - b. Adjust the 15 Hz amplitude modulation component on the RF pulses as observed at the VIDEO OUTPUT MONITOR for a modulation percentage of 20 ± 5 percent by means of the 15 Hz LEVEL pot, R55.

15. TACAN MODULATION GENERATOR CALIBRATION (C9) (Cont'd)

2. 135 Hz Calibration

- a. Adjust the 135 Hz amplitude modulation component on the RF pulses as observed at the VIDEO OUTPUT MONITOR for a modulation percentage of 20 ± 5 percent by means of the 135 Hz LEVEL pot, R61.

16. IDENT CODE/TONE GENERATOR CALIBRATION (C8)

1. By means of selection of resistor R22 position 26-8/9 adjust the pulse on the Q output of I24, pin 9 for a duration of 5 ± 0.5 sec.

17. EQUALIZATION PULSE GENERATOR CALIBRATION (C8)

1. By means of selection of resistor R17 position 28-5/12, adjust the pulse on the Q output of I29, pin 6 for a duration of 100 ± 10 usec.

18. DME INTERROGATION RATE O.S. CALIBRATION (C8)

1. By means of selection of resistor R21 position 9-8/9 adjust the pulse on the Q output of I24, pin 6 for a duration of at least 50 usec.

19. TRANSPONDER INTERROGATION INITIATION CALIBRATION (C8)

1. By means of selection of resistor R2 position 15-8/9 adjust the pulse on the input to NAND gate I2, pin 15 for a duration of 60 ± 10 nsec.

20. TRANSPONDER PULSE LEVEL LOGIC CALIBRATION (C8)

1. By means of selection of resistor R7 position 28-8/9 adjust the pulse on the Q output of I29, pin 10 for a duration of 2.0 ± 0.1 usec.

21. TRANSPONDER PULSE WIDTH GENERATOR CALIBRATION (C10)

1. a. Place the XPDR PULSE WIDTH control in the 1.4 usec position.

b. By means of the XPDR PULSE WIDTH CAL. pot, R5, adjust the width of the TRANSPONDER RF pulses as observed at the VIDEO OUTPUT MONITOR for a duration of 1.4 ± 0.05 usec.

21. TRANSPONDER PULSE WIDTH GENERATOR CALIBRATION (C10) (Cont'd)

2. a. Place the XPDR PULSE WIDTH control in the 0.4 usec position.
 - b. By means of the XPDR PULSE WIDTH LINEARITY pot, R2, adjust the duration of the TRANSPONDER RF pulses for a duration of 0.4 ± 0.05 usec.
3. Repeat steps 1 and 2 as there is interaction.

NOTE: Use 0.5 amplitude points to determine the RF pulse duration of the leading and falling edges.

22. XPDR P2 DEVIATION GEN CALIBRATION (C11)

1. a. Place the XPDR P2 DEVIATION control in the +1.0 usec position.
 - b. By means of the XPDR P2 DEVIATION CAL pot, R29, adjust the TRANSPONDER P1-P2 RF pulse spacing as observed at the VIDEO OUTPUT MONITOR for a spacing of 3.0 ± 0.05 usec.
2. a. Place the XPDR P2 DEVIATION control in the -1.0 usec position.
 - b. By means of the XPDR P2 DEVIATION LINEARITY pot, R59, adjust the XPDR P1-P2 RF pulse spacing for a spacing of 1.0 ± 0.05 usec.
3. Repeat steps 1 and 2 as there is interaction.

NOTE: Use the 0.5 amplitude point of the rising edge of the RF pulse to determine the P1-P2 spacing.

23. TRANSPONDER P3 DEVIATION GENERATOR CALIBRATION (C11)

1. a. Place the XPDR P3 DEVIATION control in the +1.0 usec position. Select XPDR mode A.
 - b. By means of the XPDR P3 DEVIATION CAL pot, R41, adjust the XPDR P1-P3 RF pulse spacing as observed at the VIDEO OUTPUT MONITOR for a spacing of 9.0 ± 0.05 usec.
2. a. Place the XPDR P3 DEVIATION control in the -1.0 usec position.
 - b. By means of the XPDR P3 DEVIATION LINEARITY pot, R37, adjust the XPDR P1-P3 RF pulse spacing for a spacing of 7.0 ± 0.05 usec.

23. TRANSPONDER P3 DEVIATION GENERATOR CALIBRATION (C11) (Cont'd)

3. Repeat steps 1 and 2 as there is interaction.

NOTE: Use the 0.5 amplitude point of the rising edge of the RF pulse to determine the P1-P3 spacing.

24. TRANSPONDER DOUBLE INTERROGATION GENERATOR CALIBRATION (C11)

1. a. Place the TRANSPONDER DOUBLE INTERROGATION control in the full CW position.

b. By means of the TRANSPONDER DOUBLE INTERROGATION RANGE HI pot, R52, adjust the spacing between the INITIAL INTERROGATION P3 RF pulse and the DOUBLE INTERROGATION P1 RF pulse as observed at the VIDEO OUTPUT MONITOR for a spacing of 260 ± 10 usec.
2. a. Place the TRANSPONDER DOUBLE INTERROGATION control in the full CCW position.

b. By means of selection of resistor, R51, adjust the spacing between the RF pulses for a spacing of 35 ± 5 usec.
3. Repeat steps 1 and 2 as there is interaction.

NOTE: Use the 0.5 amplitude points of the rising edges of the RF pulses to determine the spacing.

25. DME U.T. DATA RATE MONITOR CALIBRATION (C4)

1. By means of selection of resistor R3 position 26-8/9, adjust the pulse on the Q output of I27, pin 10 for a duration of 190 ± 10 msec.

26. DME U.T. FLAG ALARM RECEIVER CALIBRATION (C9)

1. By means of the FLAG LEVEL pot, R28, cause the ALARM line (collector of Q6) to go to a "0" when the DME U.T. FLAG ALARM line goes through 1.0 volt.

27. ANALOG DISTANCE PULSE TRIGGER GENERATOR CALIBRATION (C9)

1. By means of selection of resistor R26 adjust the pulse spacing within the range of 66 to 100 msec (10 to 14 Hz).

28. ANALOG DISTANCE PULSE LOGIC CALIBRATION (C6)

1. By means of section of resistor R4 position 4-8/9, adjust the pulse on the \bar{Q} output of I4, pin 6 for a duration of 7 ± 1 usec.

29. ANALOG DISTANCE PULSE DRIVER CALIBRATION (C10)

1. By means of the ANALOG DISTANCE PULSE LO LEVEL pot, R36, adjust the low level of the pulse on the ANALOG DISTANCE PULSE line for a level of 3.0 ± 0.2 volts.
2. By means of the ANALOG DISTANCE PULSE HI LEVEL pot, R32, adjust the high level of the pulse for a level of 7.0 ± 0.2 volts.

30. INDICATOR U.T. WARNING FLAG DRIVER CALIBRATION (C11)

1. a. Place the SERIAL DATA OUTPUT control in the OFF position.
b. By means of the WARNING FLAG LEVEL pot, R21, adjust the voltage level on the INDICATOR U.T. WARNING FLAG line for a level of 18.5 ± 0.2 volts.
2. a. Place the SERIAL DATA OUTPUT control in the FLAG position.
b. By means of selection of resistor, R20, adjust the voltage level on the INDICATOR U.T. WARNING FLAG line for 1 ± 0.25 volts.

31. INDICATOR U.T. MINIMUM DATA RATE GENERATOR CALIBRATION (C9)

1. By means of selection of resistor R79, adjust the pulse spacing to within the range of 190 ± 10 msec. (5Hz).

32. INDICATOR U.T. SERIAL BCD CLOCK OSCILLATOR CALIBRATION (C9)

1. a. Set the SERIAL DATA CLOCK control to 15 KHz.
b. By means of the CLOCK HI LIMIT pot, R85, adjust the PRF on the 14-30 KHz CLOCK line to within 30 ± 2 KHz.
2. a. Set the SERIAL DATA CLOCK control to 7 KHz.
b. By means of the CLOCK LO LIMIT pot, R84, adjust the PRF on the 14-30 KHz CLOCK line to within 14 ± 2 KHz.
3. Repeat steps 1 and 2 as there is interaction between them.
4. When Calibration is completed the PRF on the 14-30 KHz Clock line should be 22 ± 1 KHz with the Serial Data Clock control set for 11 KHz.

33. INDICATOR U.T. SERIAL BCD CLOCK DRIVER CALIBRATION (C10)

1. By means of the CLOCK LO pot, R22, adjust the low level of the pulse on the INDICATOR U.T. SERIAL BCD CLOCK line for a level of 3.0 ± 0.2 volts.
2. By means of the CLOCK HI pot, R18, adjust the high level of the pulse for a level of 7.0 ± 0.2 volts.

34. INDICATOR U.T. SERIAL BCD WORD SYNC DRIVER CALIBRATION (C10)

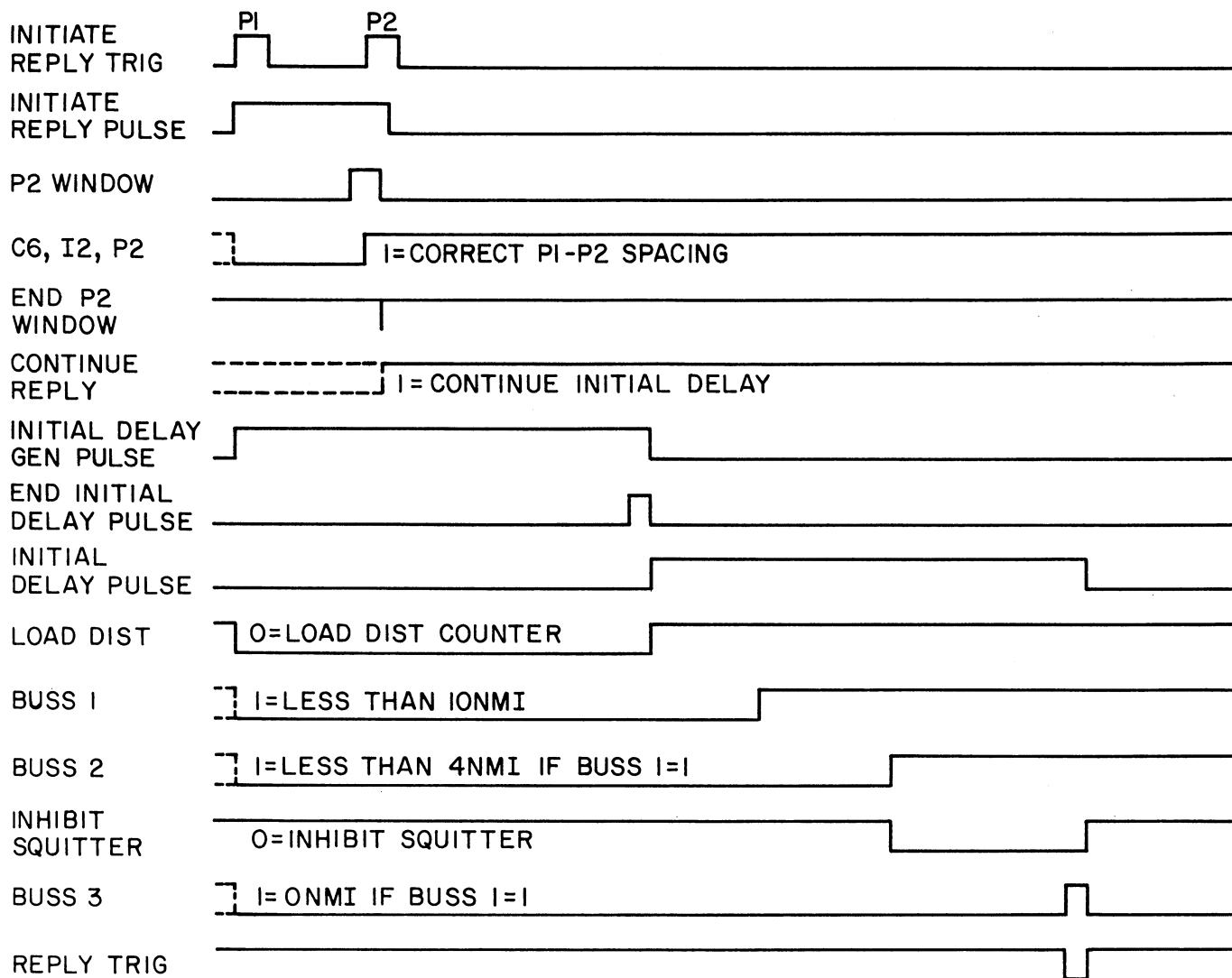
1. By means of the SYNC LO pot, R50, adjust the low level of the pulse on the INDICATOR U.T. SERIAL BCD WORD SYNC line for a level of 3.0 ± 0.2 volts.
2. By means of the SYNC HI pot, R46, adjust the high level of the pulse for a level of 7.0 ± 0.2 volts.

35. INDICATOR U.T. SERIAL BCD DISTANCE DATA DRIVER CALIBRATION (C10)

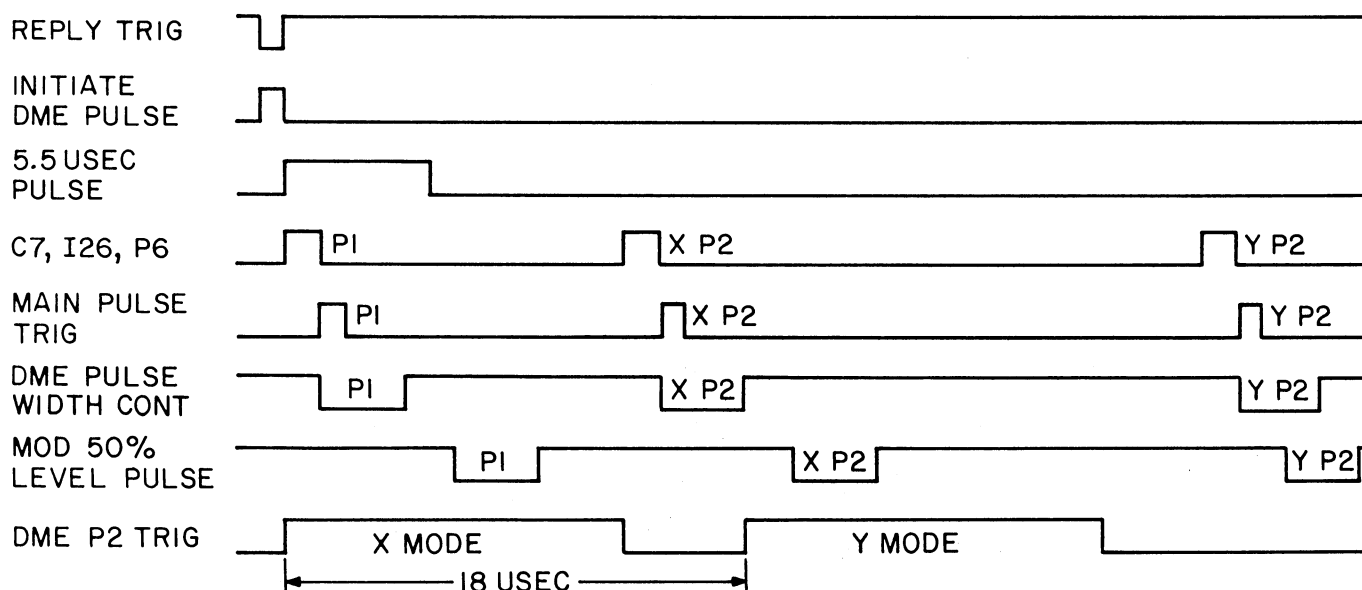
1. By means of the DISTANCE DATA LO pot, R29, adjust the low level of the pulse on the SERIAL BCD DISTANCE DATA line for a level of 3.0 ± 0.2 volts.
2. By means of the DISTANCE DATA HI pot, R25, adjust the high level of the pulse for a level of 7.0 ± 0.2 volts.

36. RANGE RATE PULSE DRIVER CALIBRATION (C10)

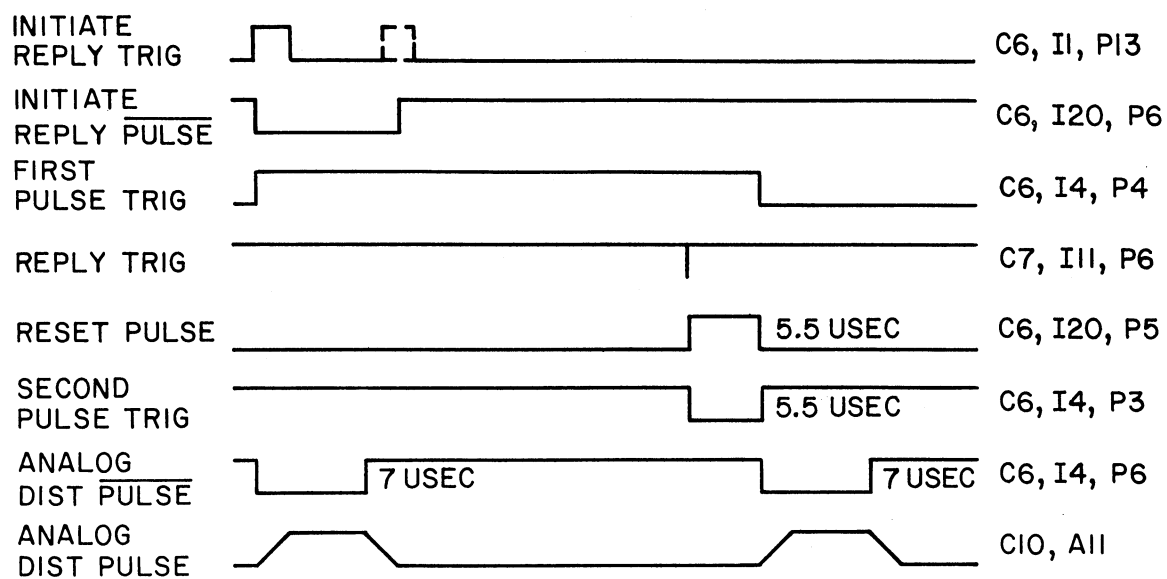
1. By means of selection of R53 adjust the pulse on I11, P6 for a duration of 7 ± 1 usec.
2. By means of the RANGE RATE PULSE LO pot, R60, adjust the low level of the pulse on the RANGE RATE pulse line for a level of 3.0 ± 0.2 volts.
3. By means of the RANGE RATE PULSE HI pot, R56, adjust the high level of the pulse for a level of 7.0 ± 0.2 volts.



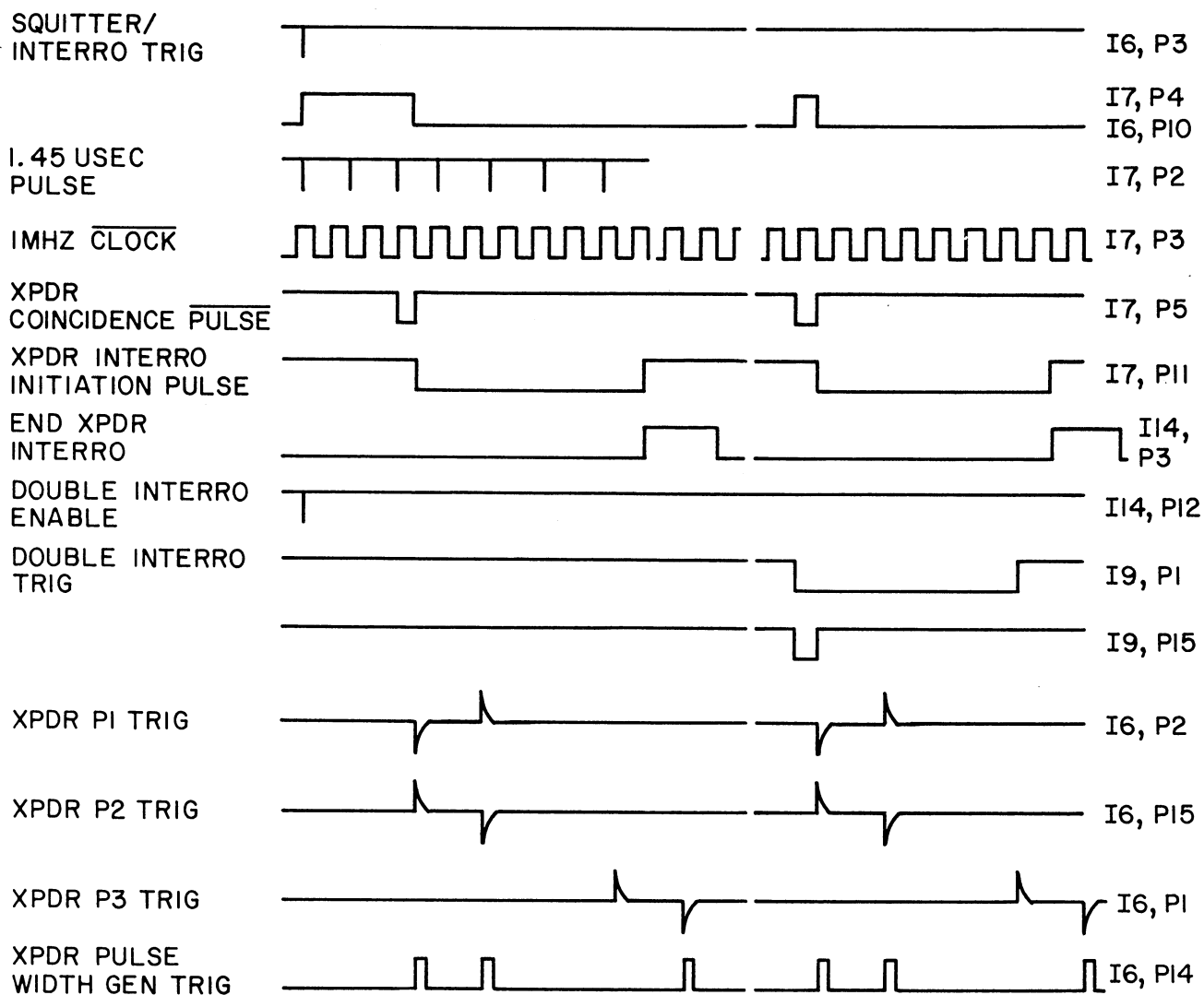
TIMING DIAGRAM FOR INTERRO P1-P2 SPACING,
INITIAL DELAY AND DISTANCE DELAY LOGIC
FIG 1



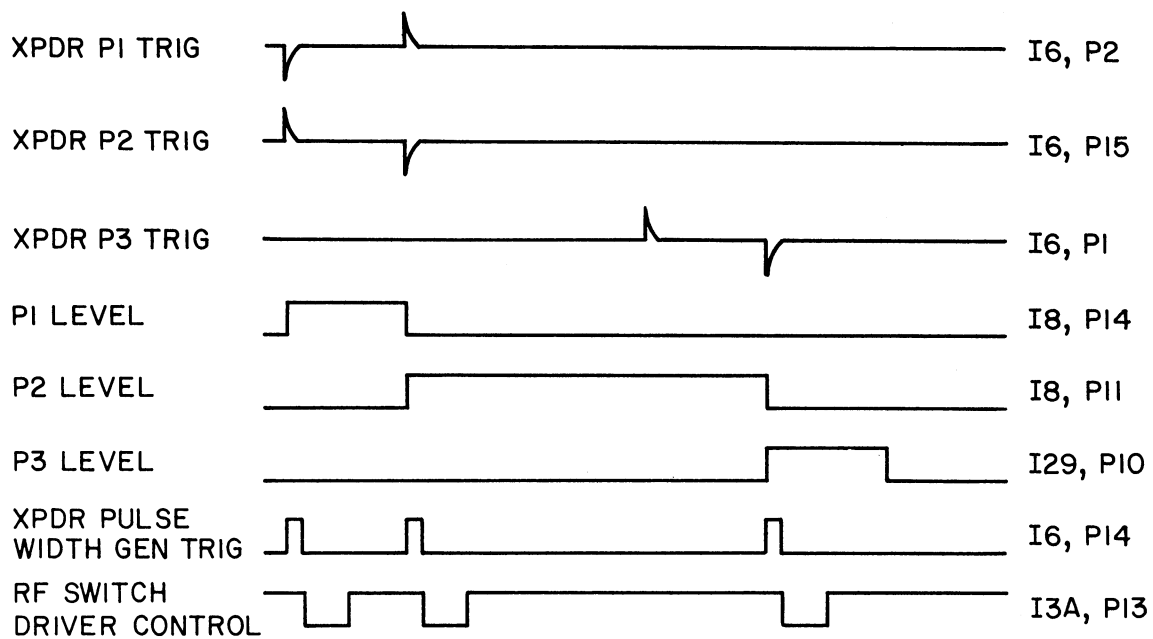
TIMING DIAGRAM
FIG. 2



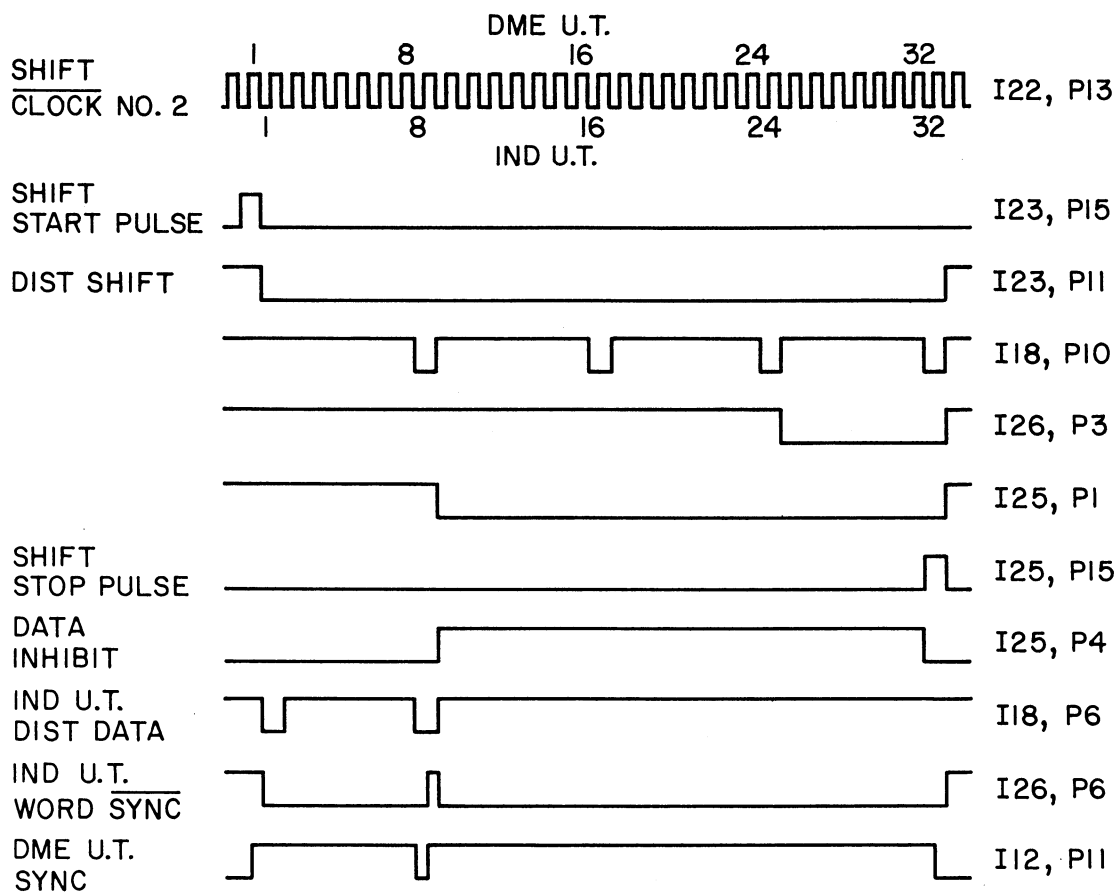
ANALOG DISTANCE PULSE LOGIC
TIMING DIAGRAM
FIG 3



TIMING DIAGRAM FOR XPDR INTERRO INITIATION
LOGIC AND XPDR PULSE TRIGGER LOGIC
FIG 5



TIMING DIAGRAM FOR XPDR PULSE TRIG LOGIC,
XPDR PULSE LEVEL LOGIC AND XPDR PULSE WIDTH GEN
FIG 6

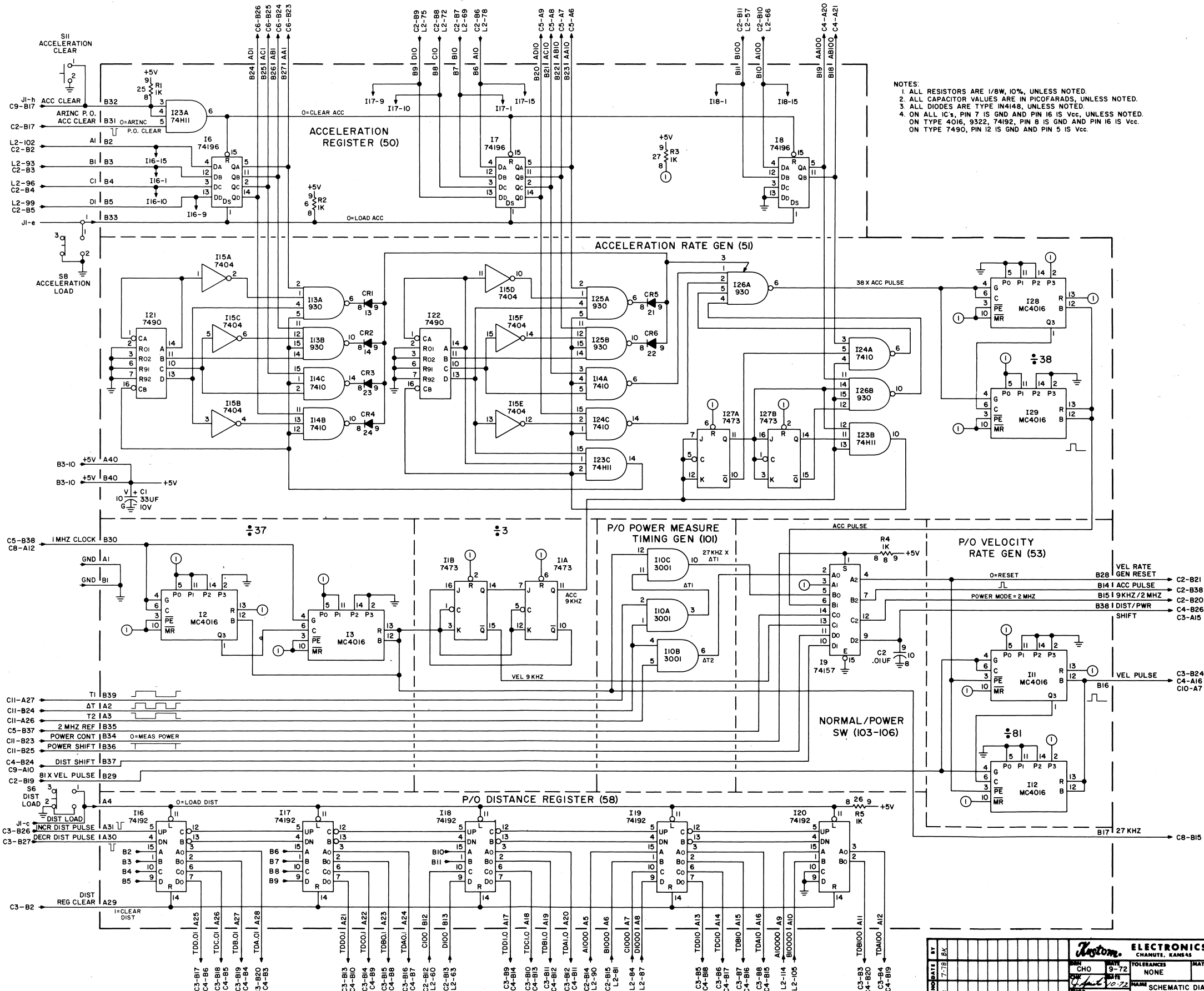


TIMING DIAGRAM FOR
WORD SYNCHRONIZATION LOGIC
FIG 7

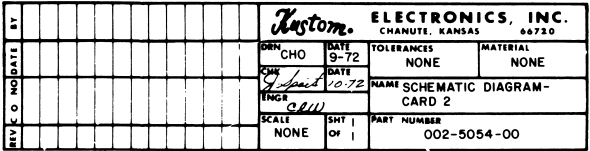
MODE	PS- 1 I5, P5	PS- 2 I5, P11	PS- 4 I5, P14	PS- 8 I5, P2	PS- 10 I6, P5	PS- 20 I6, P11	PS- 40 I6, P14	PS- 80 I6, P2	PS- 100 I7, P5	PS- 200 I7, P11	PS- 400 I7, P14	PS- 800 I7, P2
% RETURN	1	0	0	0	0	0	0	0	1	0	0	0
SQUITTER RATE DME INTERRO RATE	1	*	*	1	1	0	0	1	1	0	0	1
ΔF	*	*	*	*	*	*	*	*	*	*	*	*

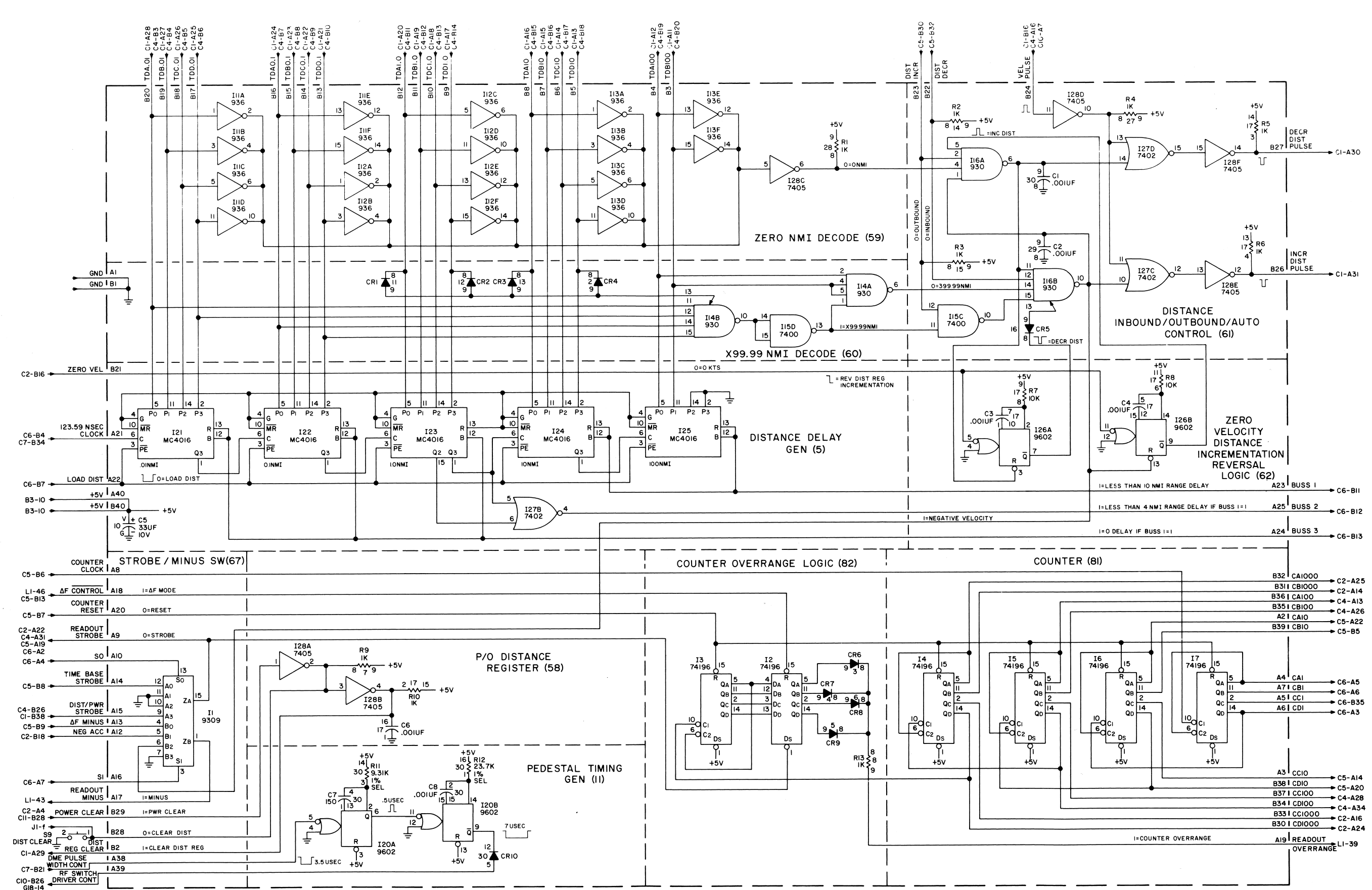
* = Depends on N value determined by Freq. Control Logic, L3

TIME BASE COUNTER PROGRAM vs. MODE
FIG 8



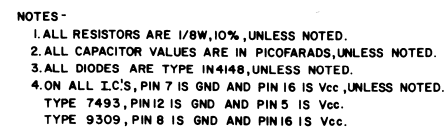
ELECTRONICS, INC.			
CHANUTE, KANSAS 66720			
BY	DATE	REV	CHK
1	7-78	8K	
TOLERANCES		MATERIAL	
9-72		NONE	
NAME		SCHEMATIC DIAGRAM -	
SCALE		CARD 1	
PART NUMBER		002-5053-00	

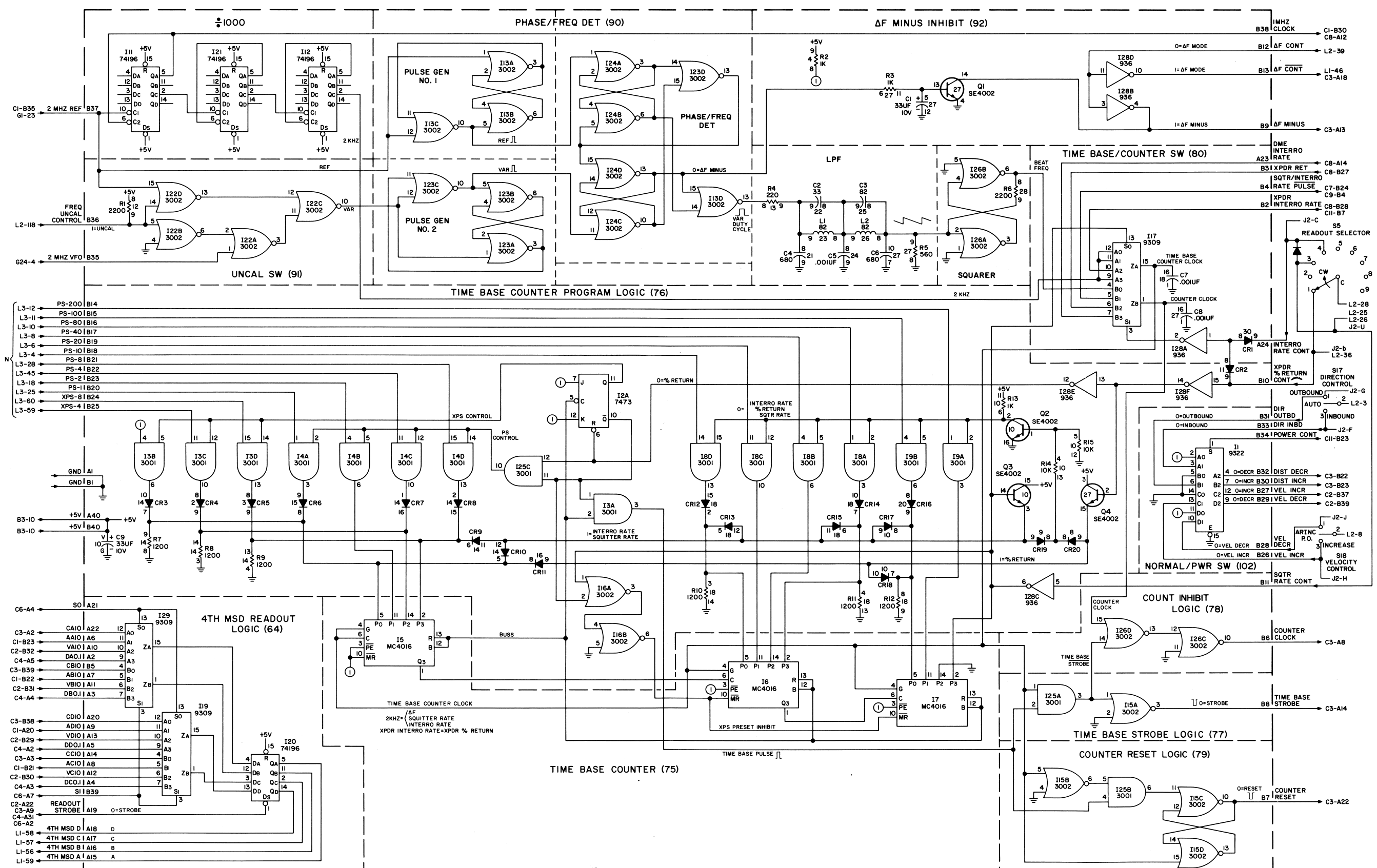




- NOTES:
1. ALL RESISTORS ARE 1/8W, 10%, UNLESS NOTED.
 2. ALL CAPACITOR VALUES ARE IN PICOFARADS, UNLESS NOTED.
 3. ALL DIODES ARE TYPE 1N4148, UNLESS NOTED.
 4. ON ALL IC's, PIN 7 IS GND AND PIN 16 IS Vcc.

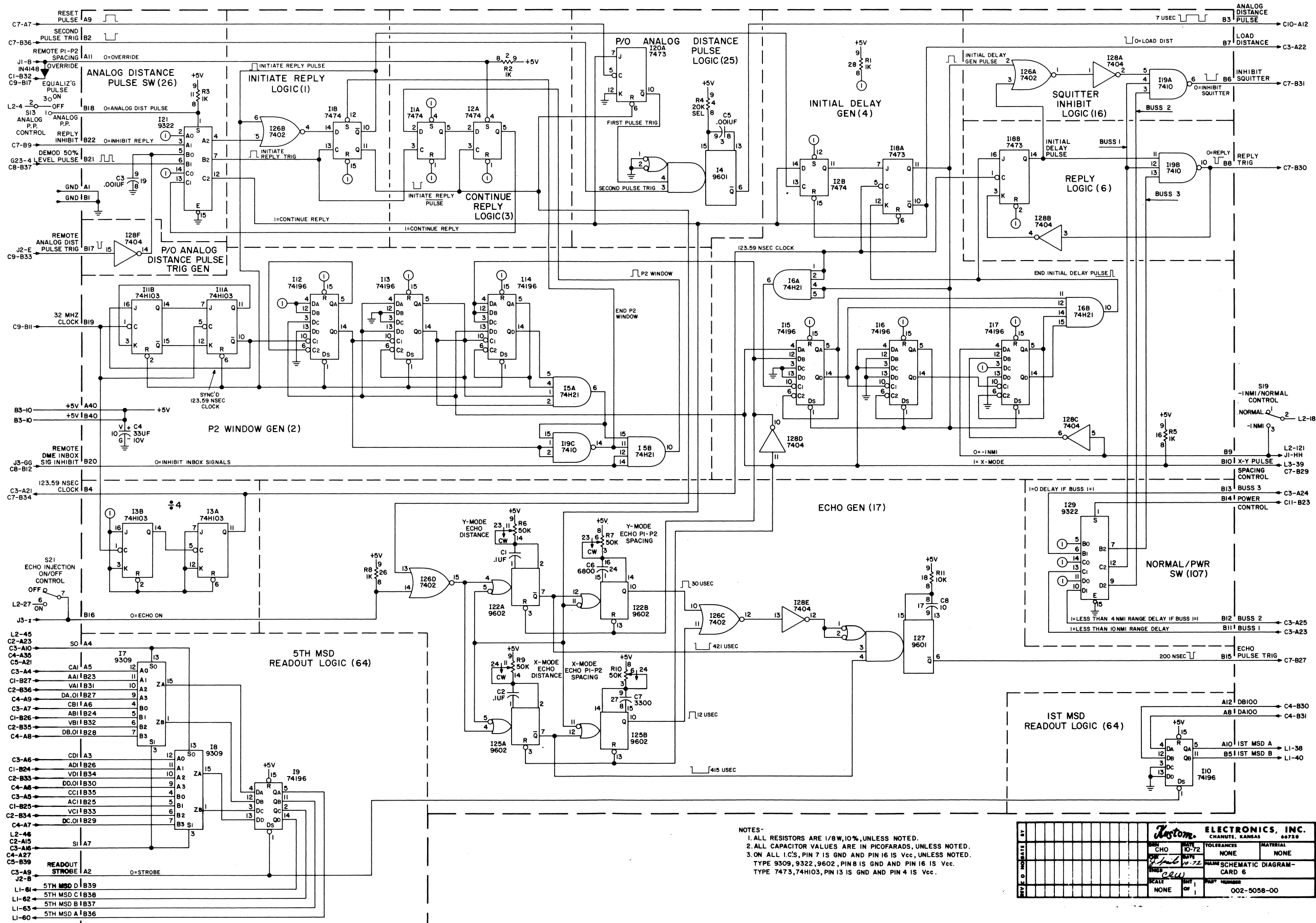
BY		DATE		REV		Kustom ELECTRONICS, INC. CHANUTE, KANSAS 66720	
DRN	CHO	DATE	9-72	TOLERANCES	NONE	MATERIAL	NONE
CHK	DATE	10-72	NAME	SCHEMATIC DIAGRAM - CARD 3			
ENG	SCALE	SHT	1	PART NUMBER	002-5055-00		





NOTES:
1. ALL RESISTORS ARE 1/8W, 10%, UNLESS NOTED.
2. ALL CAPACITOR VALUES ARE IN PICOFARADS, UNLESS NOTED.
3. ALL INDUCTOR VALUES ARE IN MICROHENRYS, UNLESS NOTED.
4. ALL DIODES ARE TYPE 1N4148, UNLESS NOTED.
5. ON ALL IC's, PIN 7 IS GND AND PIN 16 IS Vcc, UNLESS NOTED.
ON TYPE 9309, 9322, 4016, PIN 8 IS GND AND PIN 16 IS Vcc.
ON TYPE 7473, PIN 13 IS GND AND PIN 4 IS Vcc.

ELECTRONICS, INC.	
CHAMUTE, KANSAS 66720	
DATE: 9-72	TOLERANCES: NONE
BY: [Signature]	MATERIAL: NONE
CHK: [Signature]	NAME: SCHEMATIC DIAGRAM - CARD 5
SCALE: NONE	PART NUMBER: 002-5057-00



NOTES-

1. ALL RESISTORS ARE 1/8W, 10%, UNLESS NOTED.

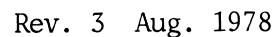
2. ALL CAPACITOR VALUES ARE IN PICOFARADS, UNLESS NOTED.

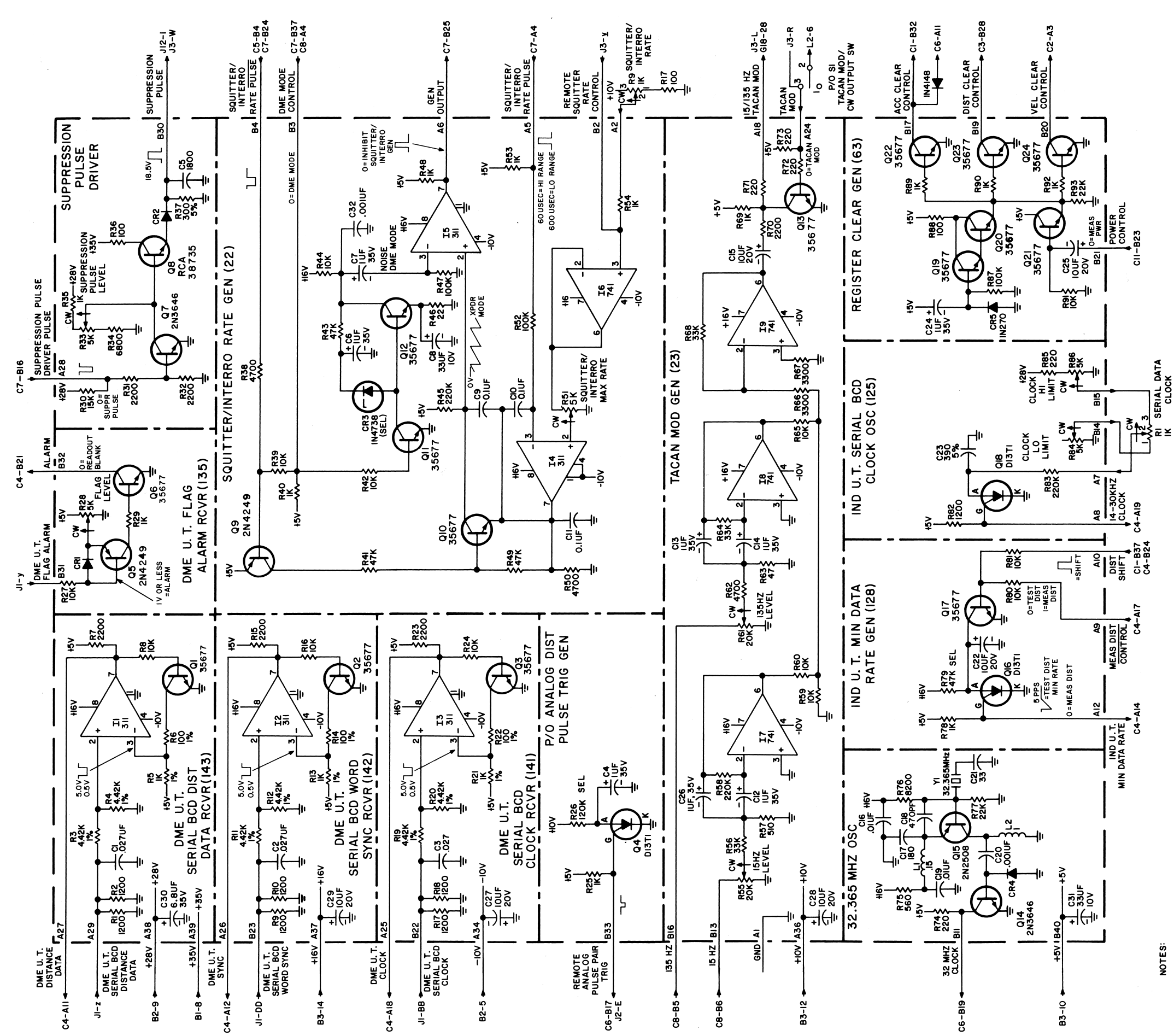
3. ON ALL I.C'S, PIN 7 IS GND AND PIN 16 IS Vcc, UNLESS NOTED.

TYPE 9309, 9322, 9602, PIN 8 IS GND AND PIN 16 IS Vcc.

TYPE 7473, 74H103, PIN 13 IS GND AND PIN 4 IS Vcc.

ELECTRONICS, INC.		CHAMUTE, KANSAS 66720	
DATE	10-72	TOLERANCES	NONE
BY	10-72	MATERIAL	NONE
SCALE	1:1	NAME	SCHEMATIC DIAGRAM - CARD 6
PART NUMBER	002-5058-00		





Rev. 3									
REV	DATE	BY	CHKD	APPD	TEST	SCALE	SWT	OP	PART NUMBER
1	7/81	JTS	2-72	10-12	10-12	10-12	10-12	10-12	002-5061-00
2	8-71	7-18	7-18	7-18	7-18	7-18	7-18	7-18	002-5061-00
3	8-71	7-18	7-18	7-18	7-18	7-18	7-18	7-18	002-5061-00
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86	8-71	7-18	7-18	7-18	7-18	7-18	7-18	7-18	002-5061-00
87	8-71	7-18	7-18	7-18	7-18	7-18	7-18	7-18	002-5061-00
88	8-71	7-18	7-18	7-18	7-18	7-18	7-18	7-18	002-5061-00
89	8-71	7-18	7-18	7-18	7-18	7-18	7-18	7-18	002-5061-00
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91	8-71	7-18	7-18	7-18	7-18	7-18	7-18	7-18	002-5061-00
92	8-71	7-18	7-18	7-18	7-18	7-18	7-18	7-18	002-5061-00
93	8-71	7-18	7-18	7-18	7-18	7-18	7-18	7-18	002-5061-00
94	8-71	7-18	7-18	7-18	7-18	7-18	7-18	7-18	002-5061-00
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97	8-71	7-18	7-18	7-18	7-18	7-18	7-18	7-18	002-5061-00
98	8-71	7-18	7-18	7-18	7-18	7-18	7-18	7-18	002-5061-00
99	8-71	7-18	7-18	7-18	7-18	7-18	7-18	7-18	002-5061-00
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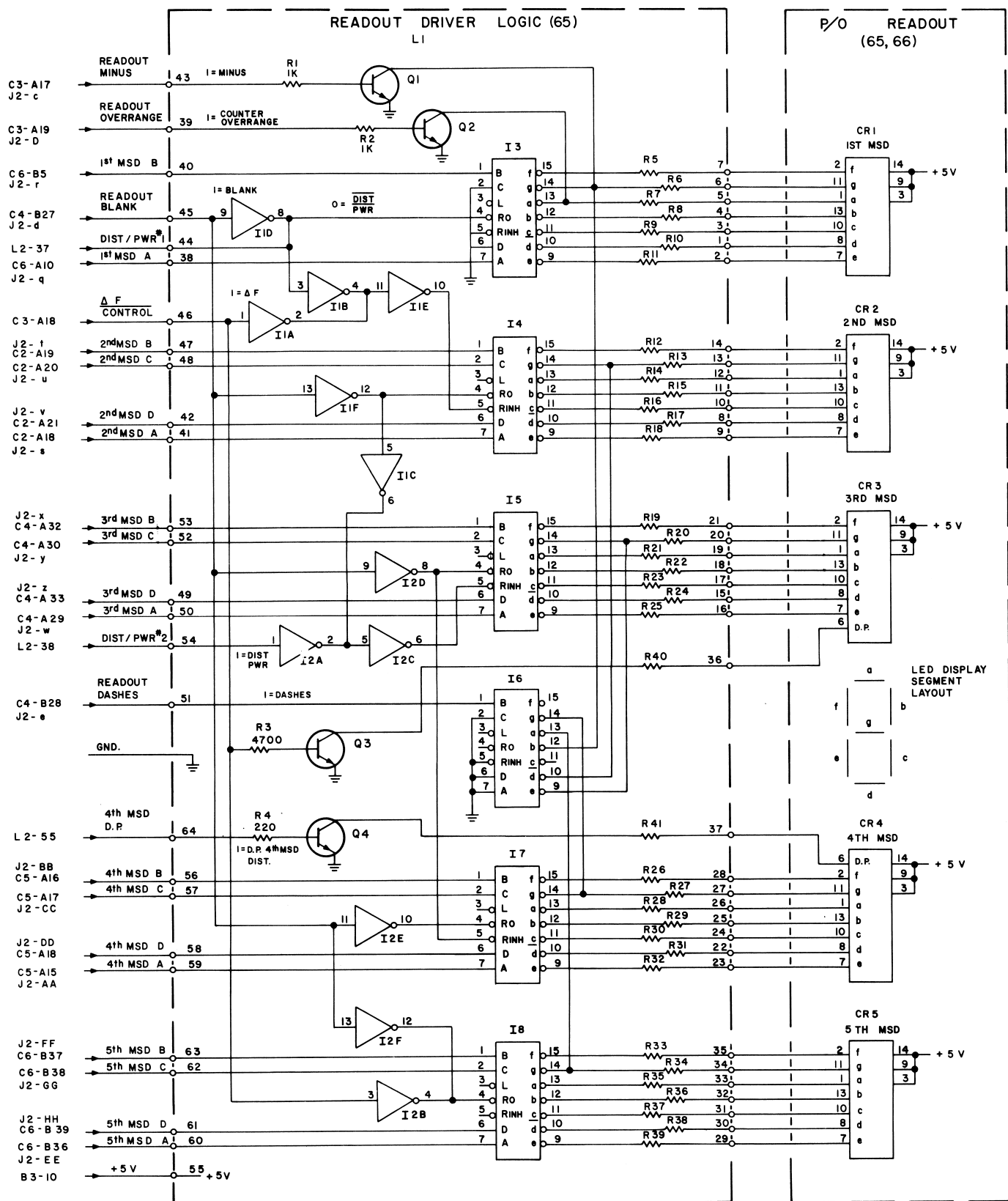
- NOTES:
1. ALL CAPACITOR VALUES ARE IN PICOFARADS, UNLESS NOTED.
 2. ALL RESISTORS ARE 1/4W, 10%, UNLESS NOTED.
 3. ALL INDUCTOR VALUES ARE IN MICROHENRYS, UNLESS NOTED.
 4. ALL DIODES ARE TYPE IN4148, UNLESS NOTED.

1. ALL RESISTORS ARE 1/4W, 10%, UNLESS NOTED.
2. ALL CAPACITOR VALUES ARE IN PICOFARADS, UNLESS NOTED.
3. ALL DIODES ARE TYPE IN4148, UNLESS NOTED.
4. ON ALL INTEGRATED CIRCUITS, PIN 16 IS Vcc AND PIN 8 IS GND, UNLESS NOTED. ON TYPE 7473, PIN 4 IS Vcc AND PIN 11 IS GND. ON TYPE 9501, PIN 14 IS Vcc AND PIN 7 IS GND.

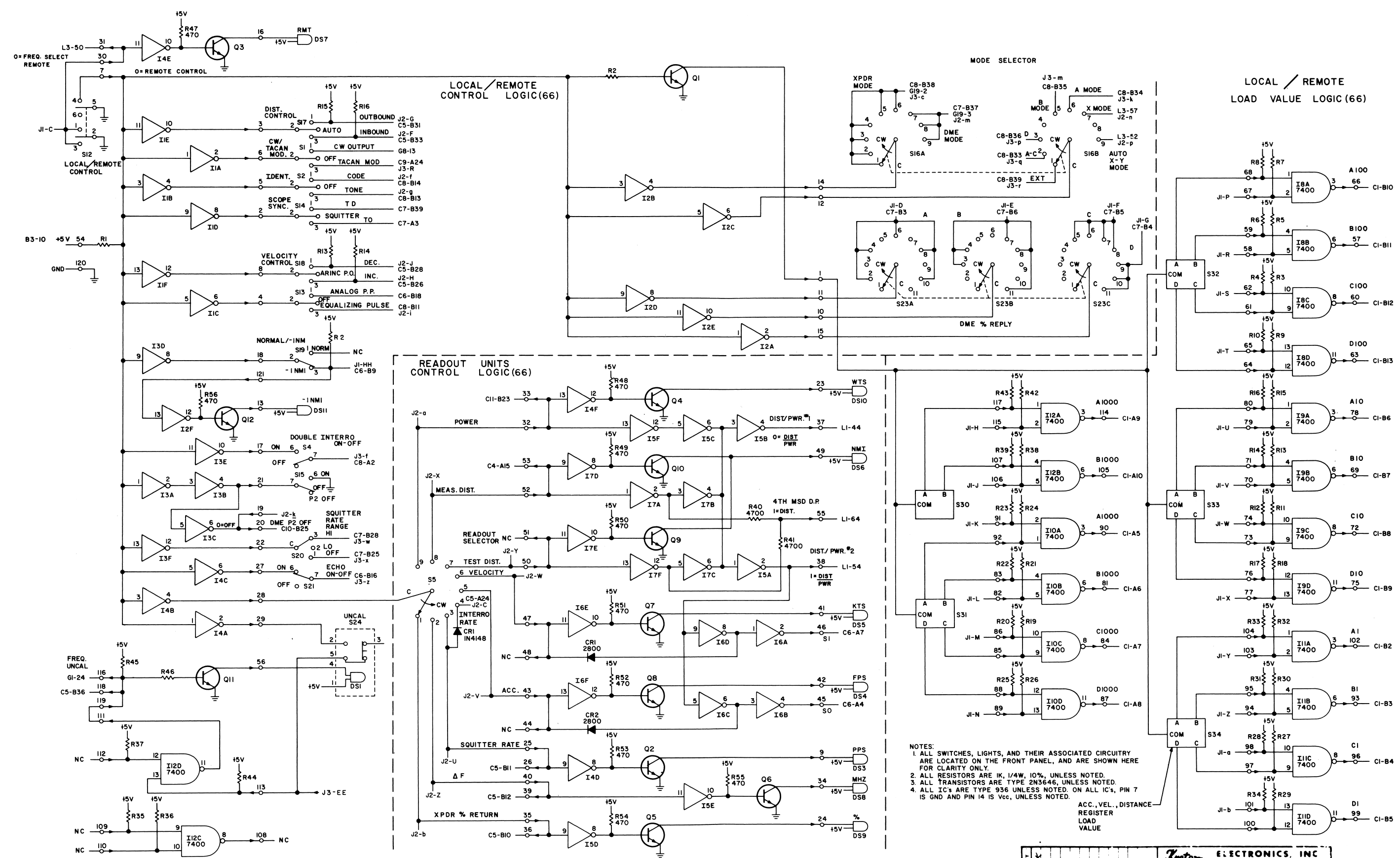
1. ALL RESISTORS ARE 1/4W, 10%, UNLESS NOTED.
2. ALL CAPACITOR VALUES ARE IN PICOFARADS, UNLESS NOTED.
3. ALL DIODES ARE TYPE IN4148, UNLESS NOTED.
4. ON ALL INTEGRATED CIRCUITS, PIN 16 IS Vcc AND PIN 8 IS GND, UNLESS NOTED. ON TYPE 7473, PIN 4 IS Vcc AND PIN 11 IS GND. ON TYPE 9501, PIN 14 IS Vcc AND PIN 7 IS GND.

REV. C	DATE	BY	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
REV. C	DATE	BY	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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REV. C	DATE	BY	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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REV. C	DATE	BY	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28																																																																								

ELECTRONICS, INC.
CHANUTE, KANSAS 66720

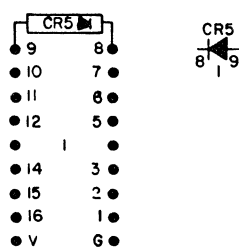
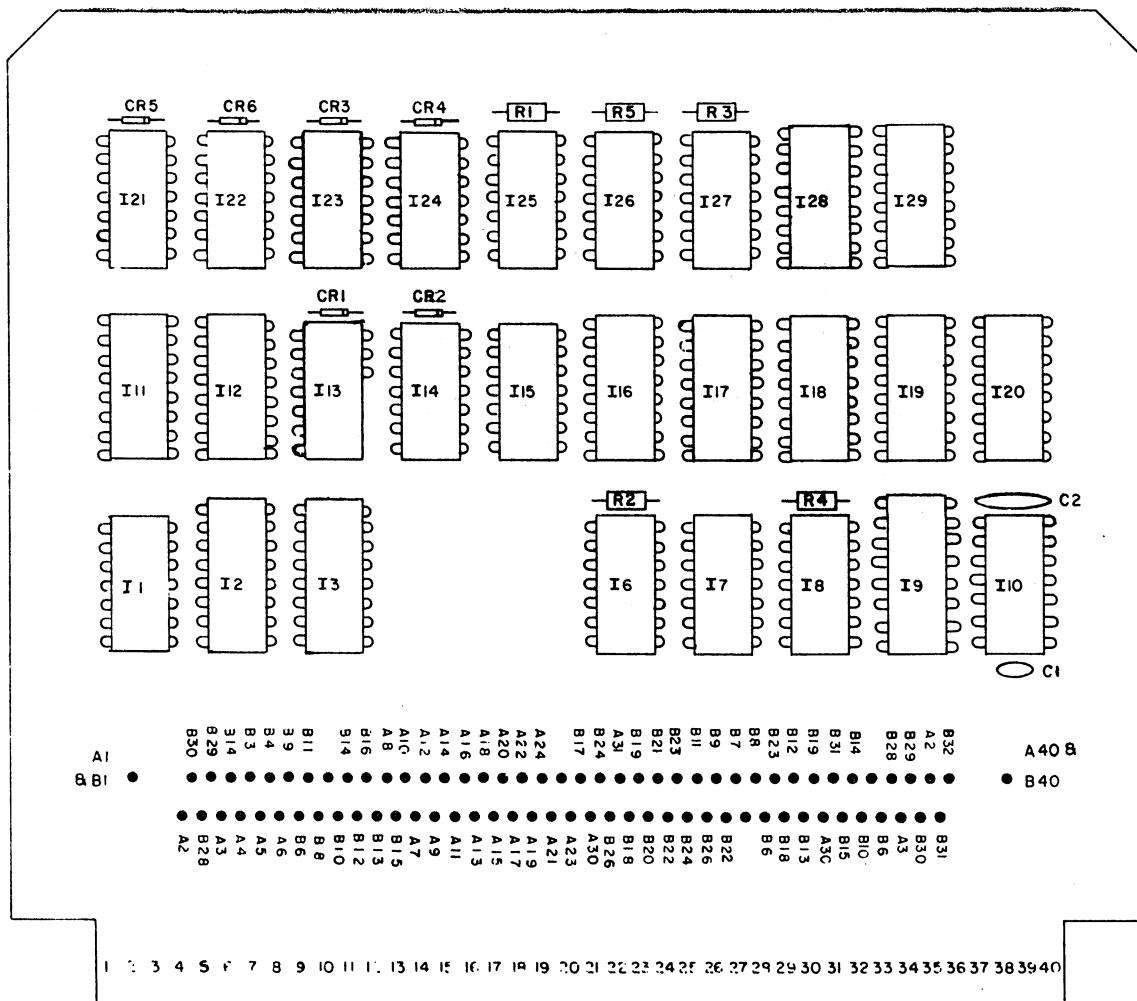


BY				ELECTRONICS, INC.			
DATE				CHANUTE, KANSAS 64720			
REV				TOLERANCES			
1				NONE			
2				MATERIAL			
3				NAME			
4				SCHEMATIC DIAGRAM			
5				READOUT DRIVER LOGIC L1			
6				PART NUMBER			
7				002-5079-00			



DATE		JLS 10-72		TOLERANCES		NONE		MATERIAL		NONE	
REV		1		SCALE		NONE		SMT		OF 1	
MOD		2671		NAME		SCHEMATIC DIAGRAM- READOUT CONTROL LOGIC, L2		PART NUMBER		002-5075-00	
REV		1		DATE		10-72		SMT		OF 1	

Custom. ELECTRONICS, INC.
CHANDLER, KANSAS 66740



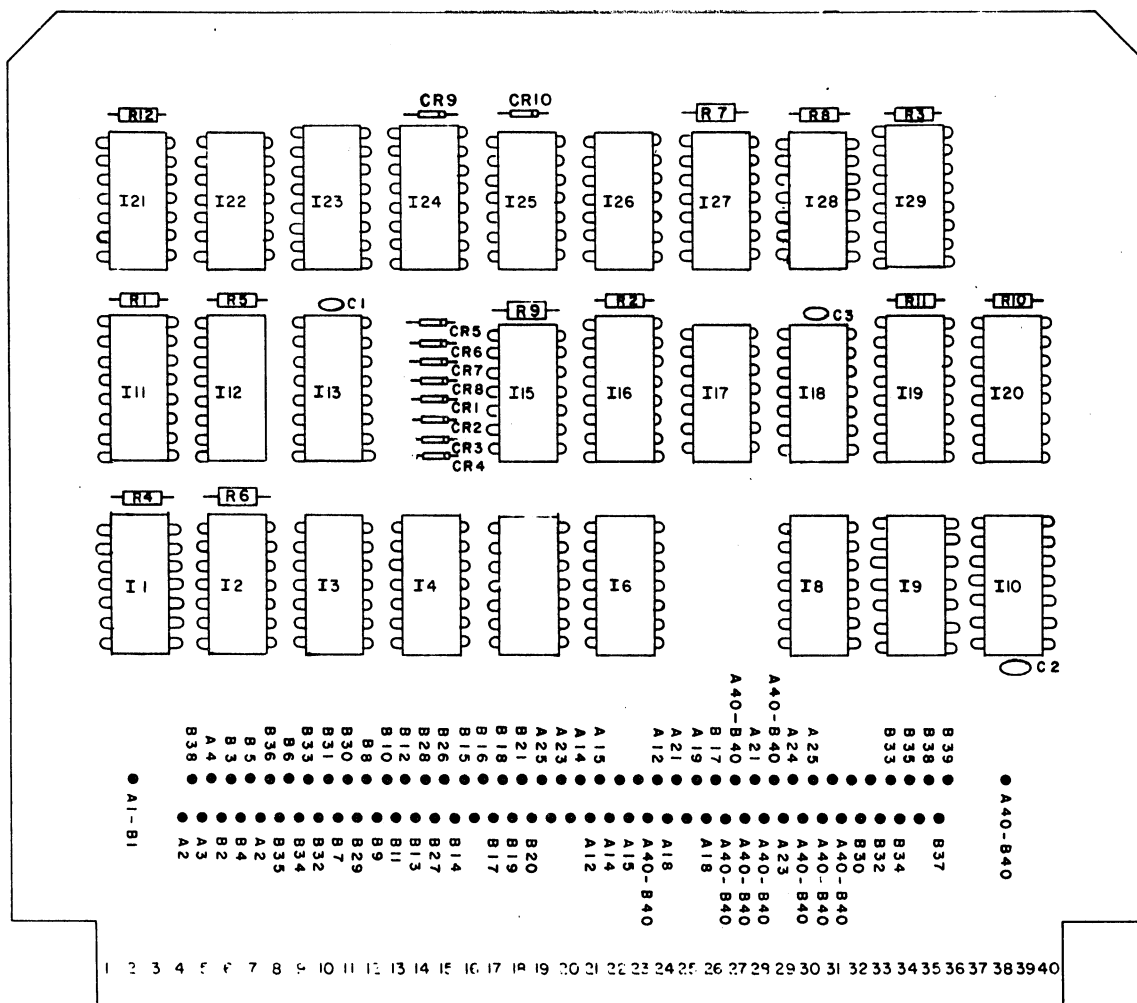
DET 1

NOTE:

1. SCHEMATIC IC REFERENCE NOS. AND PIN NOS. CORRESPOND WITH THE NOS. ON THE BOARD (SEE DET 1). THUS PIN 14 AND PIN 8 OF A 14 PIN IC ARE DESIGNATED AS PIN 16 AND PIN 10 ON THE SCHEMATIC

Rev. 3 Aug. 1978

Kustom.		ELECTRONICS INC.	
CHICAGO, ILLINOIS 60677			
DATE: 8-78	DESIGN: NONE	MATERIAL: NONE	
NAME: CARD ASSY (NO. 1)			
SCALE: NONE	SHEET: 1 OF 1	PART NUMBER: 300-5053-00	



CR511	
● 9	8 ●
● 10	7 ●
● 11	6 ●
● 12	5 ●
● 14	3 ●
● 15	2 ●
● 16	1 ●
● V	G ●

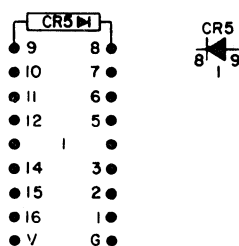
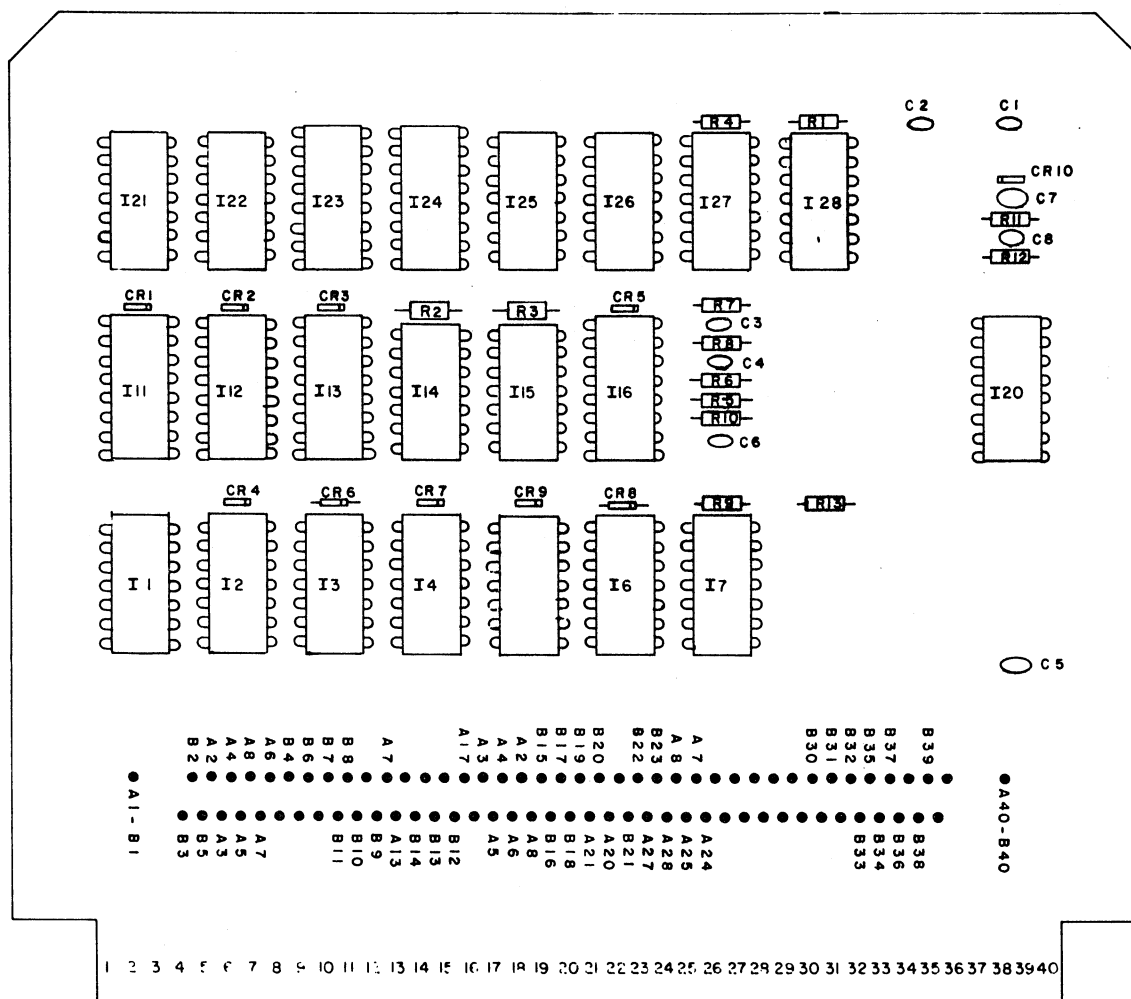
DET 1



NOTES

- SCHEMATIC IC REFERENCE NOS. AND PIN NOS. CORRESPOND WITH THE NOS. ON THE BOARD (SEE DET 1). THUS PIN 14 AND PIN 8 OF A 14 PIN IC ARE DESIGNATED AS PIN 16 AND PIN 10 ON THE SCHEMATIC.

Kustom		ELECTRONICS INC.	
CHANDLER KANSAS 66720			
DATE 8-78	TOLERANCE NONE	MATERIAL NONE	
NAME KIDDOO	NAME CARD ASSY. (NO. 2)		
SCALE NONE	SMT 01	PART NUMBER 300-5054-00	

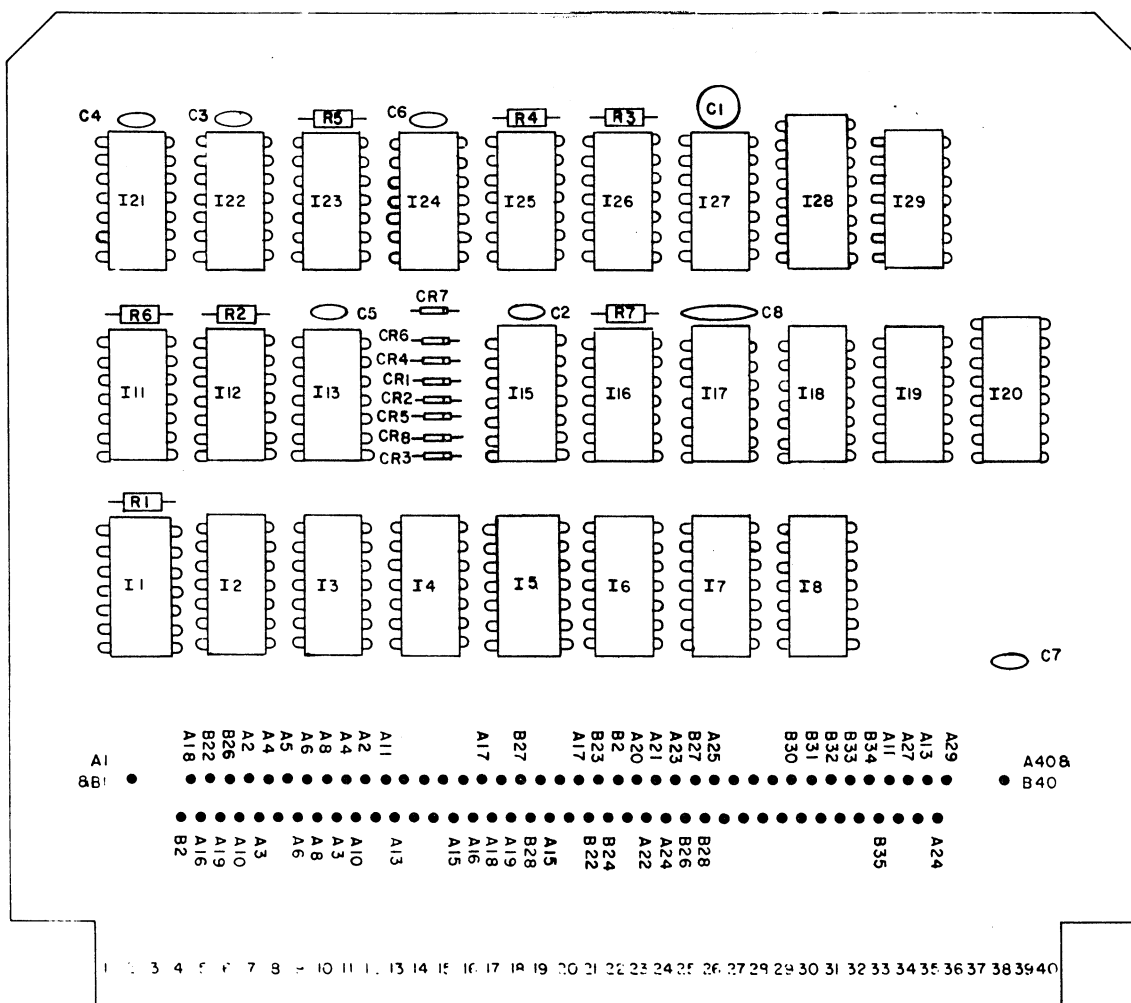


DET 1

NOTES

1. SCHEMATIC IC REFERENCE NOS. AND PIN NOS. CORRESPOND WITH THE NOS. ON THE BOARD (SEE DET 1). THUS PIN 14 AND PIN 8 OF A 14 PIN IC ARE DESIGNATED AS PIN 16 AND PIN 10 ON THE SCHEMATIC.

Custom. ELECTRONICS INC. (MANUTE, KANSAS) 06720			
DRG KIDDOO	DATE 8-78	TOLERANCES NONE	MATERIAL NONE
CHK	DATE	NAME CARD ASSY. (NO. 3)	
ENGR	SCALE NONE	SMT OF 1	PART NUMBER 300-5055-00



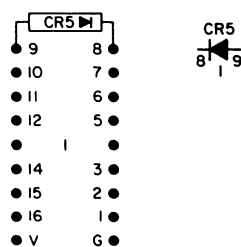
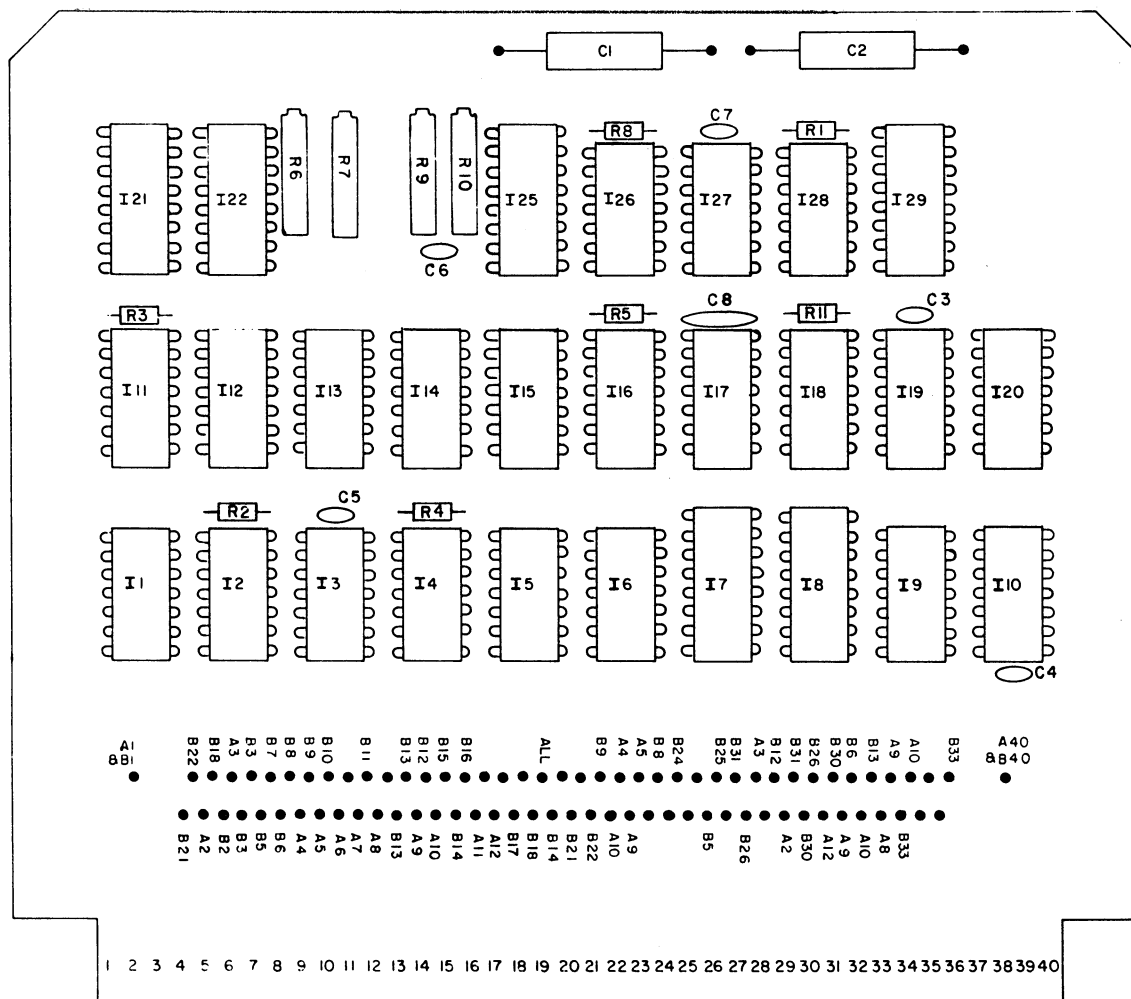
NOTE:

1. SCHEMATIC IC REFERENCE NOS. AND PIN NOS. CORRESPOND WITH THE NOS. ON THE BOARD (SEE DET 1). THUS PIN 14 AND PIN 8 OF A 14 PIN IC ARE DESIGNATED AS PIN 16 AND PIN 10 ON THE SCHEMATIC.

DET 1

Rev. 3 Aug. 1978

Kustom.		ELECTRONICS INC.	
MINUTIE KANSAS 66720			
DATE KIDDOO 8-78	DATE	MATERIAL NONE	MATERIAL NONE
NAME CARD ASSY (NO. 4)			
SCALE NONE	SMT 01	PART NUMBER 300-5056-00	

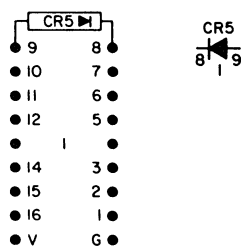
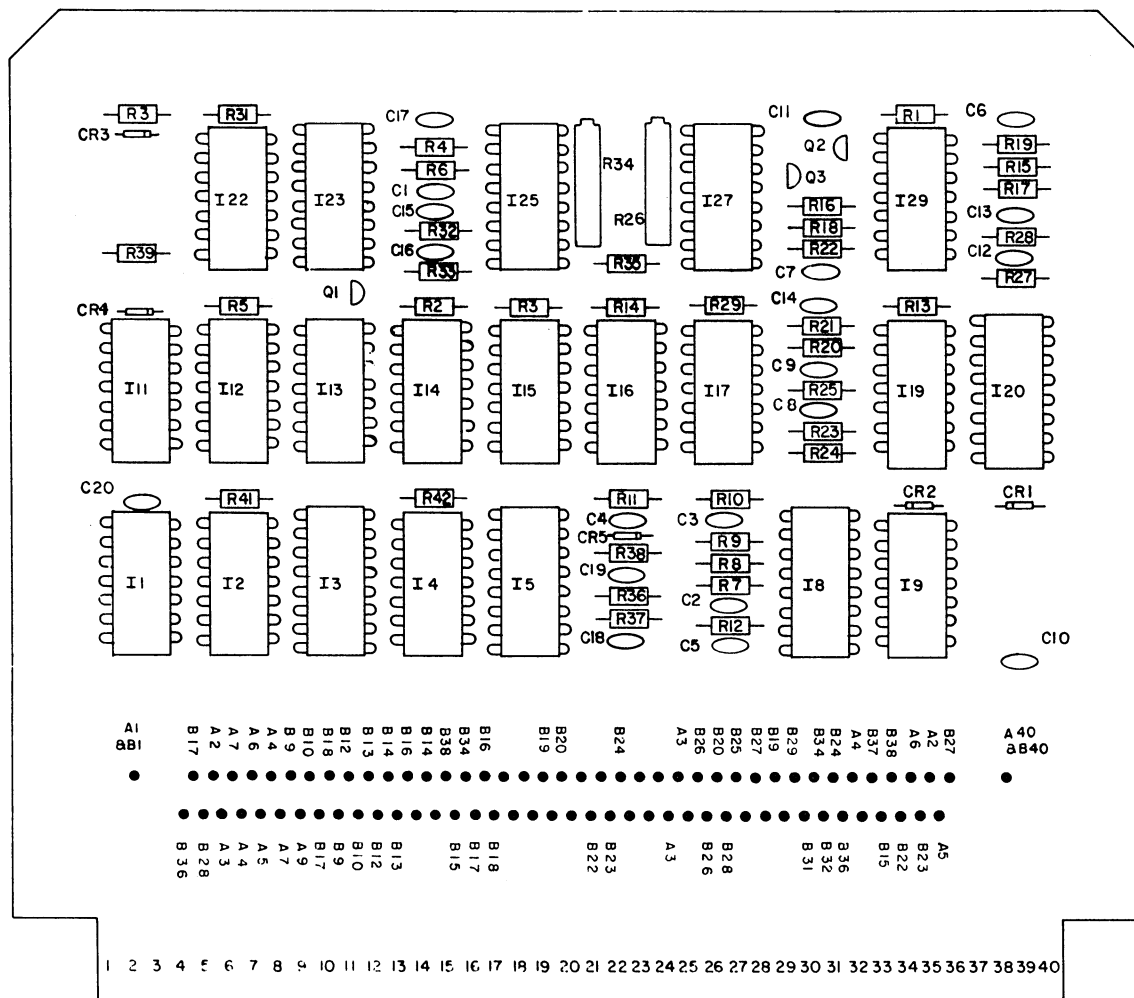


DET 1

NOTE:

1. SCHEMATIC IC REFERENCE NOS. AND PIN NOS. CORRESPOND WITH THE NOS. ON THE BOARD (SEE DET 1). THUS PIN 14 AND PIN 8 OF A 14 PIN IC ARE DESIGNATED AS PIN 16 AND PIN 10 ON THE SCHEMATIC.

		Kustom. ELECTRONICS, INC. CHANUTE KANSAS 66720	
DRN	KIDD 00	DATE	8-78
CHK		DATE	
TNGR		NAME	
SCALE		PART NUMBER	
NONE		300-5058-00	
TOLERANCES		NONE	
MATERIAL		NONE	
CARD ASSY. NO. 6			



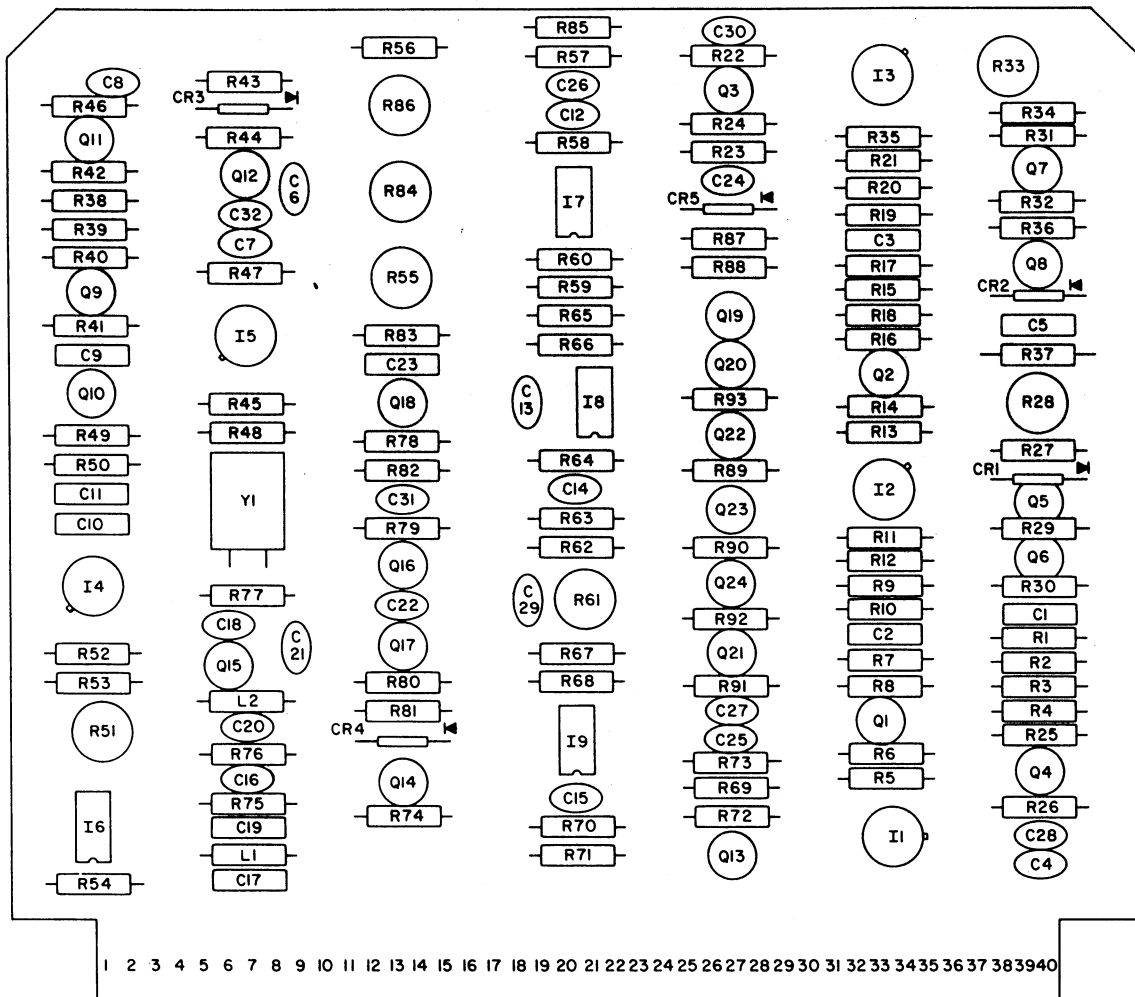
DET 1

NOTE:

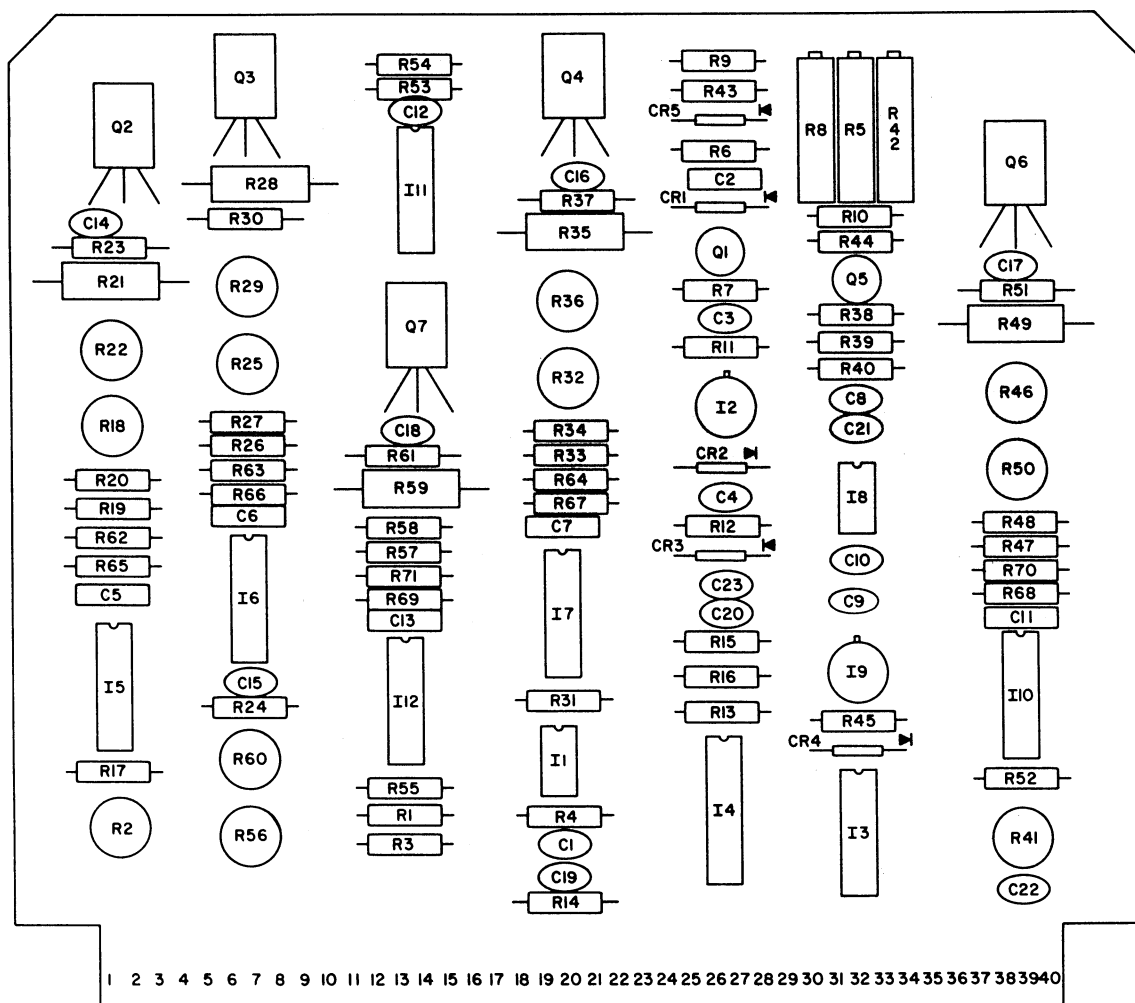
1. SCHEMATIC IC REFERENCE NOS. AND PIN NOS. CORRESPOND WITH THE NOS. ON THE BOARD (SEE DET 1). THUS PIN 14 AND PIN 8 OF A 14 PIN IC ARE DESIGNATED AS PIN 16 AND PIN 10 ON THE SCHEMATIC.

Rev. 3 Aug. 1978

Kustom. ELECTRONICS, INC. CHANUTE KANSAS 66720		DRN: KIDDOO	DATE: 8-78	TOLERANCES: NONE	MATERIAL: NONE
		CHK:	DATE:	NAME: CARD ASSY. NO. 7	
ENG:		SCALE: NONE	SHT: 1 OF 1	PART NUMBER: 300-5059-00	

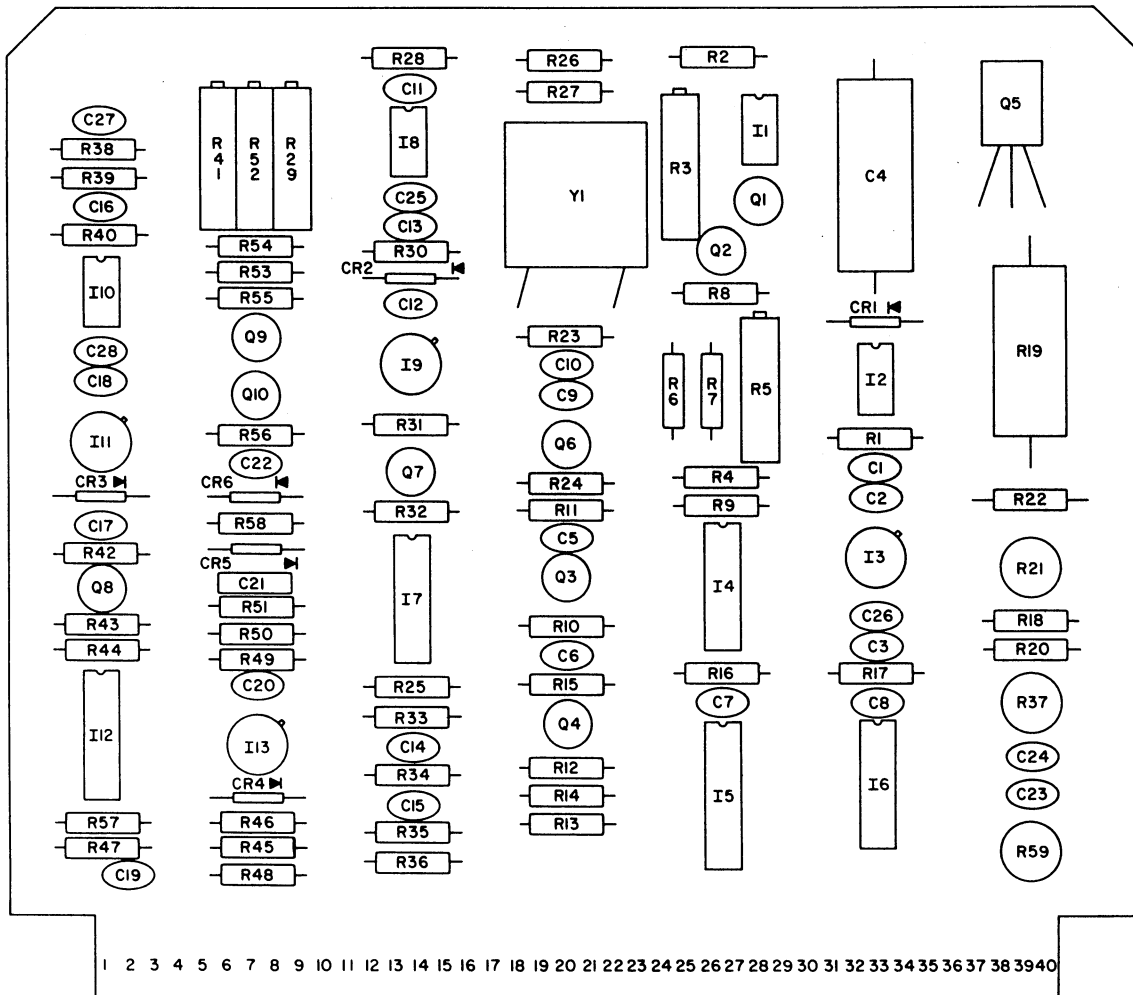


Kustom.		ELECTRONICS, INC.	
CHANDLER, KANSAS		66720	
DRN	DATE	TOLERANCES	MATERIAL
JLS	8-72	NONE	NONE
CHK	DATE	NAME	
	8-72	CARD 9	
ENCL	SMT	PART NUMBER	
NONE		300-5061-00	

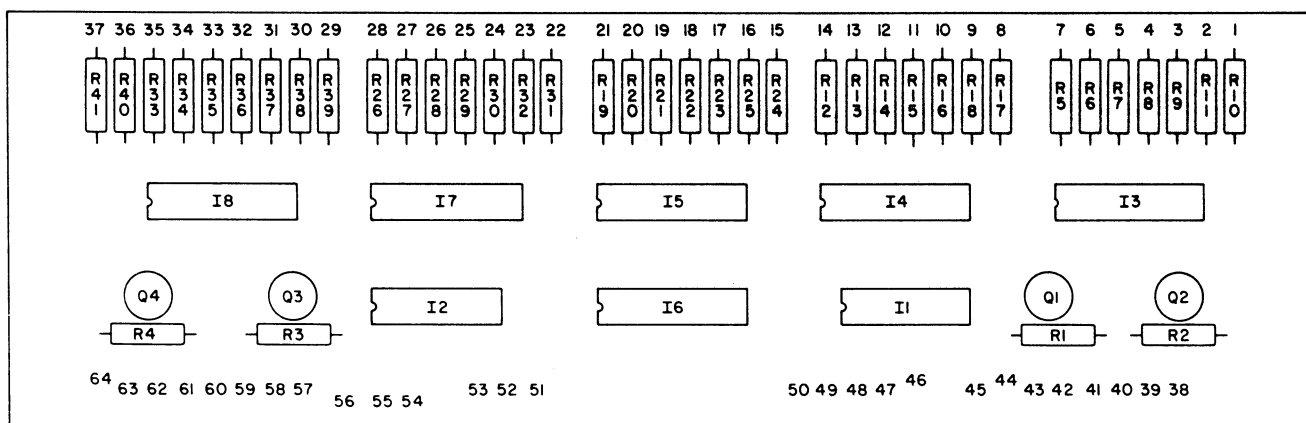


REV. 3		DATE 8-72		JLS		DATE 10-72		NAME		CARD 10	
1		1013		1013		1013		1013		1013	
SCALE		NONE		SMT		OF		PART NUMBER		300-5062-00	
TOLERANCES		NONE		MATERIAL		NONE		ELECTRONICS, INC.		CHANUTE, KANSAS 66720	

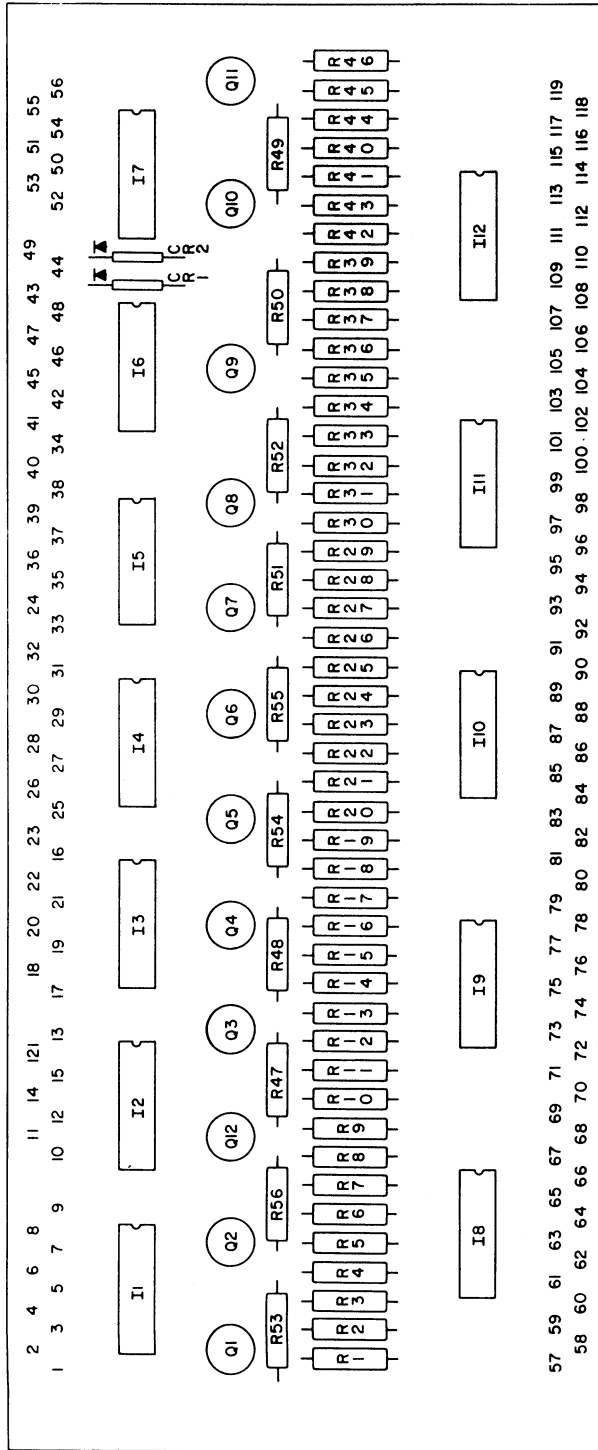
Rev. 3 Aug. 1978



Kustom.		ELECTRONICS, INC.	
MANUTE KANSAS 66720			
OWN	JLS	DATE	8-72
ENG	DATE	TOLERANCES	NONE
NAME	NAME	MATERIAL	NONE
NAME	NAME	CARD II	
NAME	NAME	PAP	300-5063-00
NONE			



		Kustom.		ELECTRONICS, INC.	
		CHANUTE KANSAS		66720	
DRN	JLS	DATE	9-72	TOLERANCES	NONE
CHK		DATE		MATERIAL	NONE
ENGR		NAME			
SCALT	NONE	INDICATOR DRIVER LOGIC, LI			
SMT	OF	PART NUMBER			
		300-5079-00			



Custom ELECTRONICS		DATE: 9-72 JLS: 9-72 NONE	DATE: 10-72 JLS: 10-72 NONE
REMOTE CONTROL LOGIC, L2		SCALE: 1/2" = 1" NONE	PART NUMBER: 300-5075-00
REV: 1 C: 1 O: 1 NO: 1 DATE: 1	I1 I2 I3 I4 I5 I6 I7 I8 I9 I10 I11 I12	Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12	R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12

PARTS LIST

ASSEMBLY NO:	200-5053-00
DESCRIPTION:	CARD #1 SUB-ASSY
ASSY DWG NO:	300-5053-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C2	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
CR1-CR6	DIODE 1N4148	007-6016-00
I1	VT IC SN7473N	007-7057-01
I2	VT IC MC4016P	007-7080-01
I3	VT IC MC4016P	007-7080-01
I6-I8	VT IC SN74196	007-7006-01
I9	VT IC SN74157N	007-7069-01
I10	VT IC MC3001P	007-7076-01
I11	VT IC MC4016P	007-7080-01
I12	VT IC MC4016P	007-7080-01
I13	VT IC 930	007-7002-01
I14	VT IC SN7410N	007-7051-01
I15	IC SN7404N	007-7049-00
I16-I20	VT IC SN74192N	007-7063-01
I21	VT IC SN7490	007-7059-01
I22	VT IC SN7490	007-7059-01
I23	VT IC SN74H11N	007-7052-01
I24	VT IC SN7410N	007-7051-01
I25	VT IC 930	007-7002-01
I26	VT IC 930	007-7002-01
I27	VT IC SN7473N	007-7057-01
I28	VT IC MC4016P	007-7080-01
I29	VT IC MC4016P	007-7080-01
R1-R5	RESISTOR F/C 1K 1/8W 10%	130-0102-05
	PC BD 5053 1	009-5053-00
	ROLL PIN 3/32 X 1/4 LG	090-0022-02
	EJECTOR CIRCUIT BD	090-0107-00

ASSEMBLY NO:	200-5054-00
DESCRIPTION:	CARD #2 SUB-ASSY
ASSY DWG NO:	300-5054-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C2	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C3	CAPACITOR CER .001 UF 15%	107-0005-00
CR1-CR10	DIODE 1N4148	007-6016-00
I1	VT IC SN7402	007-7048-01
I2	VT IC SN7405N	007-7050-01
I3-I6	VT IC SN74192N	007-7063-01
I8	VT IC MC9309P	007-7068-01
I9	VT IC MC9309P	007-7068-01
I10	VT IC SN74196	007-7006-01
I11	VT IC SN7404N	007-7049-01
I12	VT IC SN7405N	007-7050-01
I13	VT IC SN7405N	007-7050-01
I15	VT IC 930	007-7002-01
I16	VT IC SN7404N	007-7049-01
I17	VT IC SN7410N	007-7051-01
I18	VT IC SN7405N	007-7050-01
I19	VT IC 930	007-7002-01
I20	VT IC SN7410N	007-7051-01
I21	VT IC SN7490	007-7059-01
I22	VT IC SN7410N	007-7051-01
I23	VT IC 930	007-7002-01
I24	VT IC SN7490	007-7059-01
I25	VT IC MC3006	007-7078-01
I26	VT IC SN7410N	007-7051-01
I27	VT IC SN7490	007-7059-01
I28	VT IC 930	007-7002-01
I29	VT IC SN7473N	007-7057-01
R1-R10	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R11	RESISTOR F/C 270 OHM 1/8W 1%	130-0271-05
R12	RESISTOR F/C 1K 1/8W 10%	130-0102-05
	PC BD 5054 2	009-5054-00
	ROLL PIN 3/32 X 1/4 LG	090-0022-02
	EJECTOR CIRCUIT BD	090-0107-00

ASSEMBLY NO:	200-5055-00
DESCRIPTION:	CARD #3 SUB-ASSY
ASSY DWG NO:	300-5055-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1-C4	CAPACITOR CER .001 UF 15%	107-0005-00
C5	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C6	CAPACITOR CER .001 UF 15%	107-0005-00
C7	CAPACITOR D/C 150 PF X5F 10%	109-1510-35
C8	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
CR1-CR10	DIODE 1N4148	007-6016-00
I1	VT IC MC9309P	007-7068-01
I2-I7	VT IC SN74196	007-7006-01
I11-I13	VT IC 936	007-7003-01
I14	VT IC 930	007-7002-01
I15	VT IC SN7400N	007-7047-01
I16	VT IC 930	007-7002-01
I20	VT IC 9602	007-7032-01
I21-I25	VT IC MC4016P	007-7080-01
I26	VT IC 9602	007-7032-01
I27	VT IC SN7402	007-7048-01
I28	VT IC SN7405N	007-7050-01
R1-R6	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R7	RESISTOR PREC 10K 1/8W 1%	125-1002-01
R8	RESISTOR PREC 10K 1/8W 1%	125-1002-01
R9	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R10	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R11	RESISTOR PREC 9.31K 1/8W 1%	125-9311-01
R12	RESISTOR PREC 23.7K 1/8W 1%	125-2372-01
R13	RESISTOR F/C 1K 1/8W 10%	130-0102-05
	PC BD 5055 3	009-5055-00
	ROLL PIN 3/32 X 1/4 LG	090-0022-02
	EJECTOR CIRCUIT BD	090-0107-00
	SPAGHETTI TUBING 22 AWG	150-0001-04

ASSEMBLY NO:	200-5056-00
DESCRIPTION:	CARD #4 SUB-ASSY
ASSY DWG NO:	300-5056-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR TANT 47 UF 20V 20%	096-1007-10
C2	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C3	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C4-C6	CAPACITOR CER .001 UF 15%	107-0005-00
C7	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C8	CAPACITOR D/C 100 PF X5F 10%	109-1010-35
CR1-CR8	DIODE 1N4148	007-6016-00
I1-I8	VT IC SN7495N	007-7061-01
I11	VT IC SN7404N	007-7049-01
I12	VT IC SN7404N	007-7049-01
I13	VT IC 930	007-7002-01
I15	VT IC 936	007-7003-01
I16	VT IC SN7402	007-7048-01
I17	VT IC SN7473N	007-7057-01
I18	VT IC SN7410N	007-7051-01
I19	VT IC MC3001P	007-7076-01
I20	VT IC MC9309P	007-7068-01
I21	VT IC SN7473N	007-7057-01
I22	VT IC SN7400N	007-7047-01
I23	VT IC SN7473N	007-7057-01
I24	VT IC SN7493N	007-7060-01
I25	VT IC SN7402	007-7048-01
I26	VT IC SN7400N	007-7047-01
I27	VT IC 9601	007-7070-01
I28	VT IC MC9309P	007-7068-01
I29	VT IC SN74196	007-7006-01
R1	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R2	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R3	RESISTOR F/C 18K 1/8W 10%	130-0183-05
R4	RESISTOR F/C 220 OHM 1/8W 10%	130-0221-05
R5	RESISTOR F/C 220 OHM 1/8W 10%	130-0221-05
R6	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R7	RESISTOR F/C 100 OHM 1/8W 10%	130-0101-05
	PC BD 5056 4	009-5056-00
	ROLL PIN 3/32 X 1/4 LG	090-0022-02
	EJECTOR CIRCUIT BD	090-0107-00

ASSEMBLY NO:	200-5057-00
DESCRIPTION:	CARD #5 SUB-ASSY
ASSY DWG NO:	300-5057-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C2	CAPACITOR D/C 33 PF X5F 10%	109-3300-35
C3	CAPACITOR D/C 82 PF X5F 10%	109-8200-35
C4	CAPACITOR D/C 680 PF X5F 10%	109-6810-35
C5	CAPACITOR CER .001 UF 15%	107-0005-00
C6	CAPACITOR D/C 680 PF X5F 10%	109-6810-35
C7	CAPACITOR CER .001 UF 15%	107-0005-00
C8	CAPACITOR CER .001 UF 15%	107-0005-00
C9	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
CR1-CR20	DIODE 1N4148	007-6016-00
I1	VT IC SN74157N	007-7069-01
I2	VT IC SN7473N	007-7057-01
I3	VT IC MC3001P	007-7076-01
I4	VT IC MC3001P	007-7076-01
I5-I7	VT IC MC4016P	007-7080-01
I8	VT IC MC3001P	007-7076-01
I9	VT IC MC3001P	007-7076-01
I11	VT IC SN74196	007-7006-01
I12	VT IC SN74196	007-7006-01
I13-I16	VT IC MC3002P	007-7077-01
I17	VT IC MC9309P	007-7068-01
I19	VT IC MC9309P	007-7068-01
I20	VT IC SN74196	007-7006-01
I21	VT IC SN74196	007-7006-01
I22-I24	VT IC MC3002P	007-7077-01
I25	VT IC MC3001P	007-7076-01
I26	VT IC MC3002P	007-7077-01
I28	VT IC 936	007-7003-01
I29	VT IC MC9309P	007-7068-01
L1	INDUCTOR 82 UH 10%	019-2016-33
L2	INDUCTOR 82 UH 10%	019-2016-33
Q1-Q4	TRANSISTOR 35677	007-0008-00
R1	RESISTOR F/C 2.2K 1/8W 10%	130-0222-05
R2	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R3	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R4	RESISTOR F/C 220 OHM 1/8W 10%	130-0221-05
R5	RESISTOR F/C 560 OHM 1/8W 10%	130-0561-05
R6	RESISTOR F/C 2.2K 1/8W 10%	130-0222-05
R7-R12	RESISTOR F/C 1.2K 1/8W 10%	130-0122-05
R13	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R14	RESISTOR F/C 10K 1/8W 10%	130-0103-05
R15	RESISTOR F/C 10K 1/8W 10%	130-0103-05
	PC BD 5057 5	009-5057-00
	ROLL PIN 3/32 X 1/4 LG	090-0022-02
	EJECTOR CIRCUIT BD	090-0107-00

ASSEMBLY NO:	200-5058-00
DESCRIPTION:	CARD #6 SUB-ASSY
ASSY DWG NO:	300-5058-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR P/C .1 UF	108-5000-01
C2	CAPACITOR P/C .1 UF	108-5000-01
C3	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
C4	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C5	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
C6	CAPACITOR M/C 6800 PF 100V	107-0002-39
C7	CAPACITOR M/C 3300 PF 100V	107-0002-35
C8	CAPACITOR D/C 10 PF NPO 5%	110-1000-04
I1	VT IC SN7474N	007-7058-01
I2	VT IC SN7474N	007-7058-01
I3	VT IC SN74H103	007-7085-01
I4	VT IC 9601	007-7070-01
I5	VT IC SN74H21	007-7053-01
I6	VT IC SN74H21	007-7053-01
I7	VT IC MC9309P	007-7068-01
I8	VT IC MC9309P	007-7068-01
I9	VT IC SN74196	007-7006-01
I10	VT IC SN74196	007-7006-01
I11	VT IC SN74H103	007-7085-01
I12-I17	VT IC SN74196	007-7006-01
I18	VT IC SN7473N	007-7057-01
I19	VT IC SN7410N	007-7051-01
I20	VT IC SN7473N	007-7057-01
I21	VT IC SN74157N	007-7069-01
I22	VT IC 9602	007-7032-01
I25	VT IC 9602	007-7032-01
I26	VT IC SN7402	007-7048-01
I27	VT IC 9601	007-7070-01
I28	VT IC SN7404N	007-7049-01
I29	VT IC SN74157N	007-7069-01
R1-R3	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R4	RESISTOR PREC 20K 1/8W 1%	125-2002-01
R5	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R6	RESISTOR POT 50K 20 TURN	133-0060-11
R7	RESISTOR POT 50K 20 TURN	133-0060-11
R8	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R9	RESISTOR POT 50K 20 TURN	133-0060-11
R10	RESISTOR POT 50K 20 TURN	133-0060-11
R11	RESISTOR F/C 10K 1/8W 10%	130-0103-05
	PC BD 5058 6	009-5058-00
	ROLL PIN 3/32 X 1/4 LG	090-0022-02
	EJECTOR CIRCUIT BD	090-0107-00

ASSEMBLY NO:	200-5059-01
DESCRIPTION:	CARD #7 SUB-ASSY
ASSY DWG NO:	300-5059-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR M/C .0033 UF 50V 10%	107-0001-17
C2	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
C3	CAPACITOR D/C 150 PF X5F 10%	109-1510-35
C4	CAPACITOR D/C 150 PF X5F 10%	109-1510-35
C5	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
C6	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C7-C9	CAPACITOR D/C 150 PF X5F 10%	109-1510-35
C10	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C11	CAPACITOR M/C 470 PF 100V	107-0002-26
C12	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
C13	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
C14	CAPACITOR D/C 100 PF X5F 10%	109-1010-35
C15	CAPACITOR M/C .056 UF 50V 10%	107-0001-32
C16	CAPACITOR M/C .0056 UF 50V 10%	107-0001-20
C17	CAPACITOR M/C .0033 UF 50V 10%	107-0001-17
C18	CAPACITOR D/C 150 PF X5F 10%	109-1510-35
C19	CAPACITOR D/C 150 PF X5F 10%	109-1510-35
C20	CAPACITOR D/C 470 PF X5F 10%	109-4710-35
CR1	DIODE 5082-2800	007-6021-00
CR2-CR5	DIODE 1N4148	007-6016-00
I1	VT IC 936	007-7003-01
I2	VT IC QUAD 2 INPUT NAND TRIGGER	007-7138-01
I3	VT IC SN74167	007-7139-01
I4	VT IC SN7490	007-7059-01
I5	VT IC 9602	007-7032-01
I8	VT IC 9602	007-7032-01
I9	VT IC SN7473N	007-7057-01
I11	VT IC SN7473N	007-7057-01
I12	VT IC SN7451	007-7056-01
I13	VT IC SN74H21	007-7053-01
I14	VT IC SN7402	007-7048-01
I15	VT IC SN74196	007-7006-01
I16	VT IC SN74196	007-7006-01
I17	VT IC SN7410N	007-7051-01
I19	VT IC SN7404N	007-7049-01
I20	VT IC 9602	007-7032-01
I22	VT IC SN7400N	007-7047-01
I23	VT IC 9602	007-7032-01
I25	VT IC 9602	007-7032-01
I27	VT IC 9602	007-7032-01
I29	VT IC SN7474N	007-7058-01
Q1	TRANSISTOR 35677	007-0008-00
Q2	TRANSISTOR 35677	007-0008-00
Q3	TRANSISTOR PNP 2N4249	007-0009-00
R1-R3	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R4	RESISTOR F/C 33K 1/8W 10%	130-0333-05
R5	RESISTOR F/C 3.3K 1/8W 10%	130-0332-05
R6	RESISTOR PREC 33.2K 1/8W 1%	125-3322-01
R7	RESISTOR PREC 33.2K 1/8W 1%	125-3322-01

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
R8	RESISTOR F/C 10K 1/8W 10%	130-0103-05
R9	RESISTOR F/C 10K 1/8W 10%	130-0103-05
R10	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R11	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R12	RESISTOR PREC 18.2K 1/8W 1%	125-1822-01
R13	RESISTOR F/C 10K 1/8W 10%	130-0103-05
R14	RESISTOR F/C 10K 1/8W 10%	130-0103-05
R15	RESISTOR F/C 100K 1/8W 10%	130-0104-05
R16	RESISTOR F/C 10K 1/8W 10%	130-0103-05
R17	RESISTOR F/C 27K 1/8W 10%	130-0273-05
R18	RESISTOR F/C 8.2K 1/8W 10%	130-0822-05
R19	RESISTOR F/C 47K 1/8W 10%	130-0473-05
R20	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R21	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R22	RESISTOR F/C 4.7K 1/8W 10%	130-0472-05
R23-R25	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R26	RESISTOR POT 50K 20 TURN	133-0060-11
R27	RESISTOR PREC 20K 1/8W 1%	125-2002-01
R28	RESISTOR PREC 20K 1/8W 1%	125-2002-01
R29	RESISTOR F/C 100 OHM 1/8W 10%	130-0101-05
R30	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R31	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R32	RESISTOR PREC 39.2K 1/8W 1%	125-3922-01
R33	RESISTOR PREC 39.2K 1/8W 1%	125-3922-01
R34	RESISTOR POT 50K 20 TURN	133-0060-11
R35	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R36-R38	RESISTOR F/C 10K 1/8W 10%	130-0103-05
R39	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R41	RESISTOR F/C 4.7K 1/8W 10%	130-0472-05
R42	RESISTOR F/C 4.7K 1/8W 10%	130-0472-05
	MULTIWIRE PC BD	009-5059-01
	ROLL PIN 3/32 X 1/4 LG	090-0022-02
	EJECTOR CIRCUIT BD	090-0107-00

ASSEMBLY NO:	200-5060-00
DESCRIPTION:	CARD #8 SUB-ASSY
ASSY DWG NO:	300-5060-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR D/C 330 PF X5F 10%	109-3310-35
C2	CAPACITOR CER .001 UF 15%	107-0005-00
C3	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
C4	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C5	CAPACITOR D/C 330 PF X5F 10%	109-3310-35
C6	CAPACITOR M/C .01 UF 50V 10%	107-0001-23
C7	CAPACITOR D/C 330 PF X5F 10%	109-3310-35
C8	CAPACITOR M/C .01 UF 50V 10%	107-0001-23
C9	CAPACITOR TANT 330 UF 6V 20%	096-1007-04
CR1-CR3	DIODE 5082-2800	007-6021-00
CR4-CR6	DIODE 1N4148	007-6016-00
I2	VT IC SN7400N	007-7047-01
I3	VT IC SN7400N	007-7047-01
I4	VT IC SN7404N	007-7049-01
I6	VT IC SN7410N	007-7051-01
I7	VT IC SN7474N	007-7058-01
I8	VT IC SN74H103	007-7085-01
I9	VT IC SN7473N	007-7057-01
I10	VT IC 8281	007-7005-01
I11-I13	VT IC SN74165N	007-7062-01
I14	VT IC SN7402	007-7048-01
I15	VT IC SN7404N	007-7049-01
I16	VT IC MC4016P	007-7080-01
I17	VT IC MC3006	007-7078-01
I18	VT IC MC3006	007-7078-01
I19	VT IC SN7442	007-7054-01
I20	VT IC SN7442	007-7054-01
I21	VT IC SN7473N	007-7057-01
I22	VT IC SN74196	007-7006-01
I23	VT IC MC4016P	007-7080-01
I24	VT IC 9602	007-7032-01
I25	VT IC 930	007-7002-01
I26	VT IC SN7473N	007-7057-01
I27	VT IC SN7400N	007-7047-01
I29	VT IC 9602	007-7032-01
I30	VT IC 936	007-7003-01
R1	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R2	RESISTOR F/C 270 OHM 1/8W 10%	130-0271-05
R3-R6	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R7	RESISTOR PREC 5.62K 1/8W 1%	125-5621-01
R8-R10	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R11	RESISTOR F/C 220 OHM 1/8W 10%	130-0221-05
R12-R15	RESISTOR F/C 1K 1/8W 10%	130-0102-05
R16	RESISTOR F/C 10K 1/8W 10%	130-0103-05
R17	RESISTOR PREC 33.2K 1/8W 1%	125-3322-01
R18-R20	RESISTOR F/C 10K 1/8W 10%	130-0103-05
R21	RESISTOR PREC 33.2K 1/8W 1%	125-3322-01
R22	RESISTOR PREC 49.9K 1/8W 1%	125-4992-01
	PC BD 5060 8	009-5060-00
	ROLL PIN 3/32 X 1/4 LG	090-0022-02
	EJECTOR CIRCUIT BD	090-0107-00

ASSEMBLY NO:
DESCRIPTION:
ASSY DWG NO:

200-5061-00
CARD #9 SUB-ASSY
300-5061-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1-C3	CAPACITOR MLR .027 UF 100V 10%	105-0030-32
C4	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C5	CAPACITOR MLR .0018 UF 100V	105-0030-18
C6	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C7	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C8	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C9-C11	CAPACITOR MLR .1 UF 100V 10%	105-0030-39
C12-C14	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C15	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C16	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C17	CAPACITOR CER	107-0002-22
C18	CAPACITOR D/C 470 PF X5F 10%	109-4710-35
C19	CAPACITOR MLR .01 UF 100V 5%	105-0030-00
C20	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C21	CAPACITOR D/C 33 PF X5F 10%	109-3300-35
C22	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C23	CAPACITOR MICA 390 PF 300V 10%	100-0000-08
C24	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C25	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C26	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C27-C29	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C30	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C31	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C32	CAPACITOR D/C .001 UF Z5F 10%	109-1021-16
CR1	DIODE 1N4148	007-6016-00
CR2	DIODE 1N4148	007-6016-00
CR3	IC 1N4738A	007-6026-00
CR4	DIODE 1N4148	007-6016-00
CR5	DIODE GERMANIUM 1N270	007-6020-00
I1-I5	VT IC LM311H	007-7045-01
I6-I9	IC N5741V UT	007-7042-01
L1	COIL .15 UH	019-2016-00
L2	INDUCTOR MOLD 1 UH 10%	019-2016-10
Q1-Q3	TRANSISTOR 35677	007-0008-00
Q4	TRANSISTOR D13T1 PUT	007-0036-00
Q5	TRANSISTOR PNP 2N4249	007-0009-00
Q6	TRANSISTOR 35677	007-0008-00
Q7	TRANSISTOR 2N3646	007-0025-00
Q8	TRANSISTOR 38735	007-0002-00
Q9	TRANSISTOR PNP 2N4249	007-0009-00
Q10-Q13	TRANSISTOR 35677	007-0008-00
Q14	TRANSISTOR 2N3646	007-0025-00
Q15	TRANSISTOR PNP 2N5208	007-0026-00
Q16	TRANSISTOR D13T1 PUT	007-0036-00
Q17	TRANSISTOR 35677	007-0008-00
Q18	TRANSISTOR D13T1 PUT	007-0036-00
Q19-Q24	TRANSISTOR 35677	007-0008-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
R1	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R2	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R3	RESISTOR PREC 4.42K 1/8W 1%	125-4421-01
R4	RESISTOR PREC 4.42K 1/8W 1%	125-4421-01
R5	RESISTOR PREC 1K 1%	125-1001-01
R6	RESISTOR PREC 100 OHM 1%	125-1000-01
R7	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R8	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R9	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R10	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R11	RESISTOR PREC 4.42K 1/8W 1%	125-4421-01
R12	RESISTOR PREC 4.42K 1/8W 1%	125-4421-01
R13	RESISTOR PREC 1K 1%	125-1001-01
R14	RESISTOR PREC 100 OHM 1%	125-1000-01
R15	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R16	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R17	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R18	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R19	RESISTOR PREC 4.42K 1/8W 1%	125-4421-01
R20	RESISTOR PREC 4.42K 1/8W 1%	125-4421-01
R21	RESISTOR PREC 1K 1%	125-1001-01
R22	RESISTOR PREC 100 OHM 1%	125-1000-01
R23	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R24	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R25	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R26	RESISTOR F/C 120K 1/4W 10%	130-0124-25
R27	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R28	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R29	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R30	RESISTOR F/C 15K 1/4W 10%	130-0153-25
R31	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R32	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R33	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R34	RESISTOR F/C 6.8K 1/4W 10%	130-0682-25
R35	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R36	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R37	RESISTOR F/C 300 OHM 1/2W 5%	130-0301-13
R38	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R39	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R40	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R41	RESISTOR F/C 47K 1/4W 10%	130-0473-25
R42	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R43	RESISTOR F/C 47K 1/4W 10%	130-0473-25
R44	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R45	RESISTOR F/C 220K 1/4W 10%	130-0224-25
R46	RESISTOR F/C 22 OHM 1/4W 10%	130-0220-25
R47	RESISTOR F/C 100K 1/4W 10%	130-0104-25
R48	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R49	RESISTOR F/C 47K 1/4W 10%	130-0473-25
R50	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R51	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R52	RESISTOR F/C 100K 1/4W 10%	130-0104-25

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
R53	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R54	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R55	RESISTOR POT 20K 1/2W 10%	133-0042-13
R56	RESISTOR F/C 33K 1/4W 10%	130-0333-25
R57	RESISTOR F/C 510 OHM 1/4W 5%	130-0511-23
R58	RESISTOR F/C 220K 1/4W 10%	130-0224-25
R59	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R60	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R61	RESISTOR POT 20K 1/2W 10%	133-0042-13
R62	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R63	RESISTOR F/C 47 OHM 1/4W 10%	130-0470-25
R64	RESISTOR F/C 33K 1/4W 10%	130-0333-25
R65	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R66	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R67	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R68	RESISTOR F/C 33K 1/4W 10%	130-0333-25
R69	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R70	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R71-R74	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R75	RESISTOR F/C 560 OHM 1/4W 10%	130-0561-25
R76	RESISTOR F/C 8.2K 1/4W 10%	130-0822-25
R77	RESISTOR F/C 22K 1/4W 10%	130-0223-25
R78	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R79	RESISTOR F/C 47K 1/4W 10%	130-0473-25
R80	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R81	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R82	RESISTOR F/C 1.2K 1/4W 10%	130-0122-25
R83	RESISTOR F/C 220K 1/4W 10%	130-0224-25
R84	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R85	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R86	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R87	RESISTOR F/C 100K 1/4W 10%	130-0104-25
R88	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R89	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R90	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R91	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R92	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R93	RESISTOR F/C 22K 1/4W 10%	130-0223-25
Y1	CRYSTAL 32.365 MHZ	044-0003-00
	PC BD 9	009-5061-00
	ROLL PIN 3/32 X 1/4 LG	090-0022-02
	CLIP CRYSTAL	090-0106-03
	EJECTOR CIRCUIT BD	090-0107-00
	RIVET BUTTON HEAD	092-0012-22

ASSEMBLY NO:	200-5062-00
DESCRIPTION:	CARD #10 SUB-ASSY
ASSY DWG NO:	300-5062-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C2	CAPACITOR M/C 820 PF 100V	107-0002-09
C3	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C4	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C5-C7	CAPACITOR MICA 470 PF 300V 5%	100-0000-00
C8	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C9	CAPACITOR M/C .01 UF 100V 5%	107-0002-41
C10	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C11	CAPACITOR MICA 470 PF 300V 5%	100-0000-00
C12	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
C13	CAPACITOR MICA 470 PF 300V 5%	100-0000-00
C14-C18	CAPACITOR D/C .01 UF 25V 20%	109-1030-46
C19	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C20	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C21	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C22	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C23	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
CR1-CR5	DIODE 1N4148	007-6016-00
I1	IC N5741V UT	007-7042-01
I2	VT IC LM306H	007-7044-01
I3	VT IC SN7473N	007-7057-01
I4	VT IC 9602	007-7032-01
I5-I7	VT IC 1 WATT POWER AMP	007-7196-01
I8.	IC N5741V UT	007-7042-01
I9.	VT IC LM306H	007-7044-01
I10	VT IC 1 WATT POWER AMP	007-7196-01
I11	VT IC MC4016P	007-7070-01
I12	VT IC 1 WATT POWER AMP	007-7196-01
Q1	TRANSISTOR 2N3646	007-0025-00
Q2-Q4	TRANSISTOR 2N4922	007-0030-00
Q5	TRANSISTOR 2N3646	007-0025-00
Q6	TRANSISTOR 2N4922	007-0030-00
Q7	TRANSISTOR 2N4922	007-0030-00
R1	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R2	RESISTOR POT 1K TYPE SV	133-0042-07
R3	RESISTOR PREC 100K 1/8W 1%	125-1003-01
R4	RESISTOR PREC 10K 1/8W 1%	125-1002-01
R5	RESISTOR POT 50K 20 TURN	133-0060-11
R6	RESISTOR PREC 49.9K 1/8W 1%	125-4992-01
R7	RESISTOR F/C 2.7 OHM 1/4W 10%	130-0027-25
R8	RESISTOR POT 500 OHM 20 TURN	133-0060-05
R9	RESISTOR PREC 47.5 OHM 1%	125-0475-01
R10	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R11	RESISTOR F/C 1.5K 1/4W 10%	130-0152-25
R12-R14	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R15	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R16	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R17	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R18	RESISTOR POT 1K TYPE SV	133-0042-07

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
R19	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R20	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R21	RESISTOR W/W 5 OHM 3 1/4W 10%	132-0009-00
R22	RESISTOR POT 200 OHM 10% 1 TURN	133-0042-03
R23	RESISTOR F/C 100 OHM 1/2W 10%	130-0101-15
R24	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R25	RESISTOR POT 1K TYPE SV	133-0042-07
R26	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R27	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R28	RESISTOR W/W 5 OHM 3 1/4W 10%	132-0009-00
R29	RESISTOR POT 200 OHM 10% 1 TURN	133-0042-03
R30	RESISTOR F/C 100 OHM 1/2W 10%	130-0101-15
R31	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R32	RESISTOR POT 1K TYPE SV	133-0042-07
R33	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R34	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R35	RESISTOR W/W 5 OHM 3 1/4W 10%	132-0009-00
R36	RESISTOR POT 200 OHM 10% 1 TURN	133-0042-03
R37	RESISTOR F/C 100 OHM 1/2W 10%	130-0101-15
R38	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R39	RESISTOR PREC 100K 1/8W 1%	125-1003-01
R40	RESISTOR PREC 10K 1/8W 1%	125-1002-01
R41	RESISTOR POT 1K TYPE SV	133-0042-07
R42	RESISTOR POT 50K 20 TURN	133-0060-11
R43	RESISTOR PREC 49.9K 1/8W 1%	125-4992-01
R44	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R45	RESISTOR F/C 1.5K 1/4W 10%	130-0152-25
R46	RESISTOR POT 1K TYPE SV	133-0042-07
R47	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R48	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R49	RESISTOR W/W 5 OHM 3 1/4W 10%	132-0009-00
R50	RESISTOR POT 200 OHM 10% 1 TURN	133-0042-03
R51	RESISTOR F/C 100 OHM 1/2W 10%	130-0101-15
R52	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R53	RESISTOR F/C 20K 1/4W 10%	130-0203-25
R54	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R55	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R56	RESISTOR POT 1K TYPE SV	133-0042-07
R57	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R58	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R59	RESISTOR W/W 5 OHM 3 1/4W 10%	132-0009-00
R60	RESISTOR POT 200 OHM 10% 1 TURN	133-0042-03
R61	RESISTOR F/C 100 OHM 1/2W 10%	130-0101-15
R62-R64	RESISTOR F/C 100 OHM 1/4W 10%	130-0101-25
R65	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R66	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R67	RESISTOR F/C 470 OHM 1/4W 10%	130-0471-25
R68	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R69	RESISTOR F/C 470 OHM 1/4W 10%	130-0471-25
	PC BD 5062 10	009-5062-00
	NUT HEX #4-40 KEPS	089-2058-21
	SCREW PHP 4-40 X 5/16	089-5058-05
	ROLL PIN 3/32 X 1/4 LG	090-0022-02
	EJECTOR CIRCUIT BD	090-0107-00

ASSEMBLY NO:	200-5063-00
DESCRIPTION:	CARD #11 SUB-ASSY
ASSY DWG NO:	300-5063-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1-C3	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C4	CAPACITOR P/C 1 UF	108-5000-02
C5	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C6	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C7	CAPACITOR D/C .01 UF 25V 20%	109-1030-46
C8	CAPACITOR D/C .01 UF 25V 20%	109-1030-46
C9	CAPACITOR D/C 47 PF N750 5%	110-4700-34
C10	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
C11	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C12	CAPACITOR M/C .0015 UF 100V	107-0002-32
C13	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C14	CAPACITOR D/C 150 PF X5F 10%	109-1510-35
C15	CAPACITOR D/C 150 PF X5F 10%	109-1510-35
C16	CAPACITOR TANT 1 UF 35V 20%	096-1007-23
C17	CAPACITOR M/C .0015 UF 100V	107-0002-32
C18	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C19	CAPACITOR D/C 150 PF X5F 10%	109-1510-35
C20	CAPACITOR M/C 1000 PF 50V 10%	107-0001-11
C21	CAPACITOR MLR .1 UF 100V 10%	105-0030-39
C22	CAPACITOR D/C 33 PF X5F 10%	109-3300-35
C23	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C24	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C25	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C26	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
C27	CAPACITOR TANT 33 UF 10V 20%	096-1007-09
C28	CAPACITOR TANT 10 UF 20V 20%	096-1007-08
CR1-CR5	DIODE 1N4148	007-6016-00
CR6	DIODE 5082-2800	007-6021-00
I1	IC N5741V UT	007-7042-01
I2	IC N5741V UT	007-7042-01
I3	VT IC LM306H	007-7044-01
I4	VT IC SN7473N	007-7057-01
I5	VT IC 9602	007-7032-01
I6	VT IC 9601	007-7070-01
I7	VT IC SN7473N	007-7057-01
I8	IC N5741V UT	007-7042-01
I9	VT IC N5710T	007-7046-01
I10	IC N5741V UT	007-7042-01
I11	VT IC N5710T	007-7046-01
I12	VT IC SN7473N	007-7057-01
I13	VT IC LM306H	007-7044-01
Q1	TRANSISTOR PNP 2N4249	007-0009-00
Q2	TRANSISTOR 2N3646	007-0025-00
Q3	TRANSISTOR D13T1 PUT	007-0036-00
Q4	TRANSISTOR 35677	007-0008-00
Q5	TRANSISTOR 2N4922	007-0030-00
Q6-Q8	TRANSISTOR 2N3646	007-0025-00
Q9	TRANSISTOR 2N4917	007-0027-00
Q10	TRANSISTOR 2N3646	007-0025-00
R1	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R2	RESISTOR PREC 182K 1/8W 1%	125-1823-01
R3	RESISTOR POT 20K 20 TURN	133-0060-10

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
R4	RESISTOR PREC 47.5 OHM 1%	125-0475-01
R5	RESISTOR POT 200 OHM	133-0060-04
R6	RESISTOR F/C 2.7 OHM 1/4W 10%	130-0027-25
R7	RESISTOR F/C 1.5K 1/4W 10%	130-0152-25
R8	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R9	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R10	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R11	RESISTOR F/C 270K 1/4W 10%	130-0274-25
R12	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R13	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R14	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R15-R17	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R18	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R19	RESISTOR W/W 25 OHM 5W 10%	132-0006-00
R20	RESISTOR F/C 270 OHM 1/4W 10%	130-0271-25
R21	RESISTOR POT 20K 1/2W 10%	133-0042-13
R22	RESISTOR F/C 1.5K 1/2W 10%	130-0152-15
R23	RESISTOR F/C 56K 1/4W 10%	130-0563-25
R24	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R25	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R26	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R27	RESISTOR PREC 100K 1/8W 1%	125-1003-01
R28	RESISTOR PREC 10K 1/8W 1%	125-1002-01
R29	RESISTOR POT 50K 20 TURN	133-0060-11
R30	RESISTOR PREC 49.9K 1/8W 1%	125-4992-01
R31	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R32	RESISTOR F/C 1.5K 1/4W 10%	130-0152-25
R33-R36	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R37	RESISTOR POT 1K TYPE SV	133-0042-07
R38	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R39	RESISTOR PREC 100K 1/8W 1%	125-1003-01
R40	RESISTOR PREC 10K 1/8W 1%	125-1002-01
R41	RESISTOR POT 50K 20 TURN	133-0060-11
R42	RESISTOR PREC 49.9K 1/8W 1%	125-4992-01
R43	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R44	RESISTOR F/C 1.5K 1/4W 10%	130-0152-25
R45-R48	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R49	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R50	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R51	RESISTOR F/C 39K 1/4W 10%	130-0393-25
R52	RESISTOR POT 5K 20 TURN	133-0060-08
R53	RESISTOR F/C 3.3K 1/4W 10%	130-0332-25
R54	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R55	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R56	RESISTOR F/C 1.5K 1/4W 10%	130-0152-25
R57	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R58	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R59	RESISTOR POT 1K TYPE SV	133-0042-07
Y1	CRYSTAL 1.379310 MHZ	044-0001-00
	PC BD 5063 11	009-5063-00
	NUT HEX #4-40 KEPS	089-2058-21
	SCREW PHP 4-40 X 5/16	089-5058-05
	ROLL PIN 3/32 X 1/4 LG	090-0022-02
	CLIP CRYSTAL	090-0106-01
	EJECTOR CIRCUIT BD	090-0107-00
	RIVET BUTTON HEAD	092-0012-22

ASSEMBLY NO:	200-5079-00
DESCRIPTION:	READOUT DRIVER LOGIC (L1)
ASSY DWG NO:	300-5079-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
CR1-CR5	DISPLAY 5082-7750 HP	037-0057-00*
I1	VT IC 936	007-7003-01
I2	VT IC 936	007-7003-01
I3-I8	IC 7447A	007-7199-00
Q1-Q4	TRANSISTOR 35677	007-0008-00
R1	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R2	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R3	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R4	RESISTOR F/C 220 OHM 1/4W 10%	130-0221-25
R5-R41	RESISTOR F/C 180 OHM 1/4W 10%	130-0181-25
	PC BOARD INDICATOR	009-5079-00
	IC SOCKET	033-0002-00

*UNITS WITH SERIAL NUMBERS BELOW T 300 WILL HAVE:
 DISPLAY MANN I 037-0012-00

ASSEMBLY NO: 200-5075-00
DESCRIPTION: READOUT CONTROL LOGIC (L2)
ASSY DWG NO: 300-5075-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
CR1	DIODE 5082-2900	007-6022-00
CR2	DIODE 5082-2900	007-6022-00
I1-I7	VT IC 936	007-7003-01
I8-I12	VT IC SN7400N	007-7047-01
Q1-Q12	TRANSISTOR 2N3646	007-0025-00
R1-R39	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R40	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R41	RESISTOR F/C 4.7K 1/4W 10%	130-0472-25
R42-R46	RESISTOR F/C 1K 1/4W 10%	130-0102-25
R47-R56	RESISTOR F/C 470 OHM 1/4W 10%	130-0471-25
	PC BD SWITCHING	009-5075-00

SECTION V

**FRONT PANEL AND POWER
SUPPLY INDEX**

SCHEMATIC DIAGRAMS

**FRONT PANEL
POWER SUPPLY**

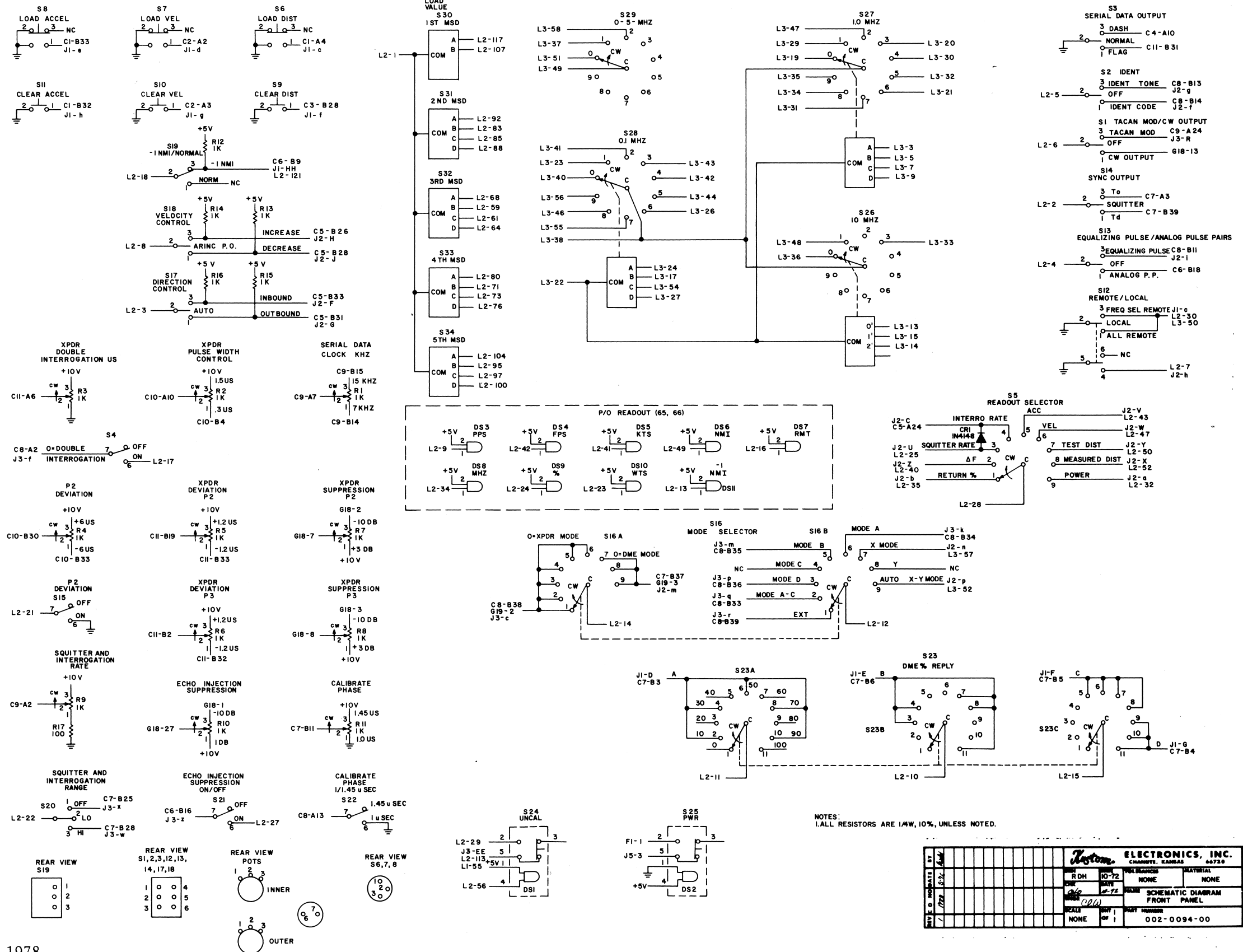
ASSEMBLY DRAWINGS

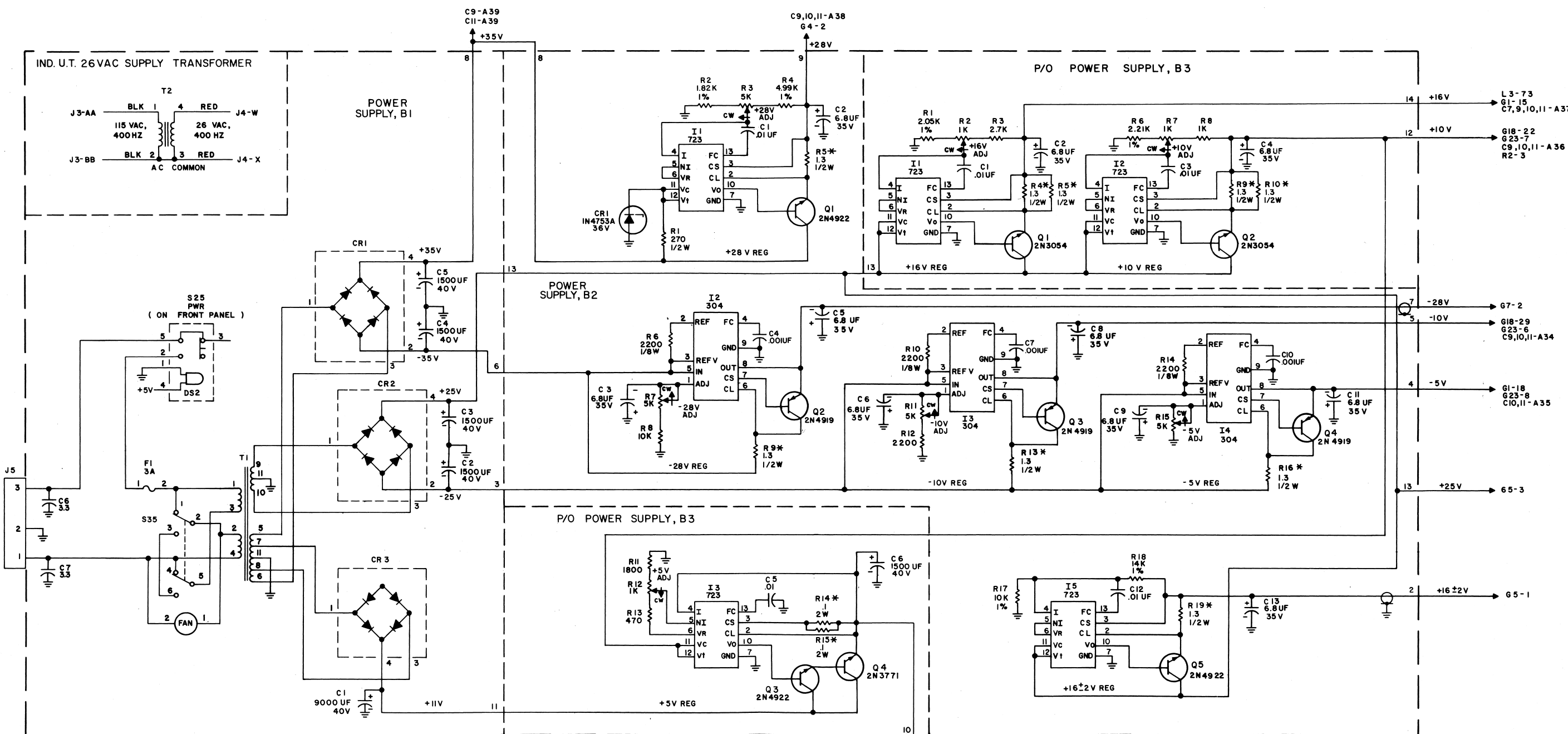
**FRONT PANEL
LEFT & RIGHT SIDE RAILS
REAR PANEL
INTERMEDIATE PLATE — TOP
INTERMEDIATE PLATE — BOTTOM
UNIT ASSEMBLY
POWER SUPPLY B2
POWER SUPPLY B3**

PARTS LIST

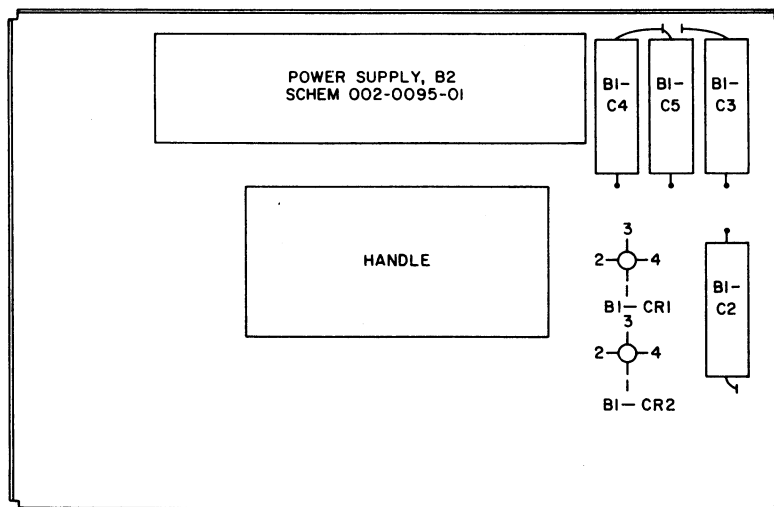
WIRE LIST

CHANNEL FREQ/MHZ FREQ SELECTOR

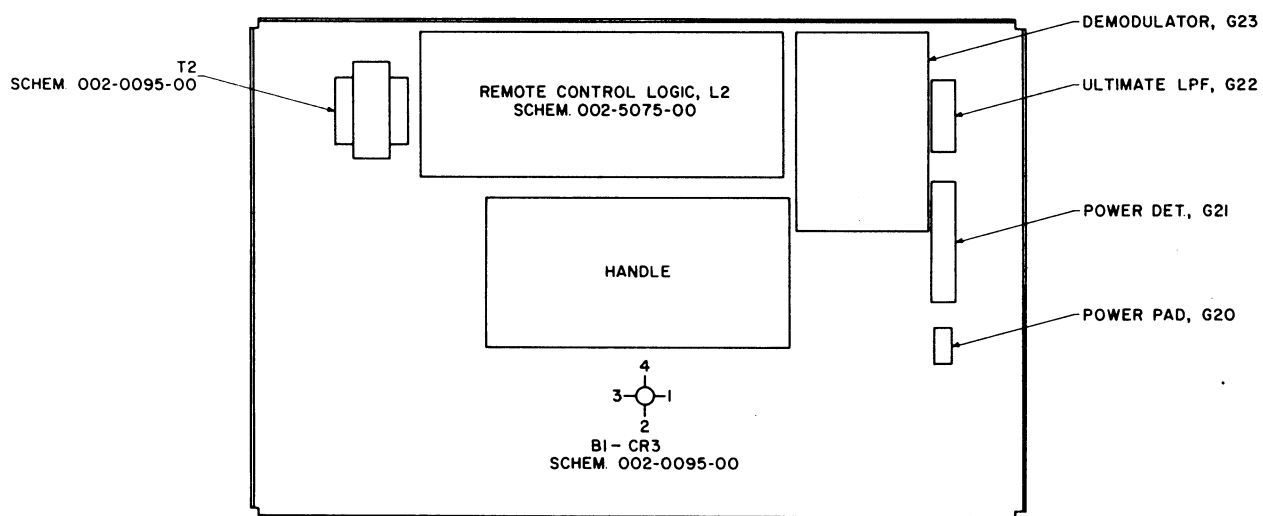




BY		DATE		ELECTRONICS, INC.	
R.D.H.		10/72		CHANNUTS, KANSAS 64720	
NONE		NONE		MATERIAL	
NONE		NONE		NONE	
SCALE		NONE		SCHEMATIC DIAGRAM	
NONE		NONE		POWER SUPPLIES B1,B2,B3	
PART NUMBER		002-0095-00/02		PART NUMBER	



LEFT SIDE RAIL, INSIDE



RIGHT SIDE RAIL, INSIDE

NOTES:

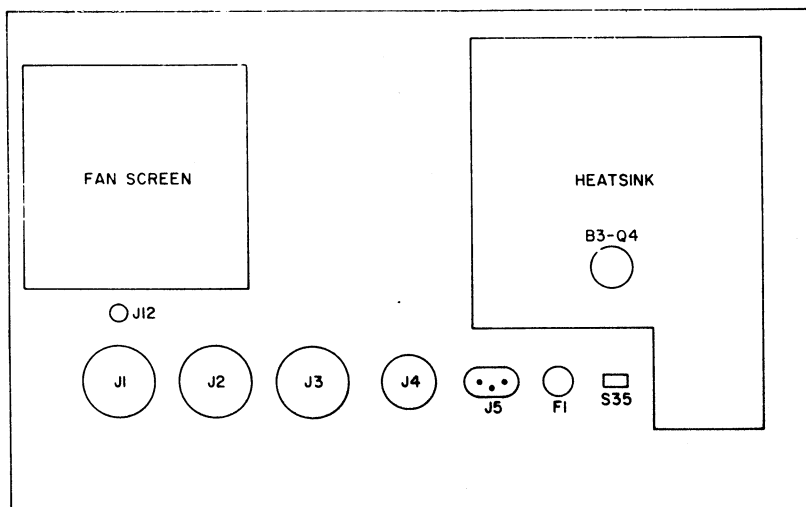
LEFT SIDE RAIL

1. REFER TO SCHEM. 002-0095-00, UNLESS NOTED.

RIGHT SIDE RAIL

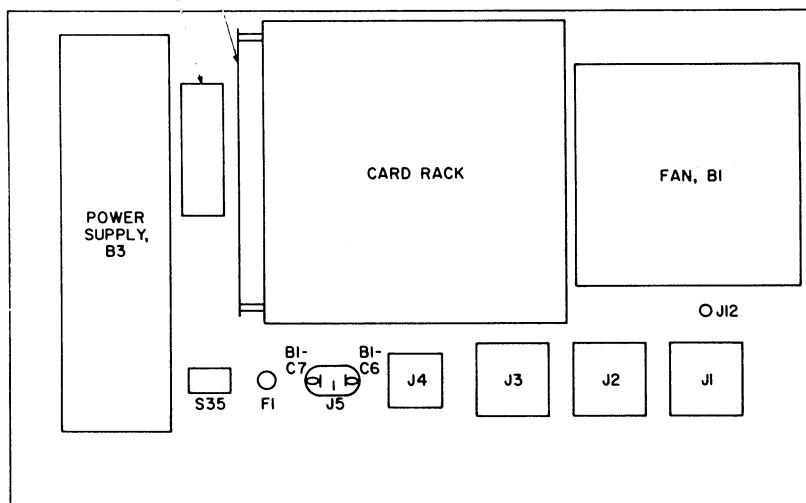
1. REFER TO SCHEM. 002-5073-00, UNLESS NOTED.
5080

		<i>Kustom.</i>		ELECTRONICS, INC.	
		CHANUTE, KANSAS		66720	
DRN	JLS	DATE	9-72	TOLERANCES	NONE
CHK		DATE		MATERIAL	NONE
ENGR				NAME	
SCALE				LEFT & RIGHT SIDE RAIL	
NONE		SHT	OF	PART NUMBER	
				300-0025-00	



OUTSIDE

B3-C6
SCHEM. 002-0095-02
FREQ. CONTROL LOGIC, L3
SCHEM. 002-5074-00

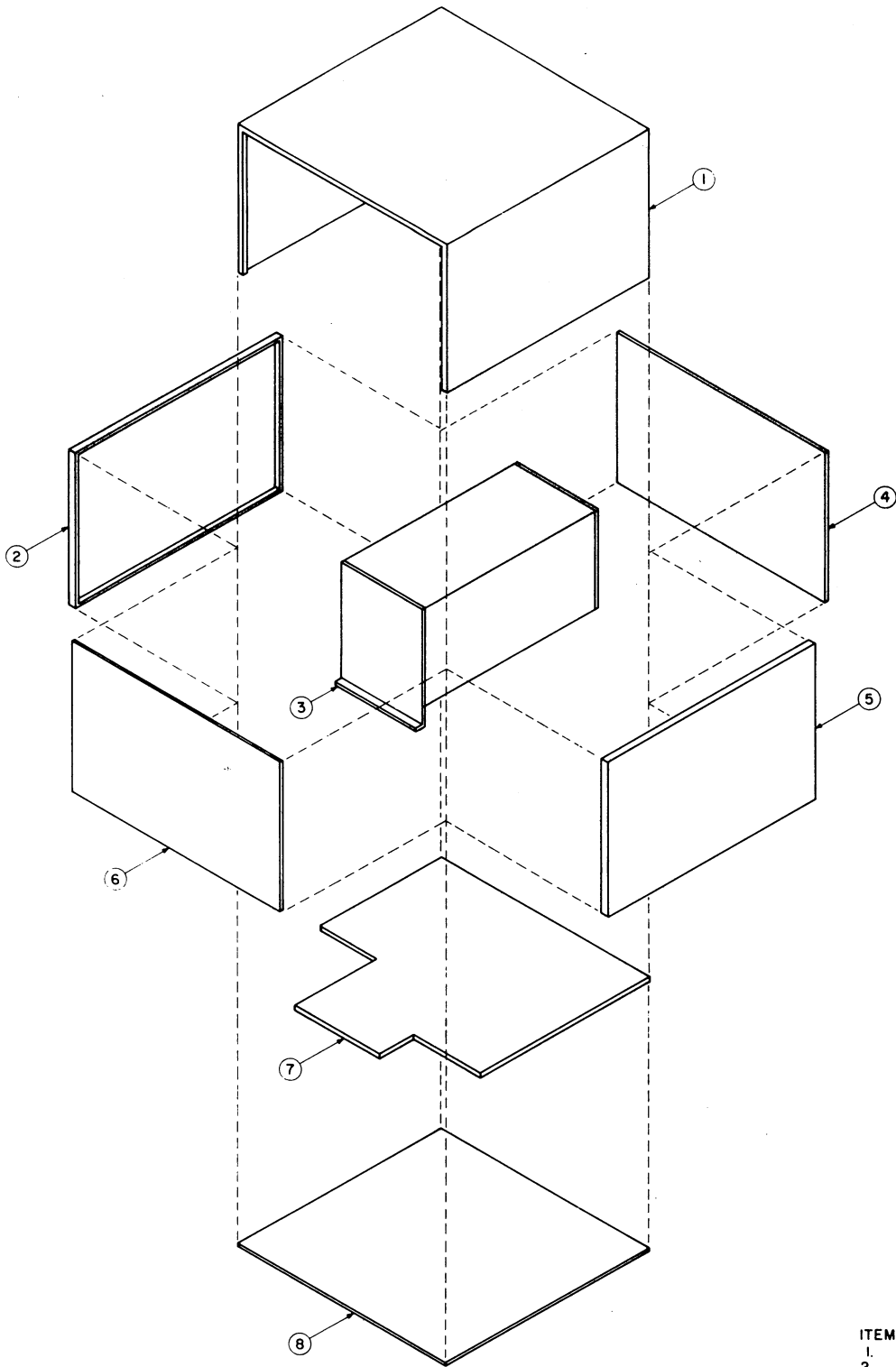


INSIDE

NOTES:

1. FOR COMPONENTS J5, F1, S35, B1, C6, C7, REFER TO SCHEM. 002-0095-00.
2. FOR COMPONENTS B3, Q4, REFER TO SCHEM. 002-0095-02.

				ELECTRONICS, INC. CHANUTE KANSAS 66720	
DRN	JLS	DATE	9-72	TOLERANCES	NONE
CHK		DATE	10-72	MATERIAL	NONE
ENGR		NAME			
SCALE		REAR PANEL			
SHT	OF	PART NUMBER			
NONE	1	300-0026-00			



ITEM	KUSTOM PART NO.
1.	047-0135-01
2.	200-0192-00
3.	200-0183-00
4.	200-0193-00
5.	200-0182-00
6.	200-0194-00
7.	200-0191-00
8.	047-0133-01

Kustom. ELECTRONICS, INC. CHANUTE, KANSAS 66720			
DRN	JLS	DATE 9-72	TOLERANCES NONE
CHK	DATE 10-72	NAME	
SCALE NONE		UNIT ASSEMBLY	
SHT OF 1		PART NUMBER 300-0027-00	

INPUT
PAD, G16
SCHEM.
002-0092-00

ATTENUATOR, G14
SCHEM. 002-0092-00

VFO, G24
SCHEM. 002-~~5077~~-00
5083

RF
MODULATOR,
G10
SCHEM.
002-~~5064~~-00
5076

LEVELING DETECTOR, G17
SCHEM. 002-~~5064~~-00
5076

FREQ. MONITOR, G19
SCHEM. 002-~~5073~~-00
5080

EMI FILTER, G25
SCHEM. 002-~~5064~~-00
5076

MASTER
VCO, G7
SCHEM.
002-5081-01

MODULATOR, G18
SCHEM. 002-~~5064~~-00
5076

LOW LOOP BOARD, G1
SCHEM. 002-~~5077~~-00
5083

-ΔF VCO, G6
SCHEM.
002-5081-00

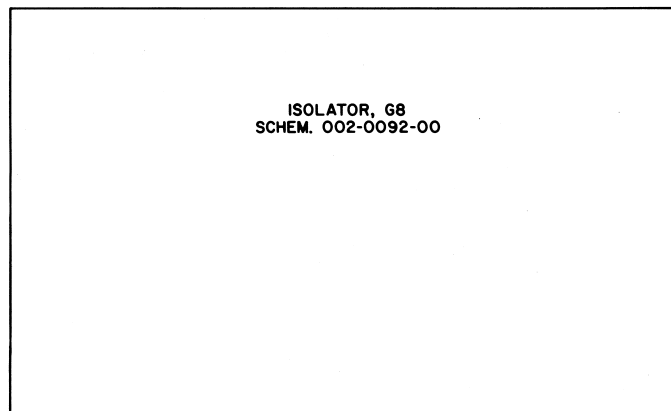
HIGH LOOP BOARD, G4
SCHEM. 002-5078-00

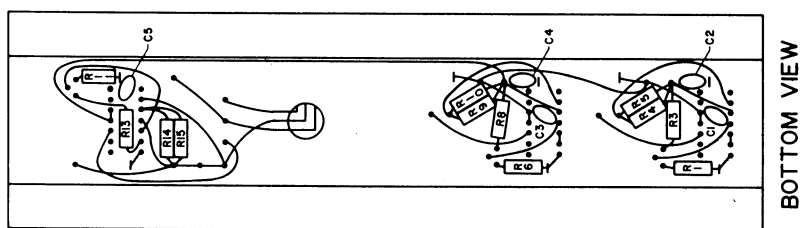
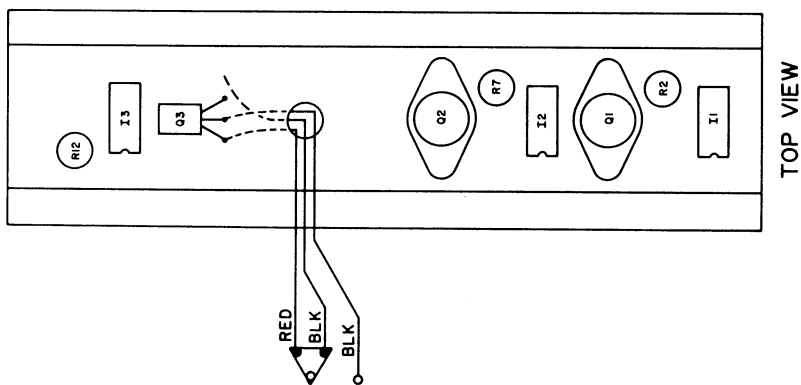
+ΔF VCO, G5
SCHEM.
002-5081-00

89 MHz OSC., G3
SCHEM. 002-5082-01

91 MHz OSC., G2
SCHEM. 002-5082-00

REV. C		NO		DATE		BY		Kustom. ELECTRONICS, INC. CHANUTE, KANSAS 66720	
DRN		JLS		DATE		TOLERANCES		MATERIAL	
CHK		DATE		7-72		NONE		NONE	
ENGR		DATE				NAME		INTERMEDIATE PLATE, BOTTOM SIDE	
SCALE		SHT		1		PART NUMBER			
NONE		OF		2		300-0023-00			

[illegible]

[illegible]

PARTS LIST

ASSEMBLY NO:	200-0194-00
DESCRIPTION:	FRONT PANEL SUB-ASSY
ASSY DWG NO:	300-0024-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
CR1	DIODE 1N4148	007-6016-00
DS1	LENS PUSHBUTTON PWR-CAL	037-0038-00
DS2	LENS PUSHBUTTON PWR-CAL	037-0038-00
DS3	LENS INDICATOR PPS	037-0008-02
DS4	LENS INDICATOR FPS	037-0008-03
DS5	LENS INDICATOR KTS	037-0008-04
DS6	LENS INDICATOR NMI	037-0008-01
DS7	LENS INDICATOR RMT	037-0008-06
DS8	LENS INDICATOR MHZ	037-0008-07
DS9	LENS INDICATOR %	037-0008-05
DS10	LENS INDICATOR WTS	037-0008-08
DS11	LENS INDICATOR -1 NMI	037-0008-00
G14	VARIABLE ATTENUATOR	015-0006-00
J6-J10	CONNECTOR BNC PANEL MTG	030-0034-00
R1	RESISTOR POT 1K	133-0047-00
R2	RESISTOR POT 1K	133-0047-00
R3/S4	RESISTOR POT 1K W/2 POS SWITCH	133-0049-00
R4/S15	RESISTOR POT 1K W/2 PCS SWITCH	133-0049-00
R5/6	RESISTOR POT 1K CONC	133-0046-00
R7/8	RESISTOR POT 1K CONC	133-0046-00
R9/S20	RESISTOR POT 1K W/3 POS SWITCH	133-0048-00
R10/S21	RESISTOR POT 1K W/2 PCS SWITCH	133-0049-00
R11/S22	RESISTOR POT 1K W/2 POS SWITCH	133-0049-00
R12-R16	RESISTOR F/C 1K 1/4W 10%	129-0102-25
R17	RESISTOR F/C 100 OHM 1/4W 10%	129-0101-25
S1-S3	SWITCH TOGGLE DPDT ON/OFF	031-0036-00
S5	SWITCH ROTARY 9 POSITION	031-0028-00
S6	SWITCH PUSHBUTTON RED	031-0030-00
S7	SWITCH PUSHBUTTON BLACK	031-0030-01
S8	SWITCH PUSHBUTTON BLACK	031-0030-01
S9-S11	SWITCH PUSHBUTTON RESET	031-0029-00
S12-S14	SWITCH TOGGLE DPDT ON/OFF	031-0036-00
S16	SWITCH ROTARY 9 POSITION	031-0026-00
S17	SWITCH TOGGLE DPDT ON/OFF	031-0036-00
S18	SWITCH TOGGLE DPDT ON/OFF	031-0036-00
S19	SWITCH TOGGLE SPST ON/OFF	031-0036-01
S23	SWITCH ROTARY 11 POSITION	031-0027-00
S24	SWITCH PUSHBUTTON CAL-PWR	031-0037-00
S25	SWITCH PUSHBUTTON CAL-PWR	031-0037-00
S26-S29	SWITCH ROTARY RF GEN	031-0017-00
S30-S34	SWITCH ROTARY VIDEO GEN	031-0016-00
	3/8 GROUND LUG	008-0012-00
	WIRE 26 GA TFE CW BLK	025-0006-00
	WIRE 26 GA TFE CW RED	025-0006-22
	WIRE 26 GA TFE CW YEL/BLK	025-0006-40
	WIRE 26 GA TFE CW WHT	025-0006-99
	BUSS WIRE #24	025-1001-00
	BULB T 1 3/4	037-0006-00
	BASE INDICATOR	037-0007-00
	FRONT PANEL	047-0128-00
	PLATE W/PAINT	047-0174-02

200-0194-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
	SPACER 4-40 X .5	076-0001-08
	KNOB 1.750 DIA	076-0031-00
	KNOB SPINNER	076-0032-00
	KNOB POINTER	076-0033-00
	KNOB CONC POINTER	076-0033-01
	KNOB W/INDICATOR	076-0034-00
	SPACER	076-0039-00
	LENS	087-1037-00
	NUT 2-56	089-2004-21
	NUT HEX 6-32 KEPS	089-2062-21
	SCREW PHP 2-56 X 1/4	089-5054-04
	SCREW PHP 6-32 X 3/8	089-5062-06
	SCREW FHP 8-32 X 1/2	089-5164-08
	SCREW PHP 4-40 X 3/8 BLK	089-5704-06
	SCREW PHP 6-32 X 5/8 BLK	089-5708-10
	WASHER INT TOOTH #2	089-8500-00

ASSEMBLY NO:	200-0192-00
DESCRIPTION:	LEFT SIDE RAIL SUB-ASSY
ASSY DWG NO:	300-0025-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C2-C5	CAPACITOR ELECT 1900 UF 40V	095-0015-03
CR1	RECTIFIER 10A	007-6018-00
CR2	RECTIFIER 10A	007-6018-00
	LUG GND #6	008-0000-00
	TERMINAL STANDOFF	010-0007-01
	WIRE 22 GA TFE YEL	025-0003-04
	WIRE 26 GA TFE CW BRN	025-0006-11
	WIRE 26 GA TFE CW GRN	025-0006-55
	WIRE 26 GA TFE CW BLU	025-0006-66
	COVER METAL DUST	040-0001-00
	PANEL LEFT SIDE	047-0140-01
	COVER SPACER W/CL IRIDITE	047-0141-01
	REG BRKT W/HDW	047-0215-04
	HANDLE	073-0023-02
	MTG BRACKET HANDLE	073-0028-02
	COVER MTG BRACKET	073-0030-02
	NUT HEX 6-32 KEPS	089-2062-21
	NUT FLOATING 10-32	089-2500-26
	SCREW PHP 6-32 X 3/8 SEMS	089-5028-06
	SCREW PHP 8-32 X 1/2	089-5064-08
	SCREW FHP 6-32 X 3/8	089-5162-06
	CLIP COMPONENT	090-0043-01
	POP RIVET 3/32 DIA	092-0000-32
	POP RIVET 1/8 AD-42-ABS	092-0000-42
	SELF CLINCH FAST 6-32	092-0003-14
	SELF CLINCH FAST 8-32	092-0003-18

ASSEMBLY NO:	200-0182-00
DESCRIPTION:	RIGHT SIDE RAIL SUB-ASSY
ASSY DWG NO:	300-0025-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
CR3	RECTIFIER 25A	007-6019-00
G20	10 DB PAD	015-0004-00
G21	DETECTOR	015-0010-00
G22	ULTIMATE LOW-PASS FILTER	200-0196-00
T2	TRANSFORMER 115V/26V	019-7019-00
	LUG GND #6	008-0000-00
	COAX SEMI RIGID UT-141-A	024-0002-00
	JACK STRAIGHT CABLE	030-0010-00
	PLUG STRAIGHT CABLE	030-0011-00
	COVER MTL DUST	040-0001-00
	COVER SPACER W/CL IRIDITE	047-0141-01
	PANEL RS	047-0225-01
	CLAMP COMPONENT	047-0230-01
	HANDLE	037-0023-02
	MTG BRACKET HANDLE	073-0028-02
	COVER MTG BRACKET	073-0030-02
	SPACER 6-32 X .75	076-0001-09
	NUT HEX 6-32 KEPS	089-2062-21
	NUT FLOATING 10-32	089-2500-26
	NUTSERT 6-32	089-2522-01
	SCREW PHP 6-32 X 3/8 SEMS	089-5028-06
	SCREW PHP 6-32 X 5/16	089-5062-05
	SCREW PHP 8-32 X 1/2	089-5064-08
	SCREW FHP 6-32 X 3/8	089-5162-06
	POP RIVET 3/32 DIA	092-0000-32
	SELF CLINCH FAST 8-32	092-0003-18

ASSEMBLY NO:	200-0193-00
DESCRIPTION:	REAR PANEL SUB-ASSY
ASSY DWG NO:	300-0026-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C6 (B3)	CAPACITOR ELECT 1900 UF 40V	095-0015-03
C6	CAPACITOR D/C 3.3 PF NPO 5%	110-0030-04
C7	CAPACITOR D/C 3.3 PF NPO 5%	110-0030-04
F1	FUSE 3 AMP MDX	036-0004-05
FAN	FAN WS 2107F-2	148-0000-00
J5	PLUG AC	030-2032-00
J12	CONNECTOR BNC PANEL MTG	030-0034-00
Q4	TRANSISTOR 2N3771	007-0033-00
S35	SWITCH 115V/230V	031-0014-00
	LUG GND #6	008-0000-00
	WIRE 22 GA TFE RED	025-0003-02
	WIRE 22 GA TFE YEL	025-0003-04
	WIRE 26 GA TFE CW ORN	025-0006-33
	WIRE 26 GA TFE CW YEL/BLK	025-0006-40
	REG BRKT W/HDW	047-0215-04
	PANEL REAR	047-0224-01
	HEAT SINK	047-5037-01
	SERIAL NO TAG	057-1061-00
	SPACER	076-0018-00
	NUT HEX #4-40 KEPS	089-2058-21
	NUT HEX #6-32 KEPS	089-2062-21
	NUT HEX #10-32 KEPS	089-2065-21
	SCREW PHP 4-40 X 3/8 SEMS	089-5026-06
	SCREW PHP 6-32 X 1/2	089-5062-08
	SCREW PHP 6-32 X 3/4	089-5062-12
	SCREW FHP 6-32 X 3/8	089-5162-06
	SCREW OHP 10-32 X 7/8	089-5265-14
	MICA WASHER	090-0003-00
	SHOULDER WASHER	090-0004-00
	COVER TO-3	090-0034-00
	CLIP COMPONENT	090-0043-01
	FUSE HOLDER	090-0080-00
	PLUG-CORD ASSY	090-0112-00
	POP RIVET 1/8 AD-42-ABS	092-0000-42
	POP RIVET 1/8 DIA F H	092-0009-01
	FILTER FAN	148-0001-01
	SCREEN FAN	148-0002-01

ASSEMBLY NO:	200-0191-00
DESCRIPTION:	INTERMEDIATE PLATE SUB-ASSY
ASSY DWG NO:	300-0023-00/01

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR ELECT 9000 UF 50V	095-0014-02
G8	ISOLATOR SUB ASSY	200-0691-00
G9	LOW PASS FILTER	017-0001-00
G11	LOW PASS FILTER	017-0000-00
G12	DIRECTIONAL COUPLER	015-0005-00
G13	SNIFFER SUB-ASSY	200-0188-00
G15	DIRECTIONAL COUPLER	015-0005-00
G16/J11	COAXIAL ATTENUATOR	015-0008-00
G17	DETECTOR	015-0010-00
G25	EMI FILTER SUB-ASSY	200-0256-00
T1	TRANSFORMER 110/220V	019-7018-00
	LUG GND #6	008-0000-00
	COAX RG-188 AU	024-0001-00
	COAX SEMI RIGID UT-141-A	024-0002-00
	WIRE 22 GA TFE BLK	025-0003-00
	WIRE 22 GA TFE RED	025-0003-02
	WIRE 22 GA TFE ORN	025-0003-03
	WIRE 22 GA TFE YEL	025-0003-04
	WIRE 26 GA TFE CW BRN	025-0006-11
	WIRE 26 GA TFE CW RED	025-0006-22
	WIRE 26 GA TFE CW ORN	025-0006-33
	WIRE 26 GA TFE CW GRN	025-0006-55
	WIRE 26 GA TFE CW BLU	025-0006-66
	WIRE 26 GA TFE CW GRY	025-0006-88
	WIRE 26 GA TFE CW WHT	025-0006-00
	CABLE ASSY	030-0007-00
	JACK STRAIGHT CABLE	030-0010-00
	PLUG STRAIGHT CABLE	030-0011-00
	JACK STRAIGHT CABLE	030-0015-00
	PLUG STRAIGHT CABLE	030-0016-00
	PLATE COUPLER W/IRIDITE	047-0228-02
	CLAMP COMPONENT	047-0230-01
	PLATE ISOLATOR	047-0231-01
	COVER VCO W/IRIDITE	047-0232-02
	COVER RF SWITCH W/IRIDITE	047-0233-02
	SPACER PLATE W/ IRIDITE	047-0409-02
	SPACER PLT XFORMER W/IRIDITE	047-0441-02
	PLATE INTERMEDIATE	047-5033-01
	SPACER	076-0039-01
	SPACER	076-0039-02
	SPACER	076-0039-03
	SPACER	076-0039-04
	SCREW PHS 6-32 X 1 1/2	089-5012-24
	SCREW PHP 4-40 X 5/8 SEMS	089-5026-10
	SCREW PHP 6-32 X 1/4 SEMS	089-5028-04
	SCREW PHP 6-32 X 3/8 SEMS	089-5028-06
	SCREW PHP 8-32 X 1/4 SEMS	089-5030-04
	SCREW PHP 2-56 X 1/4	089-5054-04

200-0191-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
	SCREW PHP 2-56 X 5/8	089-5054-10
	SCREW 4-40 X 1 PP	089-5058-16
	SCREW PHP 6-32 X 5/16	089-5062-05
	SCREW PHP 6-32 X 1/2	089-5062-08
	SCREW FHP 10-32 X 3/4 NLS	089-5538-00
	SCREW FHP 4-40 X 5/16	089-5827-05
	WASHER INT TOOTH #2	089-8500-00
	CLAMP PORT 2 1/2 IN	090-0007-00
	CLIP COMPONENT	090-0043-03
	RIVET 1/8 DIA X 3/8 LG	092-0005-46
	RIVET 1/8 DIA X 7/16 LG	092-0005-47
	RECEPTACLE SOUTHCO	092-0013-00

ASSEMBLY NO:	200-0197-00
DESCRIPTION:	REG S-ASY -5+28-28-10+16 (B2)
ASSY DWG NO:	300-0095-01

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C2	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C3	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C4	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C5	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C6	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C7	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C8	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C9	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C10	CAPACITOR D/C .001 UF Z5F 20%	109-1021-16
C11	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C12	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C13	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
CR1	DIODE ZENER 1N4753	007-5079-25
I1	IC 723 UT	007-7013-01
I2-I4	VT IC LM304H	007-7043-01
I5	IC 723 UT	007-7013-01
Q1	TRANSISTOR 2N4922	007-0030-00
Q2-Q4	TRANSISTOR 2N4919	007-0029-00
Q5	TRANSISTOR 2N4922	007-0030-00
R1	RESISTOR F/C 270 OHM 1/2W 10%	130-0271-15
R2	RESISTOR PREC 1.82K 1/8W 1%	125-1821-01
R3	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R4	RESISTOR PREC 4.99K 1/8W 1%	125-4991-01
R5	RESISTOR F/C 1.3 OHM 1/2W 5%	129-0013-13
R6	RESISTOR F/C 2.2K 1/8W 10%	130-0222-05
R7	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R8	RESISTOR F/C 10K 1/4W 10%	130-0103-25
R9	RESISTOR F/C 1.3 OHM 1/2W 5%	129-0013-13
R10	RESISTOR F/C 2.2K 1/8W 10%	130-0222-05
R11	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R12	RESISTOR F/C 2.2K 1/4W 10%	130-0222-25
R13	RESISTOR F/C 1.3 OHM 1/2W 5%	129-0013-13
R14	RESISTOR F/C 2.2K 1/8W 10%	130-0222-05
R15	RESISTOR POT 5K TYPE SV 1 TURN	133-0042-10
R16	RESISTOR F/C 1.3 OHM 1/2W 5%	129-0013-13
R17	RESISTOR PREC 10K 1/8W 1%	125-1002-01
R18	RESISTOR PREC 14K 1/8W 1%	125-1402-01
R19	RESISTOR F/C 1.3 OHM 1/2W 5%	129-0013-13
	GND TERMINAL #2X.531	008-0017-02
	LUG #2	008-0018-00
	TERMINAL FEEDTHRU	010-0008-01
	WIRE 26 GA TFE CW BRN	025-0006-11
	WIRE 26 GA TFE CW ORN	026-0006-33
	WIRE 26 GA TFE CW YEL/BLK	025-0006-40
	WIRE 26 GA TFE CW YEL	025-0006-44
	WIRE 26 GA TFE CW GRN	025-0006-55
	WIRE 26 GA TFE CW GRY	025-0006-88
	IC SOCKET	033-0002-00
	SOCKET TRANSISTOR	033-0003-00

200-0197-00

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
	IC SOCKET 10 PIN RD	033-0004-00
	HEAT SINK	047-5032-01
	NUT 2-56	089-2004-21
	NUT HEX #4-40 KEPS	089-2058-21
	SCREW PHP 2-56 X 1/4	089-5054-04
	SCREW PHP 4-40 X 7/16	089-5058-07
	WASHER INT TOOTH #2	089-8500-00
	SHOULDER WASHER	090-0004-00
	SPAGHETTI TUBING 22 AWG	150-0001-04

ASSEMBLY NO:	200-0198-00
DESCRIPTION:	REG S-ASSY +5+16+10 (B3)
ASSY DWG NO:	300-0095-02

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>KPN</u>
C1	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C2	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C3	CAPACITOR D/C .01 UF Z5V 20%	109-1030-46
C4	CAPACITOR TANT 6.8 UF 35V 20%	096-1007-29
C5	CAPACITOR D/C .01 UF 35V 20%	109-1030-46
I1-I3	IC 723	007-7013-00
Q1	TRANSISTOR NPN 2N3054	007-0032-00
Q2	TRANSISTOR NPN 2N3054	007-0032-00
Q3	TRANSISTOR 2N4922	007-0030-00
R1	RESISTOR PREC 2.05K 1/8W 1%	125-2051-01
R2	RESISTOR POT 1K TYPE SV	133-0042-07
R3	RESISTOR F/C 2.7K 1/4W 10%	129-0272-25
R4	RESISTOR F/C 1.3 OHM 1/2W 5%	129-0013-13
R5	RESISTOR F/C 1.3 OHM 1/2W 5%	129-0013-13
R6	RESISTOR PREC 2.21K 1/8W 1%	125-2211-01
R7	RESISTOR POT 1K TYPE SV	133-0042-07
R8	RESISTOR F/C 1K 1/4W 10%	129-0102-25
R9	RESISTOR F/C 1.3 OHM 1/2W 5%	129-0013-13
R10	RESISTOR F/C 1.3 OHM 1/2W 5%	129-0013-13
R11	RESISTOR F/C 1.8K 1/4W 10%	130-0182-25
R12	RESISTOR POT 1K TYPE SV	133-0042-07
R13	RESISTOR F/C 470 OHM 1/4W 10%	129-0471-25
R14	RESISTOR WIRE WOUND	132-0011-04
R15	RESISTOR WIRE WOUND	132-0011-04
	LUG GND #6	008-0000-00
	LUG #2	008-0018-00
	TERMINAL FEEDTHRU	010-0008-01
	WIRE 26 GA TFE CW BLK	025-0006-00
	WIRE 26 GA TFE CW RED	025-0006-22
	IC SOCKET	033-0002-00
	SOCKET TRANSISTOR	033-0003-00
	HEAT SINK	047-5031-01
	NUT 2-56	089-2004-21
	NUT HEX #4-40 KEPS	089-2058-21
	SCREW PHP 6-32 X 1/4 SEMS	089-5028-04
	SCREW PHP 2-56 X 1/4	089-5054-04
	SCREW PHP 4-40 X 7/16	089-5058-07
	SOCKET TRANSISTOR	090-0001-00
	MICA WASHER	090-0003-01
	SHOULDER WASHER	090-0004-00
	SPAGHETTI TUBING 22 AWG	150-0001-04

WIRE LIST

White, Type #26CW

WIRE NO.	FROM	TO	WIRE NO.	FROM	TO
1	J1-C	S12-1	25	J1- <u>g</u>	S10-1
2	J1-D	S23A-10	26	J1-h	S11-1
3	J1-E	S23B-11	27	G7-1	G4-3
4	J1-F	S23C-8	28	J1- <u>j</u>	L3-53
5	J1-G	S23C-11	29	J1- <u>k</u>	L3-62
6	J1-H	L2-115	30	J1- <u>m</u>	L3-65
7	J1-J	L2-106	31	J1- <u>n</u>	L3-63
8	J1-K	L2-91	32	J1- <u>p</u>	L3-66
9	J1-L	L2-82	33	J1-q	L3-64
10	J1-M	L2-86	34	J1- <u>r</u>	L3-68
11	J1-N	L2-89	35	J1- <u>s</u>	L3-69
12	J1-P	L2-67	36	J1- <u>t</u>	L3-70
13	J1-R	L2-58	37	J1- <u>u</u>	L3-71
14	J1-S	L2-62	38	J1- <u>v</u>	L3-67
15	J1-T	L2-65	39	J1- <u>w</u>	L3-74
16	J1-U	L2-79	40	J1- <u>x</u>	L3-72
17	J1-V	L2-70	41	J1- <u>y</u>	C9-B31
18	J1-W	L2-74	42	J1- <u>z</u>	C9-A29
19	J1-X	L2-77	44	J1-BB	C9-B22
20	J1-Y	L2-103	46	J1-DD	C9-B23
21	J1-Z	L2-94	48	J1-HH	S19-3
22	J1- <u>a</u>	L2-98	49	J1- <u>c</u>	S6-1
23	J1- <u>b</u>	L2-101	50	J1- <u>d</u>	S7-1
24	J1- <u>f</u>	S9-1	51	J1- <u>e</u>	S8-1

52	J2-D	L1-39	75	J2- <u>m</u>	S16A-9
53	J2-E	C6-B17	76	J2- <u>n</u>	S16B-7
54	J2-F	S17-3	77	G23-9	G22-2
55	J2-G	S17-1	77	J2- <u>p</u>	S16B-9
56	J2-H	S18-3	78	J2- <u>q</u>	L1-38
57	J2-J	S18-1	79	J2- <u>r</u>	L1-40
58	J2-U	S5-3	80	J2- <u>s</u>	L1-41
58	G5-1	G6-1	81	J2- <u>t</u>	L1-47
59	J2-V	S5-5	82	J2- <u>u</u>	L1-48
60	J2-W	S5-6	83	J2- <u>v</u>	L1-42
61	J2-X	S5-8	84	J2- <u>w</u>	L1-50
62	J2-Y	S5-7	85	J2- <u>x</u>	L1-53
63	J2-Z	S5-2	86	J2- <u>y</u>	L1-52
64	J2- <u>a</u>	S5-9	87	J2- <u>z</u>	L1-49
65	J2- <u>b</u>	S5-1	88	J2-AA	L1-59
66	J2- <u>c</u>	L1-43	89	J2-BB	L1-56
67	J2- <u>d</u>	L1-45	90	J2-CC	L1-57
68	J2- <u>e</u>	L1-51	91	J2-DD	L1-58
69	J2- <u>f</u>	S2-1	92	J2-EE	L1-60
70	J2- <u>g</u>	S2-3	93	J2-FF	L1-63
71	J2-h	S12-4	94	J2-GG	L1-62
72	G1-25	G24-5	95	J2-HH	L1-61
72	J2-i	S13-3	96	J3-R	S1-3
73	G1-21	G6-2	97	J3-V	C7-B17
73	J2- <u>j</u>	C10-B29	98	J3-W	J12-1
74	G1-20	G5-2	99	G18-24	G19-7
74	J2-k	L2-19	99	J3-X	C8-B10

100	J3- <u>c</u>	S16A-1	132	J4- <u>S</u>	C10-B31
101	J3- <u>d</u>	C10-A9	133	J4-T	C10-A2
102	J3- <u>e</u>	C11-B11	136	J4-Y	C10-A8
103	J3- <u>f</u>	S4-7	139	J4- <u>b</u>	C11-B30
104	J3- <u>g</u>	C11-B20	141	L1-1	1 MSD-8
105	J3- <u>h</u>	C11-B3	142	L1-2	1 MSD-7
106	J3- <u>i</u>	G18-5	143	L1-3	1 MSD-10
107	J3- <u>j</u>	G18-6	144	L1-4	1 MSD-13
108	J3- <u>k</u>	S16B-6	145	L1-5	1 MSD-1
109	J3- <u>m</u>	S16B-5	146	L1-6	1 MSD-11
111	J3- <u>p</u>	S16B-3	147	L1-7	1 MSD-2
112	J3- <u>q</u>	S16B-2	148	L1-8	2 MSD-8
113	J3- <u>r</u>	S16B-1	149	L1-9	2 MSD-7
114	J3- <u>s</u>	C10-B23	150	L1-10	2 MSD-10
115	J3- <u>t</u>	G24-2	151	L1-11	2 MSD-13
116	J3- <u>u</u>	G24-3	152	L1-12	2 MSD-1
117	J3- <u>v</u>	C9-B2	153	L1-13	2 MSD-11
118	J3- <u>w</u>	S20-3	154	L1-14	2 MSD-2
119	J3- <u>x</u>	S20-1	155	L1-15	3 MSD-8
120	J3- <u>y</u>	G18-26	156	L1-16	3 MSD-7
121	J3- <u>z</u>	S21-7	157	L1-17	3 MSD 10
123	J3-EE	S24-5	158	L1-18	3 MSD-13
124	J3-FF	G23-3	159	L1-19	3 MSD-1
125	J3-GG	C6-B20	160	L1-20	3 MSD-11
126	J3-HH	C7-B26	161	L1-21	3 MSD-2
127	J4-B	C10-A6	162	L1-22	4 MSD-8
130	J4-L	C10-A11	163	L1-23	4 MSD-7

164	L1-24	4 MSD-10	191	L1-51	C4-B28
165	L1-25	4 MSD-13	192	L1-52	C4-A30
166	L1-26	4 MSD-1	193	L1-53	C4-A32
167	L1-27	4 MSD-11	194	L1-54	L2-38
168	L1-28	4 MSD-2	196	L1-56	C5-A16
169	L1-29	5 MSD-7	197	L1-57	C5-A17
170	L1-30	5 MSD-8	198	L1-58	C5-A18
171	L1-31	5 MSD-10	199	L1-59	C5-A15
172	L1-32	5 MSD-13	200	L1-60	C6-B36
173	L1-33	5 MSD-1	201	L1-61	C6-B39
174	L1-34	5 MSD-11	202	L1-62	C6-B38
175	L1-35	5 MSD-2	203	L1-63	C6-B37
176	L1-36	3 MSD-6	204	L1-64	L2-55
177	L1-37	4 MSD-6	205	L2-1	S30-C
178	L1-38	C6-A10	206	L2-2	S14-2
179	L1-39	C3-A19	207	L2-3	S17-2
180	L1-40	C6-B5	208	L2-4	S13-2
181	L1-41	C2-A18	209	L2-5	S2-2
182	L1-42	C2-A21	210	L2-6	S1-2
183	L1-43	C3-A17	211	L2-7	S12-4
184	L1-44	L2-37	212	L2-8	S18-2
185	L1-45	C4-B27	213	L2-9	DS3-1
186	L1-46	C3-A18	214	L2-10	S23B-C
187	L1-47	C2-A19	215	L2-11	S23A-C
188	L1-48	C2-A20	216	L2-12	S16B-C
189	L1-49	C4-A33	217	L2-13	DS11-1
190	L1-50	C4-A29	218	L2-14	S16A-C

219	L2-15	S23C-C	246	L2-46	C6-A7
220	L2-16	D S7-1	247	L2-47	S5-6
221	L2-17	S4-6	248	L2-49	DS6-1
222	L2-18	S19-2	249	L2-50	S5-7
223	L2-20	C10-B25	250	L2-52	S5-8
224	L2-21	S15-7	251	L2-53	C4-A15
225	L2-22	S20-C	253	L2-56	S24-4
226	L2-23	DS10-1	254	L2-57	C1-B11
227	L2-24	DS9-1	255	L2-59	S32-B
228	L2-25	S5-3	256	L2-60	C1-B12
229	L2-26	C5-B11	257	L2-61	S32-C
230	L2-27	S21-6	258	L2-63	C1-B13
231	L2-28	S5-C	259	L2-64	S32-D
232	L2-29	S24-2	260	L2-66	C1-B10
233	L2-30	S12-1	261	L2-68	S32-A
234	L2-31	L3-50	262	L2-69	C1-B7
235	L2-32	S5-9	263	L2-71	S33-B
236	L2-33	C11-B23	264	L2-72	C1-B8
237	L2-34	DS8-1	265	L2-73	S33-C
238	L2-35	S5-1	266	L2-75	C1-B9
239	L2-36	C5-B10	267	L2-76	S33-D
240	L2-39	C5-B12	268	L2-78	C1-B6
241	L2-40	S5-2	269	L2-80	S33-A
242	L2-41	DS5-1	270	L2-81	C1-A6
243	L2-42	DS4-1	271	L2-83	S31-B
244	L2-43	S5-5	272	L2-84	C1-A7
245	L2-45	C6-A4	273	L2-85	S31-C

274	L2-87	C1-A8	302	L3-15	S26-1'
275	L2-88	S31-D	303	L3-14	S26-2'
276	L2-90	C1-A5	304	L3-12	C5-B14
277	L2-92	S31-A	305	L3-12	G1-13
278	L2-93	C1-B3	306	L3-11	C5-B15
279	L2-95	S34-B	307	L3-11	G1-14
280	L2-96	C1-B4	308	L3-10	C5-B16
281	L2-97	S34-C	309	L3-10	G1-12
282	L2-99	C1-B5	310	L3-8	C5-B17
283	L2-100	S34-D	311	L3-8	G1-10
284	L2-102	C1-B2	312	L3-6	C5-B19
285	L2-104	S34-A	313	L3-6	G1-9
286	L2-105	C1-A10	314	L3-4	C5-B18
287	L2-107	S30-B	315	L3-4	G1-11
288	L2-111	L2-119	316	L3-37	S29-1
289	L2-113	S24-5	317	L3-51	S29-0
290	L2-114	C1-A9	318	L3-22	S28-C2
291	L2-116	G1-24	319	L3-38	S28-C1
292	L2-117	S30-A	320	L3-49	S29-C
293	L2-118	C5-B36	321	L3-58	S29-2
295	J3-AA	T2-1	322	L3-58	G1-2
296	J3-BB	T2-2	323	L3-59	C5-B25
297	J4-W	T2-4	324	L3-59	G1-3
298	J4-X	T2-3	325	L3-60	C5-B24
299	L2-121	S19-3	326	L3-60	G1-4
300	J3-b	C8-A30	327	L3-9	S27-D
301	L3-13	S26-0'	328	L3-7	S27-C

329	L3-5	S27-B	359	L3-46	S28-8
330	L3-3	S27-A	360	L3-55	S28-7
331	L3-39	C6-B10	361	L3-26	S28-6
332	L3-57	S16B-7	362	L3-44	S28-5
333	L3-52	S16B-9	363	L3-42	S28-4
334	L3-28	C5-B21	364	L3-43	S28-3
335	L3-28	G1-6	365	L3-41	S28-2
336	L3-45	G5-B22	366	L3-23	S28-1
337	L3-45	G1-5	367	L3-40	S28-0
338	L3-18	C5-B23	368	L3-24	S28A
339	L3-18	G1-7	369	L3-17	S28B
340	L3-25	C5-B20	370	L3-54	S28C
341	L3-25	G1-8	371	L3-27	S28D
345	L3-33	S26-3	372	C1-A4	S6-1
346	L3-48	S26-1	373	C1-B32	S11-1
347	L3-36	S26-0	374	C1-B33	S8-1
348	L3-35	S27-8	375	C1-A2	S7-1
349	L3-34	S27-8	376	C2-A3	S10-1
350	L3-31	S27-7	377	C3-B28	S9-1
351	L3-21	S27-6	378	C4-A10	S3-3
352	L3-32	S27-5	379	C5-B26	S18-3
353	L3-30	S27-4	380	C5-B28	S18-1
354	L3-20	S27-3	381	C5-B31	S17-1
355	L3-47	S27-2	382	C5-B33	S17-3
356	L3-29	S27-1	383	C5-B35	G24-4
357	L3-19	S27-0	384	C5-B37	G1-23
358	L3-56	S28-9	385	C6-B9	S19-3

386	C6-B16	S21-7	413	C8-B33	S16B-2
387	C6-B18	S13-1	414	C8-B34	S16B-6
388	C6-B21	G23-4	415	C8-B35	S16B-5
389	C7-A2	G23-2	416	C8-B36	S16B-3
390	C7-A3	S14-3	417	C8-B38	S16A-1
391	C7-B2	J6-1	418	C8-B39	S16B-1
392	C7-B3	S23A-2	419	C9-A2	R9-2
393	C7-B4	S23C-9	420	C9-A7	R1-2
394	C7-B5	S23C-5	421	C9-A18	G18-28
395	C7-B6	S23B-3	422	C9-A24	S1-3
396	C7-B11	R11-2	423	C9-B14	R1-1
397	C7-B12	J9-1	424	C9-B15	R1-3
398	C7-B21	G18-31	425	C10-A10	R2-2
399	C7-B22	G18-32	426	C10-B4	R2-1
400	C7-B23	G18-30	427	C10-B26	G18-14
401	C7-B28	S20-3	428	C10-B30	R4-2
402	C7-B32	G18-34	429	C10-B33	R4-1
403	C7-B37	S16A-7	430	C11-B2	R6-2
404	C7-B39	S14-1	431	C11-A6	R3-2
405	C8-A2	S4-7	432	C11-B19	R5-2
406	C8-A13	S22-7	433	C11-B29	G23-5
407	C8-B11	S13-3	434	C11-B31	S3-1
408	C8-B13	S2-3	435	C11-B32	R6-1
409	C8-B14	S2-1	436	C11-B33	R5-1
410	C8-B24	G18-18	437	C8-A17	G18-9
411	C8-B25	G18-19	438	C8-A16	G18-11
412	C8-B26	G18-17	439	C8-A15	G18-10

440	C5-A24	S5-4
441	C7-B25	S20-1
442	J3-a	G18-4
443	J3-Y	G18-25
444	J3-L	G18-28
445	J3-F	G18-34
446	J2-C	S5-4
448	J3-A	L3-2
449	S1-1	G18-13
450	S12-1	S12-3
451	S12-2	S12-5
453	S16A-1-6	G19-2
454	S16A-7-9	G19-3
455	R7-2	G18-7
456	R7-3	G18-2
457	R8-2	G18-8
458	R8-3	G18-3
459	R10-2	G18-27
460	R10-3	G18-1
462	J2-B	C6-A2
463	J1-B	C6-A11
464	J12-1	C9-B30

W I R E L I S T

Black, Type #22 or #26 (GND)			Red, Type #22 or #26 (+5V) (Cont'd)		
WIRE NO.	FROM	TO	WIRE NO.	FROM	TO
1	J1- <u>i</u>	GND.	3	L3-61	B3-10
2	J1-AA	GND.	41	G1-1	G24-1
3	J1-EE	GND.	42	DS-7	S24-1
4	J3-DD	GND.	52	G18-21	G19-8
5	J4-C	GND.	39	G4-1	G1-1
6	J4-M	GND.	40	G1-1	G18-21
7	J4-U	GND.			
8	J4-V	GND.	Orange, Type #26 CW (+16V)		
9	J4-Z	GND.	344	L3-73	B3-14
10	J4- <u>a</u>	GND.	465	C7-A37	B3-14
11	J4- <u>c</u>	GND.		C9-A37	B3-14
12	J1-CC	GND.		C10-A37	B3-14
13	L2-120	GND.		C11-A37	B3-14
14	L3-16	GND.	42	G1-15	B3-14
15	S12-2	GND.	43	G1-15	G2-1
16	L1-GND	R3-1	44	G2-1	G3-1
17	C1 thru C11 A1-B1	GND.	45	G1-15	G18-23
Red, Type #22 or #26 (+5)			46	G18-23	G19-1
37	B3-10	G23-1	47	G1-15	G24-6
38	B3-10	G4-1			
4	B3-10	C1 thru C11 A40,B40	Blue, Type #26 CW (+25V, +35V)		
			59	B2-13	G5-3
1	L1-55	B3-10	60	G5-3	G6-3
2	L2-54	B3-10	470	B1-8	C9-A39
					C11-A39

W I R E L I S T

Green, Type #26 CW (+28V)

WIRE NO.	FROM	TO
48	B2-9	G4-2
469	C9-A38	B2-9
	C10-A38	B2-9
	C11-A38	B2-9

Yellow/Black, Type #26 CW (cont.)

WIRE NO.	FROM	TO
468	C9-A36	B3-12
	C10-A36	B3-12
	C11-A36	B3-12

Brown, Type #26 CW (-10V)

WIRE NO.	FROM	TO
53	B2-5	G23-6
54	B2-5	G18-29
466	C9-A34	B2-5
	C10-A34	B2-5
	C11-A34	B2-5

CO-AX, Type RG188U

WIRE NO.	FROM	TO
51	B2-7	G7-2
57	B2-2	G5-1
62	G23-10	J10 -1
63	G18-33	J7-1
64	G19-4	J8-1
66	G2-2	G5-4
65	G3-2	G6-4
68	G2-3	G1-19
67	G3-3	G1-17
69	G5-6	G4-6
70	G6-6	G4-4
71	G1-22	G4-5
92	G13-3	G19-6
1	G18-15	G10-4

Gray, Type #26 CW (-5V)

WIRE NO.	FROM	TO
55	B2-4	G23-8
56	B2-4	G1-18
61	G1-18	G18-16
467	C10-A35	B2-4
	C11-A35	B2-4

Yellow/Black, Type #26 CW (+10V)

WIRE NO.	FROM	TO
49	B3-12	G23-7
50	B3-12	G18-22
447	B3-12	R2-3

W I R E L I S T

Yellow, Type #22 GA.

WIRE NO.	FROM	TO	WIRE NO.	FROM	TO
1	J5-1	B1-T1-4	23	B1-C2(+)	GND.
2	FAN-2	B1-T1-4	24	B1-CR2-4	B1-C3(+)
3	J5-2	GND.	25	B1-C3(+)	B2-13
4	J5-3	S25-5	26	B1-C3(-)	GND.
5	B1-F1-1	S25-2	27	B1-CR3-1	B1-T1-7
6	B1-F1-2	B1-S35-1	28	B1-CR3-3	B1-T1-8
7	B1-S35-1	B1-T1-1	29	B1-CR3-4	B1-C1 (+)
8	B1-S35-5	B1-T1-3	30	B1-CR3-4	B1-11
9	B1-S35-2	B1-T1-2	31	B1-C1(-)	GND.
10	FAN-1	B1-T1-2	32	B3-C6 (+)	B3-10
11	B1-CR1-1	B1-T1-5	33	B3-C6 (-)	GND.
12	B1-CR1-3	B1-T1-6	34	B1-T1-4	DS2-1
13	B1-CR1-2	B1-6	35	B1-T1-2	DS2-4
14	B1-C4(-)	B1-6	36	B1-T1-11	GND.
15	B1-C4(+)	GND.	75	J5-1	B1-S35-4
16	B1-CR1-4	B1-8	76	B2-13	B3-13
17	B1-C5(+)	B1-8	77	B1-3	B2-3
18	B1-C5(-)	GND.	78	B1-8	B2-8
19	B1-CR2-1	B1-T1-9	79	B1-6	B2-6
20	B1-CR2-3	B1-T1-10	80	B1-11	B3-11
21	B1-CR2-2	B1-3			
22	B1-C2(-)	B1-3			

W I R E L I S T

CO-AX, Type UT141

WIRE NO.	FROM	TO
79	G7-5	G5-5
80	G7-4	G6-5
81	G7-3	G8-1
82	G7-6	G19-5
83	G8-2	G9-1
84	G9-2	G10-1
85	G10-2	G11-1
88	G11-2	G12-1
89	G12-2	G13-1
90	G12-4	G17-1
93	G13-2	G14-1
94	G14-2	G15-4
95	G15-1	G16-1
96	G15-2	G20-1
97	G20-2	G21-1
98	G21-2	G22-1

SECTION VI

REMOTE CONTROL INDEX

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REMOTE CONTROL

OPERATION

By means of the Remote Control Jacks, J1, J2 and J3, all control functions on the Test Set Front Panel are remotored with the following exceptions:

1. Attenuator
2. CW Output
3. Serial Data Output Dash
4. Serial Data Output Blank
5. Sync Output
6. Analog P.P.
7. Calibration Phase
8. Calibration 1.0/1.45 usec

The manual Attenuator used in the Test Set can be replaced by a Step Attenuator which may be controlled remotely via Remote Control Jack, J2.

When the Local/Remote Control of the Test Set is placed in the All Remote position all Test Set Controls are remotored, including Frequency Control. When in the Freq. Sel. Remote position Freq. Control only is remotored.

When the Remote/Local Control on the Test Set is placed in the All Remote position control via the Test Set Controls is removed for all Key A (see Remote Control Jack Pin Assignment lists) functions. However, when placed in Local position a Remote input may interfere with Local Control. The Key A input/outputs TTL levels and TTL voltage/current rules should be observed.

When in the All Remote Mode the Test Set frequency is remotored also via Remote Control Jack, J1. There is no interference by Remote Freq. Selector inputs with Local Freq. Control when in Local Mode.

All Key B remote input functions are remotored by forcing a voltage on the input which overrides the Test Set Control. A remote input will interfere with Local Control. The input impedance on the Key B inputs is 1000 ohms or greater.

All Key C input/outputs levels are per ARINC Characteristic 568.

All Key T input/outputs are TTL levels and are for use with a TACAN Adaptor.

Reference should be made to Figure 2 of the operations portion of this manual for REMOTE CONTROL JACK call outs.

PIN ASSIGNMENT

REMOTE CONTROL JACK J1

TYPE BTO2A-22-55S MATING CONNECTOR TYPE BTO6AC-22-55P

PIN	DESCRIPTION	KEY
A.	Attenuator Load	A
B.	P1-P2 Spacing Over-ride	A
C.	Remote Freq. Control	A
D.	DME % Reply A	A
E.	DME % Reply B	A
F.	DME % Reply C	A
G.	DME % Reply D	A
H.	Reg. Load Value A10000	A
J.	Reg. Load Value B10000	A
K.	Reg. Load Value A1000	A
L.	Reg. Load Value B1000	A
M.	Reg. Load Value C1000	A
N.	Reg. Load Value D1000	A
P.	Reg. Load Value A100	A
R.	Reg. Load Value B100	A
S.	Reg. Load Value C100	A
T.	Reg. Load Value D100	A
U.	Reg. Load Value A10	A
V.	Reg. Load Value B10	A
W.	Reg. Load Value C10	A
X.	Reg. Load Value D10	A
Y.	Reg. Load Value A1	A
Z.	Reg. Load Value B1	A
a.	Reg. Load Value C1	A
b.	Reg. Load Value D1	A

J1 Cont'd

PIN	DESCRIPTION	KEY
c.	Distance Register Load	A
d.	Velocity Register Load	A
e.	Acceleration Register Load	A
f.	Distance Register Clear	A
g.	Velocity Register Clear	A
h.	Acceleration Register Clear	A
i.	Freq. Select Common	C
j.	.01 MHz C Freq. Selector	C
k.	0.1 " A " "	C
m.	" " B " "	C
n.	" " C " "	C
p.	" " D " "	C
q.	" " E " "	C
r.	1.0 " A " "	C
s.	" " B " "	C
t.	" " C " "	C
u.	" " D " "	C
v.	" " E " "	C
w.	10 " A " "	C
x.	" " E " "	C
y.	DME U.T. Flag Alarm	C
z.	DME U.T. Serial BCD Distance Data Hi	C
AA	" " " " " " Lo	C
BB	" " " " Clock Hi	C
CC	" " " " " Lo	C
DD	" " " " Word Sync Hi	C

J1 Cont'd

PIN	DESCRIPTION	KEY
EE	DME U.T. Serial BCD Word Sync Lo	C
FF		
GG		
HH	-1 Nautical Mile	A

KEY

A = TTL Level

B = 0-10 V Analog

C = ARINC Level

T = Used with TACAN Adaptor

REMOTE CONTROL JACK J2 PIN ASSIGNMENT

TYPE BTO2A-22-55SW MATING CONNECTOR BTO6AC-22-55PW

PIN	DESCRIPTION	KEY
A.	Attenuator Readout -100's	A
B.	Data Strobe	A
C.	Readout Select-Interro. Rate	A
D.	Readout Overrange	A
E.	Analog Distance Pulse Trig	A
F.	Direction Control Inbound	A
G.	Direction Control Outbound	A
H.	Velocity Control Increase	A
J.	Velocity Control Decrease	A
K.	Readout 1's A	A
L.	Readout 1's B	A
M.	Readout 1's C	A
N.	Readout 1's D	A
P.	Readout 10's A	A
R.	Readout 10's B	A
S.	Readout 10's C	A
T.	Readout 10's D	A
U.	Readout Select-Squitter Rate	A
V.	Readout Select Acceleration	A
W.	Readout Select Velocity	A
X.	Readout Select Measured Distance	A
Y.	Readout Select Test Distance	A
Z.	Readout Select ΔF	A
a.	Readout Select Power	A

J2 Cont'd

PIN	DESCRIPTION	KEY
b.	Readout Select-XPDR & Return	A
c.	Readout Minus	A
d.	" Blank	A
e.	" Dashes	A
f.	Ident. Code	A
g.	Ident. Tone	A
h.	All Remote Control	A
i.	Equalization Pulse	A
j.	DME P2 Deviation	B
k.	DME P2 OFF	A
m.	DME Mode	A
n.	X Mode	A
p.	Auto X-Y Mode	A
q.	1st MSD A Readout Control	A
r.	" " B " "	A
s.	2nd " A " "	A
t.	" " B " "	A
u.	" " C " "	A
v.	" " D " "	A
w.	3rd " A " "	A
x.	" " B " "	A
y.	" " C " "	A
z.	" " D " "	A
AA	4th " A " "	A
BB	" " B " "	A
CC	" " C " "	A

J2 Cont'd

PIN	DESCRIPTION	KEY
DD	4th MSD D Readout Control	A
EE	5th MSD A " "	A
FF	" " B " "	A
GG	" " C " "	A
HH	" " D " "	A

KEY

A = TTL Level

B = 0-10 V Analog

C = ARINC Level

T = Used with TACAN Adaptor

REMOTE CONTROL JACK J3 PIN ASSIGNMENT

TYPE BTO2A-22-55SX MATING CONNECTOR TYPE BTO6AC-22-55PX

PIN	DESCRIPTION	KEY
A.	Air to Air Mode	A T
B.		
C.		
D.		
E.		
F.	Modulator 50% Level Pulse	A T
G.		
H.		
J.		
K.		
L.	TACAN Modulation	B T
M.		
N.		
P.		
R.	Internal TACAN Modulation	A
S.		
T.		
U.		
V.	DME U.T. Suppressor Input	C
W.	Suppressor Output	C
X.	DME Pulse Pair Trig	A
Y.	DME Reply Level	B
Z.		

J3 Cont'd

PIN	DESCRIPTION	KEY
a.	XPDR P1 Level	B
b.	XPDR P2 OFF	A
c.	XPDR Mode	A
d.	XPDR Pulse Width	B
e.	XPDR Double Interrogation Delay	B
f.	XPDR Double Interrogation	A
g.	XPDR P2 Deviation	B
h.	XPDR P3 Deviation	B
i.	XPDR P2 Level	B
j.	XPDR P3 Level	B
k.	XPDR Mode A	A
m.	" " B	A
n.		
p.	" " D	A
q.	" " A-C	A
r.	XPDR Remote Trig Mode	A
s.	XPDR Trig.	A
t.	External 2 MHz VFO	A
u.	" " " ON	A
v.	Squitter Rate Control	B
w.	Squitter Rate Hi Range	A
x.	" " Inhibit	A
y.	DME ECHO Level	B
z.	DME ECHO	A
AA	115 VAC 400 Hz	C

J3 Cont'd

PIN	DESCRIPTION	KEY
BB	AC Common	C
CC		
DD	Chassis Ground	
EE	Freq. Uncal	A
FF	Demodulator 50% Level Detector	A
GG	DME Inbox Signal Inhibit	A
HH	DME Single Pulse Trigger	A

KEY

A = TTL Level

B = 0-10 V Analog

C = ARINC Levels

T = Used with TACAN Adaptor

JACK OPERATION

REMOTE CONTROL JACK (J1)

A. Attenuator Load

Application of a "0" causes the data present on Pins U thru B of J1 to be transferred to the Attenuator control.

B. P1-P2 Spacing Over-ride

Application of a "0" causes the Test Set P1-P2 spacing window to be eliminated thus allowing the test set to reply when interrogated by a pulse pair of improper spacing.

C. Remote Frequency Control

Application of a "0" causes the Test Set frequency to be controlled remotely by pins j thru x of Jack (J1).

D.E.F.G. DME % Reply A, B, C, D

Application of a "0" controls the DME Reply Efficiency. Code is Inverse BCD (GND, OPEN, OPEN, GND = 90%)

H. thru b. Register Load Value

Application of a "0" determines the value to be loaded into the Acc, Vel, or Distance Register when the respective Register Load Control Pins c,d or e, Jack (J1), is activated. Code is Inverse BCD.

Distance, 0-399.99 NMi, used A1 thru B10000

Velocity, 0-3999, Kts., uses A1 thru B1000

Acceleration, 0-399 FPS, uses A1 thru B100

c., d., e. Distance, Velocity, Acceleration Register Load

Application of a "0" causes information on Register Load Value pins H thru b of Jack (J1) to be transferred to the appropriate Distance, Velocity, or Acc. Register.

J1 Cont'd

f.,g.,h. Distance, Velocity, Acceleration Register Clear

Application of a "0" causes the appropriate Distance, Velocity, or Acceleration Register to be cleared to zero.

i. Freq. Select Common

External Frequency selector common ground.

j. thru x Freq. Selector

Remote Frequency Selector Control input. Code is 2 out of 5 per ARINC Characteristic 410.

y. DME U.T. Flag Alarm

Warning Flag output from DME Under Test. Per ARINC Characteristic 568.

z,AA. Serial BCD Distance Data Hi, Lo

Serial BCD Distance Data Hi, Lo output from DME Under Test. Per ARINC Characteristic 568.

BB,CC Serial BCD Clock Hi, Lo

Serial BCD Clock Hi, Lo output from DME Under Test. Per ARINC Characteristic 568.

DD,EE Serial BCD Word Sync Hi, Lo

Serial BCD Word Sync. Hi, Lo output from DME Under Test. Per ARINC Characteristic 568.

J1 Cont'd

HH -1 Nautical Mile

Application of a "0" causes 1NMI to be subtracted
from Distance.

REMOTE CONTROL (J2) OPERATION

A. This Pin provides the 100's BCD Data that is loaded into the Programmable Attenuator.

B. Data Strobe

A negative going pulse indicates the information on the Readout wires q thru HH of Jack (J2) has just been updated.

C. Readout Select-Interro. Rate

Application of a "0" causes the DME Interro. Rate to appear on the Readout and on the Readout pins q thru HH of Jack (J2).

D. Readout Overrange

When in the ΔF Mode should the MHz VFO deviation be large enough to cause a ΔF reading of more than 9.99MHz. a "one" will appear on this pin to indicate Overrange.

E. Analog Distance Pulse Trig.

When in the Analog P.P. Mode, as selected by front panel switch, application of trigger will cause the Test Set to reply as if it had been properly interrogated. The Analog Distance Pulses are also generated as a result.

F. Direction Control Inbound

Application of a "0" causes the Distance Register to be incremented to a lesser value. Rate of change of Distance is controlled by the Velocity Register.

J2 Cont'd.

G. Direction Control Outbound

Application of a "0" causes the Distance Register to be incremented to a greater value.

H. Velocity Control Increase

Application of a "0" allows the Velocity Register to be incremented to a greater value. Rate of change of Velocity is controlled by the Acceleration Register.

J. Velocity Control Decrease

Application of a "0" allows the Velocity Register to be incremented to a smaller value.

K thru T Attenuator Readout

These Pins provide the 1's and 10's BCD data that is loaded into the Programmable Attenuator.

U thru b Readout Select

Application of a "0" causes the appropriate information to appear on the Readout and on the Readout pins q thru HH of Jack (J2).

c. Readout Minus

When in the Δ F Mode should the 2 MHz VFO deviation be such as to cause Test Set freq. to be less than the digitally programmed center frequency a "one" will appear on this pin providing the Freq. Uncal Mode is also selected.

J2 Cont'd

A "one" will appear when in the Acc. or Vel. Mode and the respective function is causing the Velocity to decrease or the Distance to decrease.

d. Readout Blank

A "one" will appear on this pin when the inputs from the DME Under Test are such as to cause an indicator to blank.

e. Readout Dashes

A "one" will appear on this pin when the Serial BCD Distance Data input from the DME U.T. is such as to cause the Readout to display Dashes provided the Measured Distance Readout Mode is selected.

f. Ident. Code

Application of a "0" causes the Test Set to generate the Ident Code.

g. Ident Tone

Application of a "0" causes the Test Set to generate the Ident Tone.

h. All Remote Control

Application of a "0" causes all DME and XPDR test controls to be remotely controllable by the Remote Control Jacks (J1,J2,J3), but does not cause the Test Set frequency to be controlled remotely.

J2 Cont'd

i. Equalization Pulse

Application of a "0" causes the Equalization Pulse to be generated when in the Ident. Code/Tone Mode.

j. DME P2 Deviation

Application of a 0-10V voltage to this pin causes the DME P1-P2 spacing to vary.

k. DME P2 OFF

Application of a "0" causes the removal of the DME P2 pulse.

m. DME Mode

Application of a "0" causes the Test Set to function in the DME Mode.

n. X Mode

Application of a "0" causes the DME P1-P2 Pulse Coding to conform to X Mode requirements.

p. Auto X-Y Mode

Application of a "0" causes the DME P1-P2 Pulse Coding to be automatically that which is required by the channel pairing scheme.

q. thru HH Readout Control

The information present on these wires in BCD code is the same as that which is fed to the Readout Driver Logic.

REMOTE CONTROL JACK (J3) OPERATION

A. Air to Air MODE

Application of a "0" causes the Test Set frequency to correspond to Y-Mode.

F. Modulator 50% Level Pulse

Information on this pin intended for use in Air to Air Mode.

L. TACAN Modulation

Application of modulation signal causes the RF pulse amplitude to be AM modulated.

R. Internal TACAN Modulation

Application of a "0" causes TACAN Modulation to appear on the Test Set RF output. This is 15/135Hz amplitude modulation only and does not include reference bursts. Generated internally in the Test Set.

V. DME U.T. Suppressor Input

Application of the DME U.T. Suppression Pulse causes the Test Set Scope Sync Output to be triggered by the Suppression Pulse when Sync Output Control is in the TO position.

W. Suppressor Output

This pin carries the Suppression Pulse generated by the Test Set. This pulse is synchronous with the DME Reply or the XPDR Interrogation.

J3 Cont'd

X. DME Pulse Pair Trig.

Application of a trigger pulse causes the Test Set to generate a DME P1 and P2 Pulse. The P1-P2 spacing will correspond to that generated in the Test Set.

Y. DME Reply Level

Application of a voltage causes the amplitude of the DME RF Pulse to vary.

a. XPDR P1 Level

Application of a voltage causes the amplitude of the XPDR P1 RF Pulse to vary.

b. XPDR P2 OFF

Application of a "0" removes the XPDR P2 Pulse

c. XPDR Mode

Application of a "0" causes the Test Set to function in the XPDR Mode.

d. XPDR Pulse Width

Application of a voltage causes the XPDR Pulse Width to vary.

e. XPDR Double Interrogation Delay

Application of a voltage causes the Double Interrogation Delay to vary.

J3 Cont'd

f. XPDR Double Interrogation

Application of a "0" causes the Test Set to Double Interrogate the XPDR U.T.

g. XPDR P2 Deviation

Application of a voltage causes the XPDR P1-P2 Pulse Spacing to vary.

h. XPDR P3 Deviation

Application of a voltage causes the XPDR P1-P3 Pulse Spacing to vary.

i. XPDR P2 Level

Application of a voltage causes the amplitude of the XPDR P2 RF Pulse to vary.

j. XPDR P3 Level

Application of a voltage causes the amplitude of the XPDR P3 RF Pulse to vary.

k. thru q. XPDR MODE Select

Application of a "0" to one of these pins causes the XPDR P1-P3 Pulse Spacing to correspond to the requirements of Mode A,B,C,D, or A-C.

r. XPDR Remote Trig Mode

Application of a "0" enables the S/N to generate XPDR pulses upon external trigger only.

J3 Cont'd

s. XPDR Trig.

Application of a trigger pulse causes the Test Set to generate a XPDR pulse.

t. External 2 MHz VFO

This pin allows the application of an External 2MHz VFO input to cause the deviation of the Test Set frequency. This input must be used in conjunction with "0"s on Pins U and EE at Jack (J3).

u. External 2MHz VFO ON

Application of a "0" allows an External 2MHz VFO input, pin t, Jack (J3) to be substituted for the internal 2MHz VFO.

v. Squitter Rate Control

Application of a voltage varies the Test Set Squitter Rate.

w. Squitter Rate Hi Range

Application of a "0" causes the Squitter Rate Generator to operate in the High Range, approx. 1,000 to 10,000 pulses per second.

x. Squitter Rate Inhibit

Application of a "0" causes the Squitter to be Inhibited.

J3 Cont'd

y. DME ECHO Level

Application of a voltage causes the DME ECHO Level to vary.

z. DME ECHO

Application of a "0" causes the DME ECHO to appear.

AA. 115VAC 400Hz

Application of primary power to this pin allows the Indicator U.T. to be powered by 26VAC on pins of the Indicator U.T. Jack, J4.

BB. AC Common

Other side of 400Hz primary power. Also connects to AC Common pin of the Indicator U.T. Jack, J4.

DD. Chassis Ground

Connection to Test Set Chassis.

EE. Freq. Uncal

Application of a "0" causes the Test Set frequency to be controlled by 2MHz VFO.

FF. Demodulator 50% Level Detector

Information on this pin intended for future use with Remote IFF Adaptor.

J3 Cont'd

GG. DME Inbox Signal Inhibit

Application of a "0" prevents any DME Pulses from being initiated internally except for Echo Pulses. DME Pulses may be initiated by the DME Single Pulse input, pin HH of Jack (J3), the DME Pulse Pair Trig input, pin X of Jack (J3), or the internal Echo Trigger.

HH. DME Single Pulse Trigger

Application of a trigger pulse causes the Test Set to generate a single RF pulse.

WIRING CONNECTIONS

REMOTE CONTROL JACK (J1)

PIN	CONNECTION	PIN	CONNECTION
A	J 101-P6	<u>d</u>	S7-1 C2-A2
B	C6-A11	<u>e</u>	S8-1 C1-B33
C	S12-1 L2-30 L2-31 L3-50	<u>f</u>	S9-1 C3-B28 C9-B19
D	S23A-10 C7-B3	<u>g</u>	S10-1 C2-A3 C9-B20
E	S23B-11 C7-B6	<u>h</u>	S11-1 C1-B32 C9-B17
F	S23C-8 C7-B5	<u>i</u>	Gnd
G	S23C-11 C7-B4	<u>j</u>	L3-53
H	L2-115	<u>k</u>	L3-62
J	L2-106	<u>m</u>	L3-65
K	L2-91	<u>n</u>	L3-63
L	L2-82	<u>p</u>	L3-66
M	L2-86	<u>q</u>	L3-64
N	L2-89	<u>r</u>	L3-68
P	L2-67	<u>s</u>	L3-69
R	L2-58	<u>t</u>	L3-70
S	L2-62	<u>u</u>	L3-71
T	L2-65	<u>v</u>	L3-67
U	L2-79	<u>w</u>	L3-74
V	L2-70	<u>x</u>	L3-72
W	L2-74	<u>y</u>	C9-B31
X	L2-77	<u>z</u>	C9-A29
Y	L2-103	AA	Gnd
Z	L2-94	BB	C9-B22
<u>a</u>	L2-98	CC	Gnd
<u>b</u>	L2-101	DD	C9-B23
<u>c</u>	S6-1 C1-A4		

J1 Cont'd

PIN	CONNECTION
EE	Gnd
FF	NC
GG	NC
HH	S19-3 L2-121 C6-B9

REMOTE CONTROL JACK (J2) WIRING CONNECTIONS

PIN	CONNECTION	PIN	CONNECTION
A	J101-7	<u>b</u>	S5-1 L2-35 L2-36 C5-B10
B	C6-A2 C5-A19 C4-A31 C3-A9 C2-A22	<u>c</u>	L1-43 C3-A17
C	S5-4 C5-A24	<u>d</u>	L1-45 C4-B27
D	L1-39 C3-A19	<u>e</u>	L1-51 C4-B28
E	C6-B17 C9-B33	<u>f</u>	S2-1 C8-B14
F	S17-3 C5-B33	<u>g</u>	S2-3 C8-B13
G	S17-1 C5-B31	<u>h</u>	S12-4 L2-7
H	S18-3 C5-B26	<u>i</u>	S13-3 C8-B11
J	S18-1 C5-B28	<u>j</u>	C10-B29
K	J101-13	<u>k</u>	L2-19 L2-20 C10-B25
L	J101-16	<u>m</u>	S16A-9 G19-3 C7-B37 C8-A4 C9-B3
M	J101-14	<u>n</u>	S16B-7 L3-57
N	J101-15	<u>p</u>	S16B-9 L3-52
P	J101-9	<u>q</u>	L1-38 C6-A10
R	J101-11	<u>r</u>	L1-40 C6-A5
S	J101-10	<u>s</u>	L1-41 C2-A18
T	J101-12	<u>t</u>	L1-47 C2-A19
U	S5-3 L2-25 L2-26 C5-B11	<u>u</u>	L1-48 C2-A20
V	S5-5 L2-43	<u>v</u>	L1-42 C2-A21
W	S5-6 L2-47	<u>w</u>	L1-50 C4-A29
X	S5-8 L2-52 L2-53 C4-A15	<u>x</u>	L1-53 C4-A32
Y	S5-7 L2-50	<u>y</u>	L1-52 C4-A30
Z	S5-2 L2-40 L2-39 C5-B12	<u>z</u>	L1-49 C4-A33
<u>a</u>	S5-9 L2-32 L2-33 C11-B23 C1-B34 C4-B2 C5-B34 C6-B14 C9-B21	AA	L1-59 C5-A15
		BB	L1-56 C5-A16

J2 Cont'd

PIN	CONNECTION
CC	L1-57 C5-A17
DD	L1-58 C5-A18
EE	L1-60 C6-B36
FF	L1-63 C6-B37
GG	L1-62 C6-B38
HH	L1-61 C6-B39

REMOTE CONTROL JACK (J3) WIRING CONNECTIONS

PIN	CONNECTION	PIN	CONNECTION
A	L3-2	<u>d</u>	C10-A9
B	NC	<u>e</u>	C11-B11
C	NC	<u>f</u>	S4-7 C8-A2
D	NC	<u>g</u>	C11-B20
E	NC	<u>h</u>	C11-B3
F	G18-34 C7-B32	<u>i</u>	G18-5
G	NC	<u>j</u>	G18-6
H	NC	<u>k</u>	S16B-6 C8-B34
J	NC	<u>m</u>	S16B-5 C8-B35
K	NC	<u>n</u>	NC
L	G18-28 C9-A18	<u>p</u>	S16B-3 C8-B36
M	NC	<u>q</u>	S16B-2 C8-B33
N	NC	<u>r</u>	S16B-1 C8-B39
P	NC	<u>s</u>	C10-B23
R	S1-3 C9-A24	<u>t</u>	G24-2
S	NC	<u>u</u>	G24-3
T	NC	<u>v</u>	C9-B2
U	NC	<u>w</u>	S20-3 C7-B28
V	C7-B17	<u>x</u>	S20-1 C7-B25 C9-A6
W	J12-1 C9-B30	<u>y</u>	G18-26
X	C8-B10	<u>z</u>	S21-7 C6-B16
Y	G18-25	AA	T2-1
Z	NC	BB	T2-2 T2-3 J4-X
<u>a</u>	G18-4	CC	NC
<u>b</u>	C8-A30	DD	Gnd
<u>c</u>	S16A-1 G19-2 C8-B38	EE	S24-5 L2-113

J3 Cont'd

PIN	CONNECTION
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FF	G23-3
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GG	C6-B20 C8-B17
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HH	C7-B26
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SECTION VII
MISCELLANEOUS INDEX

MINIMUM PERFORMANCE SPECIFICATIONS

CHECK LIST

COMPONENT CROSS REFERENCE

MINIMUM PERFORMANCE SPECIFICATIONS

KUSTOM INSTRUMENTS

SQUAWK/NAUT I

1. Readout Units and Decimal Points

The following units and decimals points shall appear as the Readout Selector switch is placed in all positions.

Position	Units	D.P.
XPDR % RETURN	%	-
ΔF	MHz	X.XX
Squitter Rate	PPS	-
Interro. Rate	PPS	-
Acc.	FPS	-
Vel.	KTS	-
Test Dist.	NMi	XXX.XX
Meas. Dist.	NMi	XXX.XX
Power	WTS	-

2. Acc. Reg. Loading and Clearing and Readout

The Acc. Reg. shall load upon command of the F.P. Acc. Load Switch to the value determined by the F.P. Distance - Velocity - Acceleration Switch and display this value on the Readout.

The Acc. Reg. shall clear to zero upon command of F.P. Acc. Clear Switch.

The contents of the Acc. Reg. shall always be zero upon power turn on.

3. Vel. Reg. Loading and Clearing and Readout

The Vel. Reg. shall load upon command of the F.P. Vel. Load Switch to the value determined by the F.P. Distance - Velocity - Acceleration Switch and display this value on the Readout.

The Vel. Reg. shall clear to zero upon command of F.P. Vel. Clear Switch.

The contents of the Vel. Reg. shall always be zero upon power turn on.

4. Dist. Reg. Loading and Clearing and Readout

The Dist. Reg. shall load upon command of the F.P. Dist. Load Switch to the value determined by the F.P. Distance - Velocity - Acceleration Switch and display this value on the Readout.

The Dist. Reg. shall clear to zero upon command of F.P. Dist. Clear Switch.

The contents of the Dist. Reg. shall always be zero upon power turn on.

5. Acc. Rate Gen.

The Acc. Rate shall change as the contents of the Acc. Reg. change. With 200 FPS loaded into the Acc. Reg. the output of the Acc. Rate Gen. shall be 118 pps.

6. Vel. Rate Gen.

The Vel. Rate shall change as the contents of the Vel. Reg. change. With 2000 Kts. loaded into the Vel. Reg. the output of the Vel. Rate Gen. shall be 55 pps.

7. Vel. Increase Control

The Vel. shall increase to 4000 Kts. and Halt.

8. Vel. Decrease Control

The Vel. shall decrease to 0 Kts. and Halt.

9. Vel. ARINC P.O. Control

The Vel. shall increment to 0 Kts. and then increment to larger values.

The contents of the Acc. Reg. shall be cleared to zero when the Vel. reaches 200 Kts.

10. Negative Acc. Indicator

A Minus sign shall appear to indicate negative Acc. when the Vel. Control is placed in Decrease position.

11. Distance Inbound Control

The Distance shall decrease to 0 NMi and Halt.

12. Distance Outbound Control

The Distance shall Increase to 399.99 NMi and Halt.

13. Distance Auto Control

The direction of Distance incrementation shall reverse at:

0 NMi					
99.99 NMi	and return to 0 NMi				
199.99 NMi	"	"	"	"	"
299.99 NMi	"	"	"	"	"
399.99 NMi	"	"	"	"	"

14. Measured Dist. Readout

When the Readout selector is placed in the Measured Dist. position there shall appear on the Readout the data transmitted from the DME U.T.

The Serial Data Receivers shall accept as a high level a voltage that is 10V or more and as a low level a voltage that is 1 volt or less.

The Measured Dist. Readout shall blank when the Alarm Flag voltage is 1.0 Volt or less.

15. Negative Velocity Indication

A Minus sign shall appear to indicate a Negative Vel. when the Distance Control is in the Inbound position.

16. Indicator U.T. Serial Data Clock Freq.

The Clock Freq. shall be 11 ± 0.5 KHz when the control is placed in the 11 KHz position, 7 ± 1 KHz when placed in the 7 KHz position, 15 ± 1 KHz when placed in the 15 KHz position.

17. Indicator U.T. Serial Data Clock Driver Output

The Driver Level shall be 3 ± 0.2 volts at the Low level and 7 ± 0.2 volts at the High Level.

The Rise and Fall Time shall be in the range of 1 to 10 usec.

18. Indicator U.T. Serial Data Sync. Driver Output

The Driver Level shall be 3 ± 0.2 Volts at the Low level and 7 ± 0.2 Volts at the High Level.

The Rise and Fall times shall be in the range of 1 to 10 usec.

19. Indicator U.T. Serial Data Data Driver Output

The Driver Level shall be 3 ± 0.2 volts at the Low Level and 7 ± 0.2 volts at the High Level.

The Rise and Fall times shall be in the range of 1 to 10 usec.

20. Indicator U.T. Flag Alarm Driver Output

The Flag Alarm voltage shall be 1 ± 0.2 volts when the Control is placed in the Flag position and 18.5 ± 0.2 volts when returned to Normal position.

21. Indicator U.T. Distance, Flag and Dash Indications

The Indicator U.T. shall display exactly the same Distance as that displayed by the Readout when in the Test Dist. position.

The Indicator U.T. shall blank when the Flag control is placed in the Flag position and the Readout selector is in the Test Dist. position.

The Indicator U.T. shall display Dashes when the Dash control is placed in the Dash position and the Readout selector is in the Test Dist. position.

22. Analog P.P. Control

When the Analog P.P. Control is operated a R.F. Pulse Pair shall be originated by the Initial Delay Logic.

Also there shall appear on the output of the Analog Pulse Pair Driver a pair of Pulses. The spacing between the pulses shall be 50 usec. plus the Distance Delay in X-Mode.

The repetition rate shall be in the range of 10 to 15 per sec.

23. Analog Pulse Pair Driver Output

The Driver Levels shall be 3 ± 0.2 volts at the Low level and 7 ± 0.2 volts at the High Level.

The Rise time shall be 3 usec. max. and the Fall time shall be 7 usec max.

The pulse duration shall be in the range of 4 to 10 usec.

A pair of pulses shall appear each time a RF Reply Pulse Pair is originated.

The spacing between the pulses shall be 50 usec. plus the Distance Delay in X-Mode.

24. Range Rate Driver Output

The Driver Levels shall be 3 ± 0.2 volts at the Low Level and 7 ± 0.2 volts at the High Level.

The Rise time shall be 3 usec max. and the Fall time shall be 7 usec. max.

The pulse duration shall be in the range of 4 to 10 usec.

A pulse shall appear each time the Distance Delay is changed 0.01 NMi.

25. Interrogation P1 - P2 Spacing

No Reply Pulses shall be present unless the Interrogation Pulse Pair spacing is in the range 12 ± 0.5 usec. in X Mode and 36 ± 0.5 usec., in Y Mode. Provided the P1-P2 Spacing Over-ride is not present.

26. DME % REPLY

The ratio of Replies to Interrogations shall vary in accordance with the setting of the DME % REPLY control.

27. Suppression Pulse Driver Output

The Driver output shall be 0 volts at the Low Level and 18 ± 0.2 volts at the High Level.

The synchronization shall be such that the Drive output goes to the High Level 1 to 5 usec. prior to the 10% level of the

27. Suppression Pulse Driver Output (Cont'd)

first pulse of Reply Pulse Pair or the P1 pulse of the XPDR Interro. The Driver output shall return to 0 volts approximately 8 usec. after the 50% point of P2 pulse of the Reply or approximately 2 usec after the 50% point of the P3 pulse of the XPDR Interrogation.

28. Squitter Rate

The Squitter shall vary in accordance with the Operation of the Squitter Rate Hi-Lo-Off Control.

The Squitter Rate shall vary over the range 9500 ± 250 PPS to less than 800 PPS when in the Hi Range and over the range of 800 PPS to 100 PPS when in the Lo range in both the DME Mode and XPDR Mode.

The Squitter Rate as indicated on the Readout shall be accurate to ± 1 count $\pm 0.5\%$.

The pulse spacings shall be random in the DME Mode and regular in the XPDR Mode.

29. Generator Frequency Accuracy

The Generator Frequency shall be within 0.001% of the assigned frequency called for by the MHz Frequency Select, Channel Frequency Select or the Remote Frequency Select at 25°C .

The Generator Frequency shall not vary more than $\pm 0.003\%$ from the assigned frequency over the temperature range of -15°C to $+55^{\circ}\text{C}$ after a 30 minute warm-up period.

30. UNCAL Control ΔF Control and ΔF Readout Accuracy

When the UNCAL Control is operated so as to light the Control the Generator Frequency shall be variable by means of the ΔF Control.

The ΔF Control shall be capable of causing the Generator Frequency to vary by at least ± 2 MHz from the assigned frequency.

The ΔF Readout shall indicate to within ± 0.01 MHz the deviation of the Generator Frequency from the CAL Frequency.

31. Generator Frequency Spectrum

The Generator Frequency spectrum shall have no discrete spurious outputs at any level greater than 60db below the desired output level at any frequency between 900 and 1300 MHz.

The Generator Frequency spectrum shall display not more than 30 KHz P-P Residual FM measured with a 1 KHz bandwidth.

The Generator Frequency spectrum at the -60 db level shall not be broader than 300 KHz measured with a 1 KHz bandwidth.

The Generator Frequency spectrum shall not display more than 50 KHz pulling due to modulation effects.

32. RF CW Output Level Accuracy

The RF Level shall vary not more than 1 db over the frequency range of 962 MHz to 1213 MHz.

The RF Level at the -10 dbm attenuator setting shall be in the range of -10 \pm 0.5 dbm. The Level variation shall be centered about -10 dbm.

The Rf Level attenuation below the -10 dbm Level shall agree with the Attenuator Dial setting to within \pm 0.25 db or \pm 0.004 (Dial Setting -10) db, which ever is greater.

The CW Level shall be available when the CW Output Control is placed in the ON position and the Mode Select Control is placed in the DME Mode.

33. Main Reply Pulse Level Accuracy

The peak amplitude of the Main Reply Pulses shall be within \pm 0.1 db of the CW Output Level.

34. Tacan Mod. Control

When the Tacan Mod. Control is placed in the ON position the RF Pulse amplitude shall be modulated by a composite 15 Hz and 135 Hz signal. Each component shall have a modulation factor in the range of 15% to 25%.

35. Video Output Monitor

The Video Output Monitor shall display either the demodulated CW Level or RF Pulses originating internally in either the DME Mode or the XPDR Mode.

36. Echo Injection

The Echo Pulses shall appear when the Echo Injection ON-OFF Control is in the ON Position.

The Echo Pulse Pair level shall vary in accordance with the position of the Echo Suppression Control. At the 0 db setting the Echo Pulse Pair amplitude shall be within 0.1db of the Main Reply amplitude. At the -6db setting the Echo Pulse Pair amplitude shall be -6 ± 0.5 db below the Main Reply amplitude.

The Echo Pulse Pair shall occur at a Range of 30 ± 1 Nmi.

The Echo Pulse Pair spacing shall be 12 ± 1 usec. in X Mode and 30 ± 1 usec. in Y-Mode.

37. RF ON-OFF Ratio

During the interval between pulses the RF CW Level shall be at least 80 db below the RF Pulse peak amplitude.

38. Mode Select Control

When the Mode Select Control is in the X position the P1-P2 spacing shall correspond to X Mode, in the Y position to Y Mode, and in the Auto X-Y position to either X or Y Mode as determined by the requirements of the channel pairing scheme. The Interro. P1-P2 Spacing window shall also vary accordingly.

When the Mode Select control is placed in the A,B,C,D or A-C positions the XPDR Interro. P1-P3 pulse spacing shall correspond to that mode. When placed in the EXT. position no pulses shall be originated internally.

39. P2 Deviation Control

The P1-P2 Pulse spacing shall vary in accordance with the P2 Deviation Control. With the control set at the 0 position the P1-P2 Pulse spacing shall be 12 ± 0.1 sec. in X Mode and 30 ± 0.1 usec. in Y Mode. With the control set at ± 4 usec the deviation shall be ± 0.3 usec.

The P2 Pulse shall not be present when the P2 ON-OFF Control is in the OFF position.

40. Power Readout Accuracy

The Power Readout shall be accurate to within $\pm 0.5\text{db}$ when a 1 KW pulse is applied over the frequency range of 1025 MHz to 1150 MHz. When the RF input is decreased by a factor of 10 the Power Readout shall indicate a value in the range of $10 \pm 0.5\%$ of the previous reading.

The Power Readout shall indicate zero power within 0.4 sec after the removal of the RF Pulses.

41. Detected Pulse Monitor Output

The Detected Pulse Monitor shall display the demodulated envelope of either the DME Interrogation Pulses or the XPDR Reply Pulses.

42. Scope Sync. Control

When the Scope Sync. Control is in the TO position there shall be present on the Scope Sync Output a pulse which is synchronous with the DME Interrogation P1 pulse or the XPDR Interrogation P1 pulse. When in the Squitter Pulse, Reply Pulse or Ident Pulse or the XPDR Interrogation P1 Pulse. When in the TD position the sync pulse shall be synchronous with the DME Reply pulse or the XPDR Interrogation P3 pulse.

43. Interrogation Rate Readout Accuracy

The Interro. Rate Readout shall indicate to within ± 1 count the true DME Interro Rate.

44. Range Delay Accuracy

The zero NMi delay shall be accurate to within ± 0.04 NMi.

The Range Delay shall be accurate to within ± 0.005 NMi per 100 NMi plus the Zero NMi Delay.

45. -1 NMi Control

When the -1 NMi control is activated the Range Delay shall decrease by 1 NMi. A "-1 NMi" shall appear in the Readout.

46. Pulse Priority

The pulses shall have the following order of priority. Ident pulses, Reply pulses and Squitter pulses.

The squitter pulses shall be inhibited so that they will not occur closer than 50 usec to the Reply pulses.

47. Ident Control and Equalizing Pulse Control

When the Ident. Control is placed in the Ident. position the code KID shall be generated. When placed in the Tone position a continuous string of pulses shall appear.

The repetition rate of the pulse pairs shall be 1350 pulses per second.

When the Equalization Pulse control is placed in the ON position a pulse pair shall appear 100 ± 10 usec after each Ident. pulse pair.

There shall be a interval of at least 5 sec between Ident. Code cycles.

48. Flag Alarm Level

When the voltage on the input to the Flag Alarm receiver becomes less than 1.0 volt the readout shall Blank provided the selector is in the Meas. Dist. Mode.

49. Frequency Monitor Output

There shall appear at the Freq. Monitor output a beat frequency which is the difference between the Generator Frequency +63 MHz and the DME transmitter frequency. In the XPDR mode the beat frequency is the difference between the Generator Frequency +60 MHz and the XPDR transmitter frequency.

50. Calibrate Phase Control and Cal. Output

When the Calibrate Phase 1.0 usec - 1.45 usec Control is in the 1.45 usec. position there shall appear at the Cal output a 1.45 usec. spacing pulse train which is variable in phase, as referenced to the XPDR Interrogation pulses, by means of the Calibrate Phase Control. The Phase variation shall be such that any delay may be overlaid by means of either a rising or falling edge of the pulse.

When the Calibrate Phase 1.0 usec - 1.45 usec Control is in the 1.0 usec. position a 1.0 usec. spacing pulse train appear at the Cal. Output that is also phase variable.

51. XPDR P1 Pulse Level

The peak amplitude of the P1 pulse of the XPDR Interrogation shall be within ± 0.1 db of the CW Output Level.

52. XPDR P2, P3 Suppression Control

The XPDR P2, P3 Pulse Level shall vary in accordance with the position of the XPDR P2, P3 Suppression control. At the 0 db setting the peak amplitude shall be within ± 0.1 db of the CW output Level. At the -6db setting the amplitude shall be -6 ± 0.3 db below the CW Output Level.

53. XPDR Pulse Width Control

The XPDR RF Pulse Width shall vary in accordance with the setting of the XPDR Pulse Width Control and shall be within ± 0.025 usec. of the setting of the control.

54. XPDR P2 Deviation Controls

The P1 - P2 spacing shall vary from the assigned pulse spacing of 2 usec. with the XPDR P2 Deviation Control setting and shall be within ± 0.025 usec of setting of the control.

55. XPDR P3 Deviation Control and Interrogation Modes

The P1 - P3 pulse spacing shall vary from the assigned pulse spacing with the setting of the XPDR P3 Deviation control and shall be within ± 0.025 usec. of the setting of the control.

The assigned P1 - P3 Pulse spacing shall be 8 usec. in A Mode, 17 usec. in B Mode, 21 usec. in C Mode, and 25 usec in D Mode.

In the A-C Mode there shall be three A Mode interrogations to one C Mode interrogation.

In the Ext Mode there shall be no XPDR Interrogations initiated internally.

56. XPDR Double Interrogation Control

When the Double Interrogation ON-OFF Control is placed in the On position there shall appear following each XPDR Interrogation a second Interrogation.

The delay of these pulses shall be controlled by the setting of the Double Interrogation Control and shall be variable over the range from 30 to 40 usec. to 250 to 270 usec. after P3.

57. XPDR % Return Readout

The XPDR % Return Readout shall display the ratio of XPDR Returns to Interrogations in percent and be accurate to within ± 1 count.

58. Remote Operation

When the Frequency Sel. Control is placed in the Remote position the Generator Freq. shall be determined by the inputs to the rear connector only.

When the Remote Control is placed in the All Remote position all functions listed shall be controllable from the rear connectors.

59. Regulator Voltage Accuracy

The output voltages of the power supplies shall be set within the following ranges:

+28V	+28 $\pm 0.05V$
+16V	+16 $\pm 0.20V$
+10V	+10 $\pm 0.05V$
+ 5V	+ 5 $\pm 0.05V$
- 5V	- 5 $\pm 0.20V$
-10V	-10 $\pm 0.20V$
-28V	-28 $\pm 0.30V$
+16 $\pm 2V$	+16 $\pm 2V$

The Regulator output voltages shall display no indication of degradation as the Line Voltage is dropped from 120V to 100V.

CHECK LIST

S/N _____

DATE _____

0. _____ A. Check Regulator Voltages
 _____ B. Check Card Rack Ground Voltage
 80 mv max.

1. Readout Units and Decimal Points

	<u>POSITION</u>	<u>UNITS</u>	<u>D.P.</u>
_____ A.	XPDR % Return	%	---
_____ B.	Δf	MHz	X.XX
_____ C.	Squitter Rate	PPS	--
_____ D.	Interro. Rate	PPS	--
_____ E.	Acc.	FPS	--
_____ F.	Vel.	KTS	--
_____ G.	Test Dist.	NMi	XXX.XX
_____ H.	Meas. Dist.	NMi	XXX.XX
_____ I.	Power	WTS	--

2. Acc. Reg. Loading, Clearing and Readout

- _____ A. Acc. Reg. Loads and displays the value determined by the F.P. Distance - Velocity - Acceleration Switch upon command of the F.P. Acc Load Switch
- _____ B. Acc Reg clears to zero upon command of F.P. Acc. Clear switch
- _____ C. Contents of the Acc. Reg. are zero upon Power Turn On

3. Vel. Reg. Loading, Clearing and Readout.

- _____ A. Vel. Reg. Loads and displays the value determined by the F.P. Distance - Velocity - Acceleration switch upon command of the F.P. Vel. Load Switch
- _____ B. Vel. Reg. Clears to zero upon command of F.P. Vel. Clear Switch
- _____ C. Contents of the Vel. Reg. are zero upon Power Turn On

4. Dist. Reg. Loading, Clearing and Readout

- _____ A. Dist. Reg. Loads and displays the value determined by the F.P. Distance - Velocity - Acceleration

ation switch upon command of the F.P. Dist. Load Switch.

_____ B. Dist. Reg. Clears to zero upon command of F.P. Vel. Clear switch.

_____ C. Contents of the Dist. Reg. are zero upon Power turn on.

5. Acc. Rate Gen.

_____ A. Acc. Rate changes as the contents of the Acc. Reg. changes.

_____ B. With 200 FPS loaded, read 118 PPS.

6. Vel. Rate Gen.

_____ A. Vel Rate changes as the contents of the Vel. Reg. change

_____ B. With 2000 kts. loaded, read 55 PPS.

7. Vel. Increase Control

_____ A. Vel. increases to 4000 KTS and halts

8. Vel. Decrease Control

_____ A. Vel decreases to 0 KTS and halts

9. Vel ARINC P.O. Control

_____ A. Vel increments to 0 KTS, then to larger values

_____ B. Contents of the Acc. Reg. clears to zero when Vel reaches 200 KTS

10. Negative Acc. Indicator

_____ A. Minus sign appears - to indicate negative Acc. when Vel control is placed in decrease position

11. Distance Inbound Control

_____ A. Distance decreases to 0 NMi and halts

12. Distance Outbound Control

_____ A. Distance increases to 399.99 NMi and halts

13. Distance Auto Control

Direction of distance incrementation reverses at

_____ A. 0 NMi	_____ C. 199.99 NMi	_____ E. 399.99 NMi
_____ B. 99.99 NMi	_____ D. 299.99 NMi	

14. Measured Dist. Readout

- ☐ A. Data from DME UT displayed on readout when read-out selector is placed in Meas. Dist. position.
- ☐ B. Serial Data Receivers accept as a High Level Voltage a voltage greater than 10V
- ☐ C. Serial Data Receivers accept as a Low Level Voltage a voltage less than 1V

15. Negative Velocity Indication

- ☐ A. Minus sign appears when the Direction control is in the Inbound position

16. Indicator U.T. Serial Data Clock Freq.

- ☐ A. Clock Freq. is 11 ± 0.5 Khz in 11 Khz position
- ☐ B. Clock Freq. is 7 ± 1 Khz in 7 Khz position
- ☐ C. Clock Freq. is 15 ± 1 Khz in 15 Khz position

17. Indicator U.T. Serial Data Clock Driver Output

- ☐ A. Low Driver Level is 3 ± 0.2 Volts
- ☐ B. High Driver Level is 7 ± 0.2 Volts
- ☐ C. Rise time is 1-10 usec
- ☐ D. Fall time is 1-10 usec

18. Indicator U.T. Serial Date Sync. Driver Output

- ☐ A. Low Driver Level is 3 ± 0.2 Volts
- ☐ B. High Driver Level is 7 ± 0.2 Volts
- ☐ C. Rise time is 1-10 usec
- ☐ D. Fall time is 1-10 usec

19. Indicator U.T. Serial Data Driver Output

- ☐ A. Low Driver Level is 3 ± 0.2 Volts
- ☐ B. High Driver Level is 7 ± 0.2 Volts
- ☐ C. Rise time is 1-10 usec
- ☐ D. Fall time is 1-10 usec

20. Indicator U.T. Flag Alarm Driver Output

- ☐ A. Flag alarm voltage is 1 ± 0.2 volts when control is placed in the Flag position and 18.5 ± 0.2

volts when returned to normal position

21. Indicator U.T., Distance, Flag and Dash Indications

- ☐ A. Indicator U.T. displays same distance as displayed by S/N Readout when in Test Distance position
- ☐ B. Indicator U.T. Blanks or displays a Flag when the Flag control is placed in the Flag position and the S/N readout selector is in the Test Dist. position
- ☐ C. Indicator U.T. displays Dashes when the Dash control is placed in the Dash position and the S/N readout selector is in the Test Dist. position.

22. Analog P.P. Control

- ☐ A. In Analog P.P. position on R. F. pulse pair is originated by the Initial Delay Logic
- ☐ B. Repetition rate is 10-15 per sec.

23. Analog Pulse Pair Driver Output

- ☐ A. Low Driver level 3 ± 0.2 Volts
- ☐ B. High Driver level 7 ± 0.2 Volts
- ☐ C. Rise Time 3 usec max.
- ☐ D. Fall Time 7 usec max.
- ☐ E. Pulse duration 4-10 usec
- ☐ F. A pair of pulses appear each time an R.F. reply pulse pair is originated.
- ☐ G. Spacing between pulses is 50 usec plus the Distance Delay in X-Mode

24. Range Rate Driver Output

- ☐ A. Low Driver level 3 ± 0.2 Volts
- ☐ B. High Driver level 7 ± 0.2 Volts
- ☐ C. Rise Time 3 usec max.
- ☐ D. Fall Time 7 usec max.
- ☐ E. Pulse duration 4-10 usec
- ☐ F. A pulse appears each time distance delay is changed 0.01 Nmi

25. Interrogation P1-P2 Spacing

- _____ A. P1-P2 Spacing over-ride is not present
- _____ B. No reply pulses are present unless Interrogation pulse pair spacing is 12 ± 0.5 usec in X mode and 36 ± 0.5 usec in Y mode
- _____ C. Acc. Clear Causes P1-P2 Spacing Override

26. DME % Reply

- _____ A. Ratio of replies to interrogations vary in accordance with the setting of the DME % Reply control.

27. Suppression Pulse Driver Output

- _____ A. Low level driver output 0 volts
- _____ B. High level driver output 18 ± 0.2 volts
- _____ C. Driver output goes to the high level 1-5 usec prior to the 10% level of the first pulse of Reply pulse pair or the P1 pulse of the XPDR Interrogation
- _____ D. Driver output returns to 0 volts 8 usec after the 50% point of P2 pulse of the reply or 2 usec after the 50% point of the P3 pulse of the XPDR Interrogation.

28. Squitter Rate

- _____ A. Squitter Rate varies from 9500 ± 250 PPS to less than 800 PPS in Hi range in both the DME and XPDR Modes.
- _____ B. Squitter Rate varies from greater than 800 PPS to less than 100 PPS in both the DME and XPDR Modes.
- _____ C. Squitter rate accurate to ± 1 count $\pm 0.5\%$
- _____ D. The pulse spacing is random in the DME Mode and regular in the XPDR Mode.

29. Generator Frequency Accuracy

- _____ A. Generator Frequency within $\pm 0.001\%$ of assigned frequency.
- _____ B. MHz Freq. Select
 - _____ 1. Gen. Freq. increments in 1 MHz steps as 1 MHz Freq. Select is incremented

- _____ 2. Gen. Freq. increments in 10 MHz steps
as 10 MHz Freq. Select is incremented
- _____ 3. Gen. Freq. increments in 100 MHz steps
as 100 MHz Freq. Select is incremented
- _____ C. Channel Freq. Select

Gen. Freq. is the assigned frequency for all
Channel Freq. Select positions
- _____ D. Remote Freq. Select

Gen. Freq. is the assigned frequency for all
Remote Freq. Select positions

30. UNCAL Control ΔF Control and ΔF Readout Accuracy

- _____ A. In Uncal mode generator frequency variable by
means of the ΔF Control
- _____ B. ΔF control varies generator frequency at least
± 2 MHz from the assigned frequency.
- _____ C. ΔF indicates within +0.01 MHz deviation of the
generator frequency from the CAL Frequency

31. Generator Frequency Spectrum

- _____ A. Generator frequency spectrum has no discrete
spurious outputs at any level greater than 60db
below the desired output level at any frequency
up to 1920 MHz
- _____ B. Generator frequency spectrum does not display more
than 30 KHz P.P. residual FM measured with a 1
KHz bandwidth _____ 960 _____ 1080 _____ 1215
- _____ C. Generator frequency spectrum at the -60db level
is not broader than 300 KHz measured with a 1
KHz bandwidth _____ 960 _____ 1080 _____ 1215
- _____ D. Generator frequency spectrum does not display
more than 50 KHz pulling due to modulation affects
_____ 960 _____ 1080 _____ 1215

32. R.F. CW Output Level Accuracy

- _____ A. R.F. level does not vary more than 1 db over the
frequency range of 962 MHz to 1213 MHz
- _____ B. R.F. level is -10± 0.5 dbm at the -10 dbm
attenuator setting for all freq. between 962 to
1213 MHz

- _____ C. Level variation centered about -10 dbm
 - _____ D. R.F. level attenuation below the -10 dbm level agrees with the attenuator dial setting to within $\pm 0.25\text{db}$ or ± 0.004 (Dial Setting - 10)db whichever is greater
 - _____ E. CW level available when the CW output control is placed in the ON position and the Mode Select Control is placed in the DME mode
33. Main Reply Pulse Level Accuracy
- _____ A. Peak amplitude of the main reply pulses is within $\pm 0.1\text{db}$ of the CW output level
34. Tacan Mod. Control
- _____ A. With Tacan Mod. Control ON, R.F. pulse amplitude is modulated by a composite 15 Hz and 135 Hz signal
 - _____ B. Each component has a modulation factor of 15% - 25%
35. Video Output Monitor
- _____ A. Video output monitor displays either the demodulated CW level or R.F. pulses originating internally in either the DME Mode or the XPDR mode
36. Echo Injection
- _____ A. Echo pulses appear when the Echo Injection control is in the "ON" position
 - _____ B. 0 db setting the Echo Pulse Pair Amplitude is within 0.1db of the Main Reply Amplitude.
 - _____ C. -6db setting the Echo Pulse Pair amplitude is $-6 \pm 0.5\text{db}$ below the Main Reply Amplitude
 - _____ D. Echo Pulse Pair occurs at a range of 30 ± 1 NM
 - _____ E. Echo Pulse Pair spacing is 12 ± 1 usec in X Mode and 30 ± 1 usec in Y mode
37. R.F. ON-OFF Ratio
- _____ A. RF CW level is at least 80 db below the RF Pulse peak amplitude between pulse intervals
38. Mode Select Control
- _____ A. P1-P2 spacing in X position correspond to X mode

- _____ B. P1-P2 spacing in Y mode corresponds to Y mode
- _____ C. P1-P2 spacing in the AUTO X-Y Mode corresponds to X Mode when Remote Frequency control is in X Mode or Channel Frequency select is in XXX.X0 or corresponds to Y Mode when Remote Frequency control is in Y Mode or Channel Frequency control is in XXX.X5
- _____ D. In A, B, C, D, or A-C positions the XPDR Interro P1-P3 pulse spacing corresponds to that mode
- _____ E. No pulses originated internally in EXT. position

39. P2 Deviation Control

- _____ A. P1-P2 pulse spacing varies in accordance with the P2 Deviation Control
- _____ B. 0 position on the control P1-P2 pulse spacing is 12 ± 0.1 usec in X mode and 30 ± 0.1 usec in Y mode
- _____ C. With control set at ± 4 usec the deviation is $\pm 4 \pm 0.3$ usec
- _____ D. P2 Pulse is not present when the P2 ON-OFF Control is in the OFF position

40. Power Readout Accuracy

- _____ A. Power Readout indicates zero power 0.4 sec after removal of the RF pulses
- _____ B. When RF input is decreased by a factor of 10 the Power Readout indicates a value in the range of $(10 \pm 0.5)\%$ of the previous reading
- _____ C. Power Readout is accurate to within ± 0.5 db when a 1 KW pulse is applied over the frequency range of 1025 MHz to 1150 MHz

41. Detected Output Monitor

- _____ A. The detected pulse monitor displays the demodulated envelope of either the DME Interrogation Pulses or the XPDR Reply pulses

42. Scope Sync. Control

- _____ A. With scope Sync. Control in the TO position there is a pulse present on the scope Sync. Output which is synchronous with the DME Interrogation P1 pulse or the XPDR Interrogation P1 pulse

- ☐ B. In the squitter position the sync. pulse is synchronous with each DME Squitter Pulse, Reply pulse, Ident Pulse, or the XPDR Interrogation P1 Pulse
 - ☐ C. In the TD position the sync. pulse is synchronous with the DME Reply pulse or the XPDR Interrogation P3 pulse.
43. Interrogation Rate Readout Accuracy
- ☐ A. Interro Rate Readout indicates to within ± 1 count the true DME Interro Rate
44. Range Delay Accuracy
- ☐ A. The Demodulator 50% Det. is set for 2 ± 0.05 usec delay
 - ☐ B. The Modulator 50% Det. is set for 2 ± 0.05 usec delay
 - ☐ C. Zero NMi delay accurate within ± 0.04 NMi
 - ☐ D. Range Delay accurate within ± 0.005 NMi per 100 NMi plus the zero NMi delay
45. -1 NMi Control
- ☐ A. Range decreases by 1 NMi when the -1 NMi switch is activated
 - ☐ B. "-1NMi" appears in readout when switch is activated.
46. Pulse Priority
- ☐ A. Pulses have the following priority: Ident pulses, reply pulses, and squitter pulses
 - ☐ B. Squitter pulses are inhibited so that they do not occur closer than 50 usec of the reply pulses
47. Ident Control and Equalizing Pulse Control
- ☐ A. When the Ident. Control is placed in the Ident. position the code KID is generated
 - ☐ B. When placed in the Tone position a continuous string of pulses appear
 - ☐ C. Repetition rate of the pulses is 1350 PPS
 - ☐ D. When the Equalization Pulse control is placed in the ON position a pulse pair appears 100 ± 10 usec after each Ident. pulse pair.

47 Cont'd.

_____ E. At least a 5 sec interval between Ident Code cycles

48. Flag Alarm Level

_____ When the voltage on Flag Alarm Receiver input is 1.0 volt or less the Readout Blanks in the Meas. Dist. Mode.

49. Frequency Monitor Output

_____ A. At the Freq. Monitor output a beat frequency appears which is the difference between the Generator frequency ± 63 MHz and the DME Transmitter frequency

_____ B. In the XPDR mode the beat frequency is the difference between the Generator frequency ± 60 MHz and the XPDR Transmitter frequency

50. Calibrate Phase Control and Cal. Output

_____ A. With the Calibrate Phase Control in the 1.45 usec position there appears 1.45 usec pulse at the Cal. output

_____ B. Any delay can be overlaid by means of either a rising or falling edge of the 1.45 usec pulse

_____ C. A 1.0 usec phase variable pulse appears in the 1.0 usec position

51. XPDR Pulse Level

_____ A. Peak amplitude of the XPDR Interrogation P1 pulse is within ± 0.1 db of the CW output level

52. XPDR P2, P3 Suppression Control

_____ A. XPDR P2, P3 Pulse level varies with position of the XPDR suppression control

_____ B. 0db setting, peak amplitude is within ± 0.1 db of the CW output level

_____ C. At the -6db setting the amplitude is -6 ± 0.3 db below the CW output level

53. XPDR Pulse Width Control

_____ A. The XPDR RF Pulse width is ± 0.025 usec of the setting of the control

54. XPDR P2 Deviation Controls

_____ A. The P1-P2 spacing is within ± 0.025 usec of the setting of the XPDR P2 control

55. XPDR P3 Deviation Control and Interrogation Modes

- ☐ A. The P1-P3 spacing is within ± 0.025 usec of the setting of the XPDR P3 control
- ☐ B. 8 us A mode
- ☐ C. 17 us B mode
- ☐ D. 21 us C mode
- ☐ E. 25 us D mode
- ☐ F. A-C mode there are three A-mode interrogations to one C-mode interrogation
- ☐ G. EXT. mode -no XPDR interrogations

56. XPDR Double Interrogation Control

- ☐ A. With double interrogation ON-OFF control in the ON position, there follows each XPDR Interrogation a second Interrogation.
- ☐ B. Double Interrogation Control varies the delay of these pulses from 20-25 usec to 250-270 usec after P3

57. XPDR % Return Readout

- ☐ A. The ratio of XPDR returns to Interrogations is accurate to within ± 1 count

58. Remote Operation

- ☐ A. When Frequency Sel. Control is in Remote the Generator Freq. is determined by the inputs to the rear connector only
- ☐ B. When Remote Control is placed in ALL Remote position all functions listed are controllable from the rear connectors.

59. Regulator Voltage Accuracy	
<u>Reg.</u>	<u>Output Voltage Range</u>

Reg.	Output Voltage Range	120V	100V	Ripple @100V
A. 28V	28±0.05V	_____	_____	_____
B. +16V	16± 0.20V	_____	_____	_____
C. +10V	+10 ± 0.05V	_____	_____	_____
D. +5V	+5 ± 0.05V	_____	_____	_____
E. -5V	-5 ± 0.20V	_____	_____	_____
F. -10V	-10 ±0.20V	_____	_____	_____
G. -28V	-28 ± 0.30V	_____	_____	_____
H. +16±2V	+16 ± 2V	_____	_____	_____

[illegible]

Squawk/Naut S/N _____

Date _____

Final Test Preformed By

CHECK LIST

1. With the Freq. Gen. Channelled to 960 MHz the ΔF VCO VT voltage is in the range of 0.95 to 1.00 volts.

+ ΔF _____ - ΔF _____

2. With the Freq. Gen. Channelled to 1230 MHz the ΔF VCO VT changes by $+0.3 \pm 0.05$ volts when the ΔF VCO ΔF line is shorted and recovers immediately when the short is removed.

+ ΔF _____ - ΔF _____

3. The Master VCO RF output is at least +21 dbm and flat to within 1 db over the freq. range of 960 to 1220 MHz _____

The Master VCO VT is in the range of 15 to 17 Volts when the freq. is 1200 MHz _____

With the Master VCO VT shorted to ground the freq. is less than 900 MHz _____

4. The delay between the 0.5 Amplitude point on the rising edge of the P1 pulse, as observed at the Video Output Monitor, and the falling edge of the pulse on the Mod 50% Level Pulse line, G18-34, may be varied by means of the Mod 50% Level pot over the range of 2.0 ± 0.2 usec. _____

5. The leads of the ΔF Osc. transistor, Q1, may be mechanically probed without causing loss of "lock." _____

6. Is the EMI Filter Capacitor correctly installed _____.

ENVIRONMENTAL RECORD

	Date
1. Temperature Chamber Cycle	_____
2. 7 Day Burn In	Start _____
	Stop _____
3. Timer On-Off	Start _____
	Stop _____

Record Of Component Failures

COMPONENT CROSS REFERENCE

KPN	VENDOR PART NUMBER	TYPE	DESCRIPTION	VENDOR
007 0002 00	40407	TRANS	POWER, NPN	RCA
007 0004 00	40406	TRANS	POWER, PNP	RCA
007 0008 00	SE4002	TRANS	GEN.PURPOSE,NPN	F
007 0009 00	2N4249	TRANS	GEN.PURPOSE,PNP	NAT
007 0025 00	2N3646	TRANS	SWITCH, NPN	NAT
007 0026 00	2N5208	TRANS	RF SIGNAL, PNP	MOT
007 0027 00	2N4917	TRANS	SWITCH, PNP	NAT
007 0028 00	2N3866	TRANS	RF POWER, NPN	RCA
007 0029 00	2N4919	TRANS	POWER, PNP	MOT
007 0030 00	2N4922	TRANS	POWER, NPN	MOT
007 0032 00	2N3054	TRANS	POWER, NPN	RCA
007 0033 00	2N3771	TRANS	POWER, NPN	RCA
007 0034 00	3N128	TRANS	MOSFET	RCA
007 0035 00	MM8009	TRANS	RF POWER, NPN	MOT
007 0036 00	2N6027	TRANS	PROGRAMMABLE UNIJUNCTION,PUT	G.E.
007 0037 00	2N5457	TRANS	JFET, N CHANNEL	NAT
007 4000 00	MVI2098	DIODE	VARACTOR	MOT
007 5069 00	1N4753A	DIODE	ZENER, 36V	MOT
007 6016 00	1N4148	DIODE	COMPUTER	TI
007 6018 00	1N4436/F/T	DIODE	RECTIFIER	VARO
007 6019 00	VT200/T	DIODE	RECTIFIER,25A	VARO
007 6020 00	1N270	DIODE	GEN.PURPOSE GERMANIUM	TRAN

NOTE: ALL TRANSISTORS AND DIODES ARE SILICON UNLESS OTHERWISE NOTED.

KPN	VENDOR PART NUMBER	TYPE	DESCRIPTION	VENDOR
007 6021 00	5082-2800	DIODE	HOT CARRIER	HP
007 6022 00	5082-2900	DIODE	HOT CARRIER	HP
007 6023 00	5082-3041	DIODE	PIN	HP
007 6024 00	5082-0112	DIODE	SRD	HP
007 6025 00	243	DIODE	BAND SWITCH	ITT
007 6026 00	1N4738A	DIODE	ZENER, 8.2V	MOT
007 6030 00	5082-3529	DIODE	PIN	HP
007 7001 00	9946	IC,DTL	QUAD,2-INPUT NAND	F
007 7002 00	9930	IC,DTL	DUAL 4-INPUT EXTENDABLE NAND	F
007 7003 00	9936	IC,DTL	HEX INVERTER	F
007 7005 00	N8281A	IC,TTL	4-BIT BINARY COUNTER	SIG
007 7006 00	N8280A	IC,TTL	BCD DECADE COUNTER	SIG
007 7013 00	UA723	IC,LINEAR	VOLTAGE REGULATOR	F
007 7032 00	9602	IC,TTL	DUAL ONE SHOT	F
007 7039 00	SN76010N	IC,LINEAR	AUDIO AMPLIFIER	TI
007 7042 00	UA741	IC,LINEAR	OP AMPLIFIER	F
007 7043 00	LM304	IC,LINEAR	NEG.VOLTAGE REGULATOR	NAT
007 7044 00	LM306H	IC,LINEAR	VOLTAGE COMPARATOR	NAT
007 7045 00	LM311H	IC,LINEAR	VOLTAGE COMPARATOR	NAT
007 7046 00	UA710	IC,LINEAR	VOLTAGE COMPARATOR	F
007 7047 00	SN7400N	IC,TTL	QUAD 2-INPUT NAND	TI
007 7048 00	SN7402N	IC,TTL	QUAD 2-INPUT NOR	TI
007 7049 00	SN7404N	IC,TTL	HEX INVERTER	TI
007 7050 00	SN7405N	IC,TTL	HEX INVERTER, OPEN COLLECTOR	TI

KPN	VENDOR PART NUMBER	TYPE	DESCRIPTION	VENDOR
007 7051 00	SN7410N	IC,TTL	TRIPLE 3-INPUT NAND	TI
007 7052 00	SN74H11N	IC,TTL	TRIPLE 3-INPUT AND	TI
007 7053 00	SN74H21N	IC,TTL	DUAL 4-INPUT AND	TI
007 7054 00	SN7442N	IC,TTL	BCD to DECIMAL DECODER	TI
007 7056 00	SN7451N	IC,TTL	DUAL 2-INPUT AND/OR/INVERT	TI
007 7057 00	SN7473N	IC,TTL	DUAL J-K FF	TI
007 7058 00	SN7474N	IC,TTL	DUAL TYPE D FF	TI
007 7059 00	SN7490N	IC,TTL	DECADE COUNTER	TI
007 7060 00	SN7493N	IC,TTL	4-BIT BINARY COUNTER	TI
007 7061 00	SN7495N	IC,TTL	4-BIT SHIFT REGISTER	TI
007 7062 00	SN74165N	IC,TTL	8-BIT SHIFT REGISTER	TI
007 7063 00	SN74192N	IC,TTL	SYNCHRONOUS 4-BIT UP/DOWN COUNTER	TI
007 7067 00	9109	IC,TTL	HIGH VOLTAGE HEX INVERTER	F
007 7068 00	9309	IC,TTL	DUAL 4-INPUT MULTIPLEXER	F
007 7069 00	9322	IC,TTL	QUAD 2-INPUT MULTIPLEXER	F
007 7070 00	9601	IC,TTL	ONE-SHOT	F
007 7071 00	MC1806P	IC,DTL	QUAD 2-INPUT AND	MOT
007 7072 00	CD2501E	IC,TTL	BCD to 7-SEGMENT DECODE	RCA
007 7073 00	MC1004P	IC,ECL	DUAL 4-INPUT OR/NOR	MOT
007 7074 00	MC1010P	IC,ECL	QUAD 2-INPUT NOR	MOT
007 7075 00	MC1035P	IC,ECL	TRIPLE LINE RECEIVER	MOT
007 7076 00	MC3001P	IC,TTL	QUAD 2-INPUT AND	MOT

KPN	VENDOR PART NUMBER	TYPE	DESCRIPTION	VENDOR
007 7077 00	MC3002P	IC,TTL	QUAD 2-INPUT NOR	MOT
007 7078 00	MC3006P	IC,TTL	TRIPLE 3-INPUT AND	MOT
007 7079 00	MC3062P	IC,TTL	DUAL J-K FF	MOT
007 7080 00	MC4016P	IC,TTL	PROGRAMMABLE MODULO-N DECADE COUNTER	MOT
007 7081 00	MC4044P	IC,TTL	PHASE-FREQUENCY DETECTOR	MOT
007 7082 00	uA733	IC,TTL	DIFFERENTIAL VIDEO AMPL.	F
007 7084 00	MC1810P	IC,DTL	QUAD 2-INPUT NOR	MOT
007 7085 00	SN74H103N	IC,TTL	DUAL J-K FF	TI

RCA	-	RADIO CORPORATION of AMERICA
F	-	FAIRCHILD
NAT.	-	NATIONAL
MOT.	-	MOTOROLA
G.E.	-	GENERAL ELECTRIC
TI	-	TEXAS INSTRUMENTS
VARO	-	VARO SEMICONDUCTOR
TRAN	-	TRANSITRON ELECTRONICS, INC.
HP	-	HEWLETT PACKARD
ITT	-	ITT SEMICONDUCTOR
SIG	-	SIGNETICS