ANALOG DEVICES

ANALOG CIRCUIT DESIGN SEMINAR

Analog Circuit Design Seminar

Introduction

In the last decade, substantial progress has been made in the design, processing, and volume manufacture of integrated circuits. Most of the attention has been focused on advances in digital circuitry – microprocessors, memories, gate arrays, and the like. However, the linear IC field has progressed at a rate which matches (and in many respects, exceeds) the achievements of digital ICs. New processes, refined existing processes, and new designs have made possible a wide variety of linear integrated circuits which permit more sophisticated analog measurement, control and signal conditioning functions.

This seminar examines not only the range of available products, but also the important aspects of applying these products successfully. Section I is devoted to operational amplifiers – the basic building block linear IC. Special attention will be given to the details of selecting an amplifier for a particular application. Practical circuit considerations such as decoupling and grounding, passive component selection, and loading will be discussed.

Section II examines a class of specialized amplifiers known as Instrumentation Amplifiers. These amplifiers are useful in signal conditioning applications where precise gain is required in the presence of common-mode voltages and other interfering signals. The issues of device selection, proper application, and performance limitations as they relate to accurate signal amplification are discussed.

Section III covers analog computational circuits. Many real-time operations (such as logarithms, multiplication, division, squaring, square-rooting) can easily be implemented with low cost integrated circuits which can eliminate many of the problems associated with digital signal processing. Several types of computational circuit are discussed in detail, along with application examples.

Several appendices which the analog circuit designer will find useful are included at the end of the book for future reference.

Analog Devices is well-established as a major supplier of precision analog integrated circuits and data converters. Design and process innovation combined with careful product planning underscore our committment to serving the needs of instrumentation, process control, and avionics systems designers.

In addition, we have always been committed to providing the user with the highest level of technical support available as an aid in state-of-the-art system design and application of high performance components. This seminar is an example of the continuing support to that commitment; we hope it will be of help in understanding and applying the new monolithic amplifiers and analog computational ICs.

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April 1982

Section I

Operational Amplifiers

Operational Amplifiers

1. Basic Concepts
2. Technological Considerations
3. Selecting the Right Amplifier for the Application
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1. BASIC CONCEPTS IN OPERATIONAL AMPLIFIERS

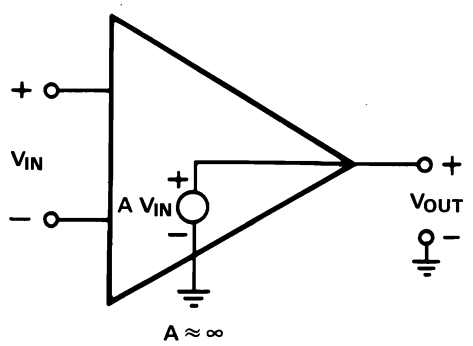
BASIC OP AMP CONCEPTS

- **The Ideal Model**
- **The Non-Ideal (Real) Amplifier**
- **Definitions of Specifications and Testing**

THE UBIQUITOUS OP AMP

The operational amplifier is the most commonly-used analog component. Op amps are available in a wide variety of technologies, specifications, prices, and even package styles from a multitude of vendors. When a circuit requires an operational amplifier, the designer is confronted with an absolutely bewildering number of amplifiers to choose from. This seminar will serve to make the selection process somewhat simpler.

Op amps are modeled as amplifiers with differential inputs, single-ended outputs, and infinite gain at all frequencies. In most designs, it is assumed that the amplifier is, in fact, ideal. It is assumed that no current flows into the input terminals, there is no offset voltage at the inputs, and no power is required for operation.



IDEAL OP AMP

THE REAL OP AMP

Input Imperfections

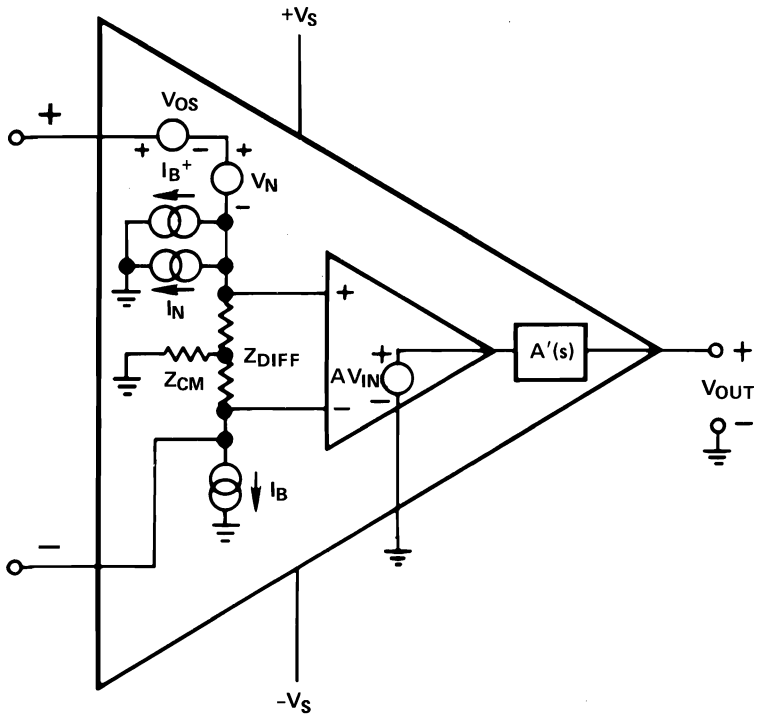
The actual characteristics of real op amps are considerably more complicated, of course. The inputs each have a dc current source (I_B) connected to them. A series dc voltage source (V_{OS}) appears in series with one input. An impedance (Z_{IN} diff) appears between the inputs, and another (Z_{INCM}) appears between the inputs and ground. These impedances usually consist of a resistance and capacitance in parallel, and the finite Z_{CM} will introduce errors due to common-mode input voltages.

There are two additional input error sources. In addition to the dc voltage and current sources, small ac sources representing the noise components must be included in the model.

Output Obstacles

The output side of the model is also nonideal. First, an output impedance, R_O, is added in series with the voltage source. The "A" term (infinite in the ideal model) is both finite and a function of frequency in a real amplifier. It is also obvious that the output voltage and current capabilities of a real op amp are bounded.

The real amplifier, thus, can be modeled as follows:



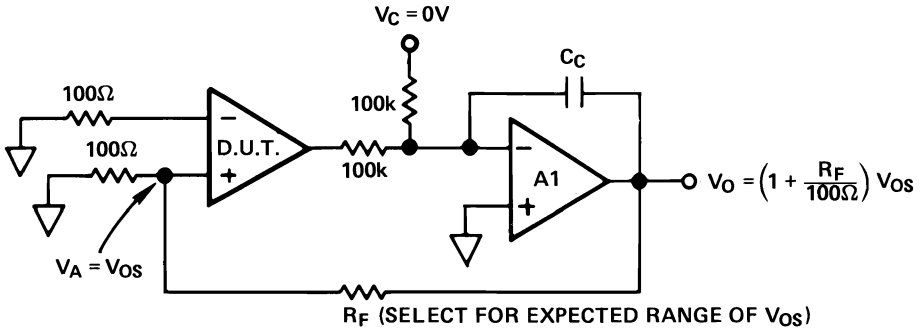
REAL OP AMP

OP AMP SPECIFICATIONS

Offset Voltage

Each of these nonideal specifications should be examined in some detail. Consider first the dc errors. Offset voltage is the result of a mismatch in the base-emitter voltages of the differential input transistors (or gate-source voltage mismatch in FET-input amplifiers). This offset voltage is indistinguishable from an input signal as far as the amplifier is concerned. Usually this offset can be trimmed to zero by the user by means of an external potentiometer, which adjusts the balance of the operating currents in the input stage until the V_{BE}s (or V_{GS}s) are equal. This trim may be effective only at one temperature, since offset voltage changes as a function of temperature.

Many circuits exist for testing offset voltage. If V_{OS} is defined as the voltage at the op amp input which will drive the output to zero in an open-loop circuit, a servo loop can be built around the device under test to determine that voltage. In the circuit shown below, a second amplifier is used to provide feedback. This feedback amplifier must have very high gain and low offset. In operation, the control voltage, V_C, is set to zero. This forces the output of the device under test (D.U.T.) to also go to zero, because no dc current can flow through the amplifier's feedback capacitor. Since the output of the D.U.T. will only go to zero when a voltage equal to its input offset voltage is applied to its input, then V_A must equal V_{OS}. Thus, the output of the feedback amplifier is equal to V_{OS} times (1+R_F/100 ohms).

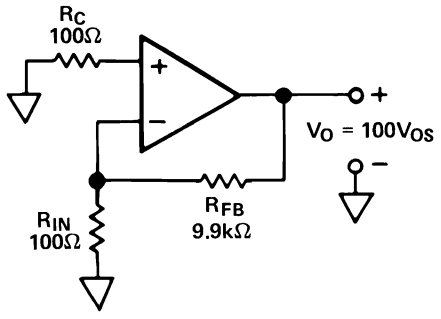


OP AMP OFFSET VOLTAGE TEST CIRCUIT

An alternate method for offset voltage measurement can also be used. This alternate circuit is simpler to build and is only slightly less accurate. If it is assumed that V_{OS} can be modeled as a source connected in series with one input, configuring the amplifier for a fairly high closed-loop gain will allow reasonably accurate measurement of offset voltage with an inexpensive voltmeter.

In order to maintain accuracy in this measurement, R_{IN} should be low enough that I_{OS} flowing through R_{IN} is at least ten times lower than the expected value of V_{OS}. R_C causes an equal voltage to be developed at each input. This common-mode voltage effect can be neglected due to the common mode rejection of the op amp. Reasonable values for R_{IN}, R_{FB}, and R_C are 100 ohms, 9.9k ohms, and 100 ohms respectively.

Another error arises in this circuit due to the finite open loop gain of the amplifier. Assuming a test circuit gain of 100, the amplifier must have a dc open-loop gain of at least 10,000 for a 1% accurate V_{OS} measurement.



SIMPLE V_{OS} TEST CIRCUIT

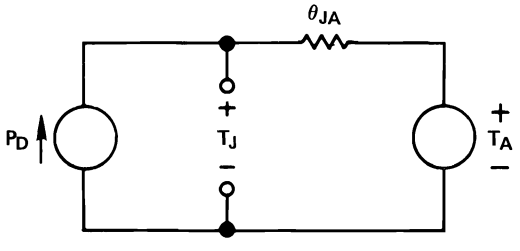
Input Bias Current

Another dc error term is the input bias current. As a consequence of the practical characteristics of transistors, base current must be supplied to the input transistors to bias them into their active operating region. This current must also return to its originating point through some dc path. Thus operational amplifiers can not be used with input signal sources which are not referred to the same power source as the amplifier. It is possible to reduce bias current-induced errors by providing a source (other than the signal path) which can leak this current.

In many applications, the errors due to bias current are actually less annoying than the errors caused by the mismatch of the bias currents on the two inputs. This difference between the bias currents is called the input offset current, and is usually specified along with the bias current.

Input currents, like the input offset voltage, vary as a function of temperature. In the case of a bipolar-input amplifier, bias current decreases at elevated temperature. This is because the transistors' β increases, and since the emitter current is constant, the base current decreases. In the case of a FET-input amplifier, the bias current is due to JFET gate leakage, which is in reality a reverse-biased junction leakage current. Such currents have the characteristic of doubling for every 10°C rise in junction temperature.

It is important to consider the test conditions under which bias current is specified, particularly in the case of a FET-input op amp. Some manufacturers specify bias current at a junction temperature of 25°C. This corresponds roughly to the bias current immediately after power is applied to the amplifier. Unfortunately most circuits are not operated in a pulsed mode, and the effects of amplifier self-heating must be considered. This effect is, in many cases, not trivial. For example, an amplifier which draws 5 milliamps of supply current from ±15 volt supplies dissipates 150 milliwatts. The thermal resistance from junction to ambient for 8-lead IC packages is typically 150°C/W. This means that the junction temperature of the amplifier in question will be 22.5°C above ambient temperature, and the bias current will be over 4 times as high as a specification based on 25°C junction temperature.



θ_{JA} = 150°C/W FOR TO-99 TYPE PACKAGES
= 155°C/W FOR EPOXY MINI-DIP
= 100°C/W FOR 14/16 PIN CERAMIC DIP

THERMAL CIRCUIT MODEL FOR IC OP AMP

CONSIDER AN OP AMP
SPECIFIED FOR 50pA I_B AT T_J = 25°C

If the Amplifier Draws 5mA from ±15V,

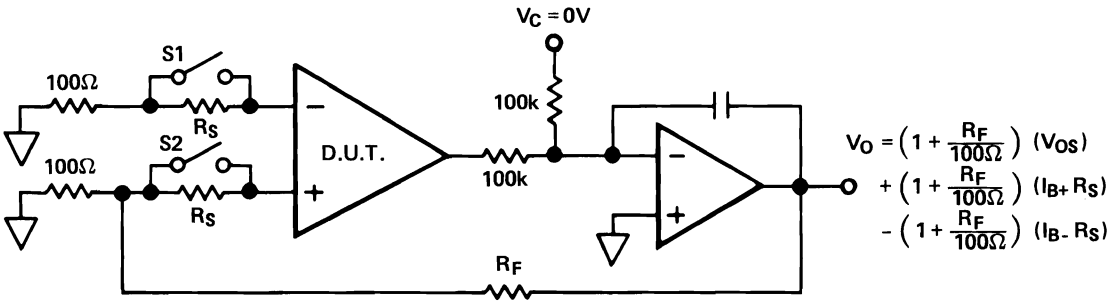
$P_D = 30 \times 5 = 150mW$

$T_J = T_A + (150mW \times 150°C/W)$

$= 25°C + 22.5°C$

Therefore, I_B will be Four Times Higher than Spec.

Bias current can be measured with essentially the same method used to measure offset voltage. The difference is that a large resistance is inserted in series with the input under test, creating an additional offset voltage equal to $I_B \times R_S$. Assuming the actual V_{OS} has been measured and recorded, the change in apparent V_{OS} due to the change in R_S can be determined and I_B easily computed. Offset current is tested by computing the difference between the bias current on the inverting input and the bias current on the noninverting input. Typical R_S values range from 100kΩ for bipolar input amplifiers to $10^{10}\Omega$ for some FET-input types.



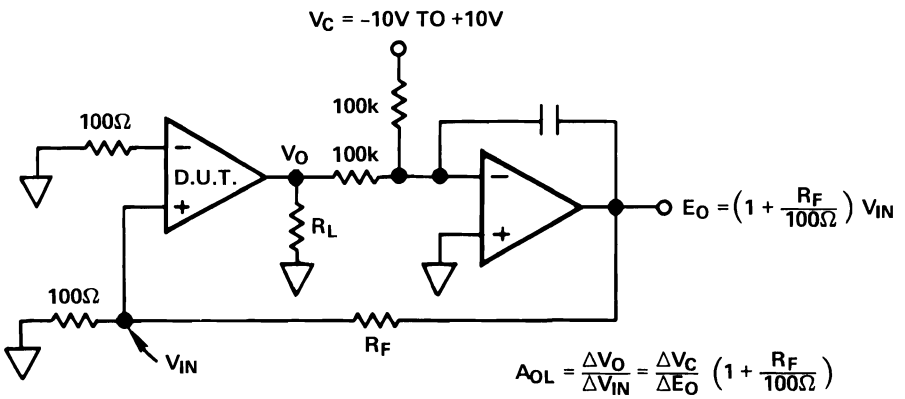
$R_S >>> 100\Omega$
S_1 IS CLOSED TO TEST I_{B+}
S_2 IS CLOSED TO TEST I_{B-}
BOTH CLOSED TO TEST V_{OS}
BOTH OPEN TO TEST I_{OS}

BIAS/OFFSET CURRENT TEST CIRCUIT

Open Loop Voltage Gain

Another op amp parameter which distinguishes a real amplifier from an ideal amplifier is open-loop gain. In the ideal op amp model, open loop gain is assumed to be infinite. The same assumption is also sometimes made when dealing with real amplifiers (with unfortunate results, as will be demonstrated later in this chapter.)

Open-loop gain of an operational amplifier is an interesting parameter to attempt to measure. It is generally not practical to measure open loop gain directly by applying a signal at the input and observing the output change. However, by using the device under test inside a feedback loop it is possible to measure the change in input voltage required to produce a known change in output voltage.

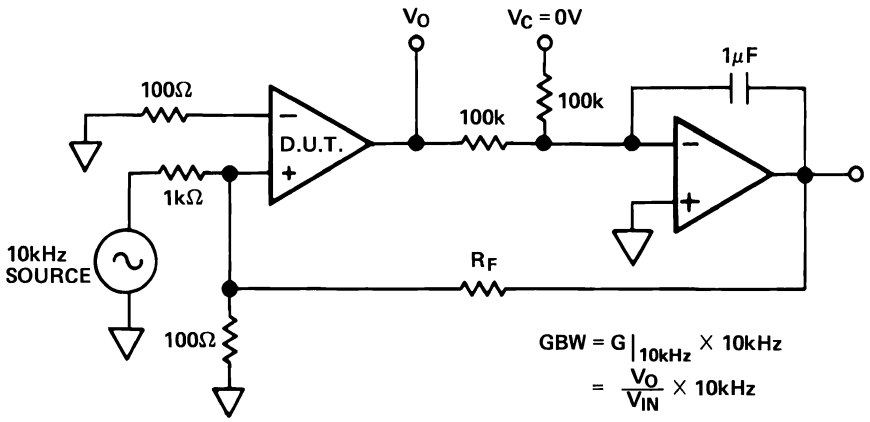


OPEN LOOP GAIN TEST CIRCUIT

In this circuit, the control voltage, V_C, is varied from -10V to +10V, causing the D.U.T. output, V_O, to vary from +10V to -10V. The D.U.T. output is varied by a change in V_{IN} produced by the second amplifier. Since V_{IN} is attenuated from E_O by the R_F/100 ohm voltage divider. E_O is easily measured, and open loop gain can readily be computed.

Frequency Response

Open-loop gain versus frequency is another difficult-to-test specification. Bandwidth is usually specified in terms of gain-bandwidth product or unity-gain small signal bandwidth. It is assumed that the amplifier under test has an open-loop gain versus frequency plot which decreases with a -20dB/decade slope. It is, therefore, possible to measure the open-loop gain at some known frequency and predict the frequency at which the open-loop gain will be unity.



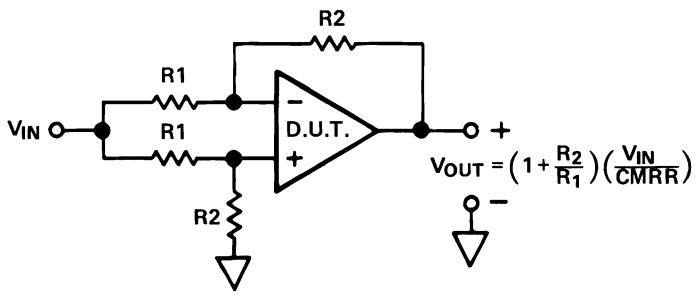
GAIN-BANDWIDTH PRODUCT TEST CIRCUIT

In the circuit shown, the D.U.T. dc output is held to 0 volts by V_C and the integrator amplifier. A low amplitude 10kHz ac input signal is applied to the D.U.T. Since the integrator has very low gain at 10kHz, the D.U.T. is effectively running open-loop for the ac signal. The ac output from the D.U.T. can be measured and the gain at 10kHz can be computed. For example, a 741-type amplifier has an open loop gain of approximately 100 at 10kHz. Thus, an easily generated 100mV input at the D.U.T. input will produce an easily measured 10V output. This corresponds to a 1MHz gain-bandwidth product.

Common-Mode Rejection Ratio

The ideal operational amplifier is a pure differential amplifier and is insensitive to the absolute voltage on the inputs with respect to ground. The real amplifier has several nonideal characteristics associated with input levels. First, of course, is the allowable range of input voltage. Most IC op amps will only operate when the voltages on the input terminals are within the range bounded by the supply voltages. The second, and perhaps more subtle, characteristic is the common-mode rejection ratio (CMRR). CMRR is defined the ratio of the change in common mode to the resulting change in input offset voltage. It is often convenient to specify this parameter logarithmically in dB: CMR = 20 log (CMRR).

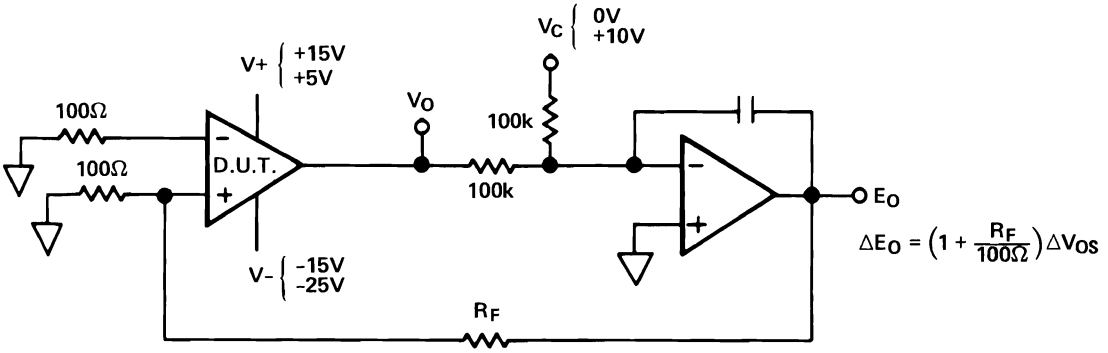
Common-mode rejection can be measured several ways. One method uses four precision resistors to configure the op amp as a subtractor amplifier. The disadvantage inherent in this circuit is that the ratio match of the resistors also determines the subtractor's CMRR. A mismatch of 0.1% between resistor pairs will result a CMR of only 60dB. Since most amplifiers exhibit CMR in excess of 80dB (some as high as 120dB), it is clear that this circuit is only marginally useful.



RESISTORS MUST MATCH WITHIN 1ppm (0.0001%)
IN ORDER TO MEASURE CMR>100dB

SIMPLE CMR TEST CIRCUIT

A better circuit uses a technique similar to that used for measuring offset voltage with one exception. Rather than applying a fixed zero volt input to the D.U.T. operating on plus/minus 15 volt supplies, the same input is applied to the D.U.T. with asymmetrical power supplies, such as +5V and -25V. The output of the amplifier is forced to remain centered between the supplies and the input voltage to the D.U.T. which forces this to occur is measured.



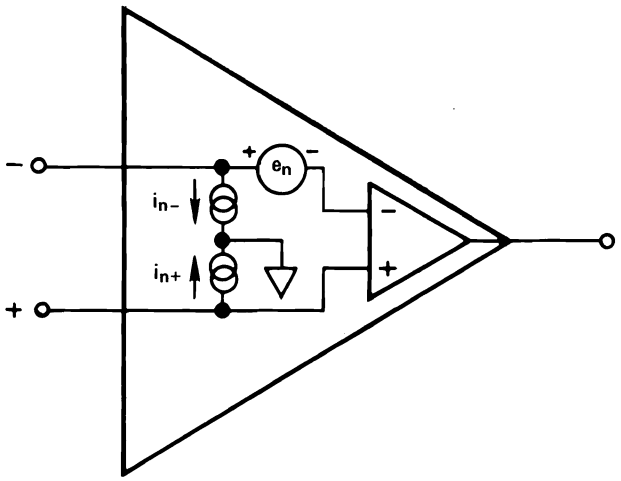
COMMON-MODE REJECTION TEST CIRCUIT

The change in V_{OS} can be readily translated into CMR. If this 10Vchange in CMB creates a 1 millivolt change in V_{OS}, the CMRR is 10000 and the CMR is 80dB.

Noise

There are two types of noise existing in circuits using op amps. The first type of noise will be referred to here as "interference". This is noise which originates from sources not related to the actual circuit. Such noise sources include ground and power-supply noise created by other circuitry in a system, stray electromagnetic pickup of line frequency energy (and the harmonics thereof), broadcasting stations, contact arcing in mechanical switches, and transients due to switching in reactive circuits. Even mechanical vibration can create noise in high impedance amplifier circuits. This external noise can often be minimized or even eliminated, once the interfering source is identified and appropriate actions are taken.

The second type of noise is the inherent noise of the circuit itself. Unlike interference, it cannot be totally eliminated since it is caused by components in the actual circuit such as resistors and sources within the amplifier. The best that can be accomplished is minimizing the noise in a specific bandwidth of interest. To effectively do this, it is important to construct reasonably accurate models of the noise sources in op amps. There are essentially three sources of noise to consider in op amps. The first is the input noise voltage, and the other two are the noise components of the bias current at the two inputs.



VOLTAGE AND CURRENT NOISE MODEL

Since these noise sources are assumed to be aperiodic and not regularly recurring, we shall consider them in terms of their statistical properties—rms value, peak value, and frequency content. Measurement of the rms value of a random noise waveform requires an averaging interval which is long compared to the period of the lowest frequency of interest. The rms noise value is a useful and meaningful way to characterize the amount of noise generated by an amplifier.

$$E_n^2 = \int_0^T e_n^2(t)dt$$

where E_n (rms) is the rms noise voltage value

T is the interval of observation

e_n is the instantaneous noise voltage

Low frequency noise is difficult to measure, since very long observation intervals are needed. In some cases, low frequency noise is measured by direct observation on a storage-type oscilloscope screen using very slow sweep periods.

Since the noise most often encounted is for all practical purposes Gaussian in its amplitude distribution, it is possible to use the rms value to predict the approximate peak-to-peak amplitude. For instance, multiplying the rms value by a factor of 6.6 will yield a peak-to-peak value which will only be exceeded 0.1% of the time. The table below shows the relationship between rms and peak-to-peak values.

RMS TO PEAK-TO-PEAK RATIOS

Nominal Peak-to-Peak	% of Time Noise will Exceed Nominal Peak-to-Peak Value
2 X rms	32%
3 X rms	13%
4 X rms	4.6%
5 X rms	1.2%
6 X rms	0.27%
6.6 X rms	0.10%
7 X rms	0.046%
8 X rms	0.006%

Types of Noise
Noise encounted in op amp circuits can be generally classified into a few specific categories:

Johnson Noise
Thermal agitation of electrons in resistive circuit elements results in random movement of charge through the resistive material. This flow of random current through a resistance creates a voltage. Johnson noise can be computed from the formula:

JOHNSON NOISE VOLTAGE

$$E_N \text{ (rms)} = \sqrt{4kTRB}$$

Where: k = Boltzmann's Constant (1.374×10^{-23} J/°K)
T = Temperature in °K
R = Resistance in Ohms
B = Bandwidth in Hertz

At room temperature, this expression simplifies to

SIMPLE JOHNSON NOISE FORMULAE

$$E_N \text{ (rms)} \approx \frac{1}{8}\sqrt{RB} \quad \text{or} \quad e_n \approx 4\sqrt{R}$$

E_N = Total Noise in μV rms
R = Resistance in Kilohms
B = Bandwidth in Kilohertz

e_n = Spectral Density in $nV/\sqrt{Hz}$
R = Resistance in Kilohms

As a reference point, a 1kΩ resistor produces 4nV/Hz white noise, or 120nV (0.12V) rms noise in a 1kHz bandwidth. Johnson noise is generally less important inside the amplifier than it is in the external resistors in the circuit. In many circuits the noise of external resistors is much higher than amplifier-generated noise.

"Flicker" or "1/f" Noise
Flicker noise is usually the dominant noise source at frequencies below approximately 100Hz. Noise with "1/f" characteristic has a power spectrum which is inversely proportional to frequency; thus the voltage noise will be inversely proportional the square root of frequency. It is interesting to note the 1/f noise contains equal amounts of noise in any decade (or octave) of frequency. Noise with this spectral characteristic is also called "pink" noise.

"Shot" (or Schottky) Noise

Shot noise arises whenever current passes through a transistor junction. Shot noise is generally expressed as a current and follows the predictable form:

SHOT NOISE

$$I_N = 5.7 \times 10^{-4} \sqrt{I_J B}$$

Where I_N is Noise Current in Picoamps rms
I_J is Junction Current in Picoamps
B is Bandwidth of Interest (in Hertz)

As the noise current flows through various circuit impedances inside the amplifier it produces a noise voltage. Shot noise can be considered a "white" noise source and is the dominant contributor to amplifier noise at high frequencies.

Popcorn Noise

Occasionally a transistor will exhibit an erratic 1 to 100Hz fluctuation between two values of h_{fe} as a result of surface irregularities of contaminants. If such a transistor is used in the differential input stage of an operational amplifier (and is biased at a constant I_E), the input bias current will jump between two values, creating a voltage noise as it flows through source and feedback impedances. Most amplifiers produced today are free from popcorn noise; however occasional bad lots are processed, warranting periodic screening.

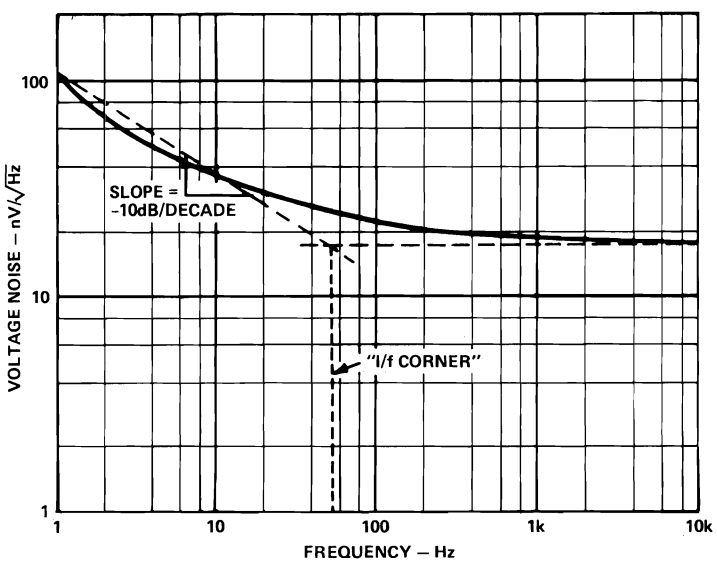
Noise Specifications

A complete data sheet for an operational amplifier should contain some noise specifications. Since it is not economically practical for a manufacturer to 100% test all op amps for noise, most noise specs quoted are typical. If noise is the most critical parameter in the application, many vendors are willing to screen amplifiers to a particular guaranteed maximum noise level (at additional cost).

Noise is often specified in terms of a graph of total noise up to a given frequency. Such curves are useful when the noise gain versus frequency characteristics of a circuit are known. It is important to consider both the voltage and current noise curves (and the gain to each versus frequency) in a computation of total noise.

Another useful set of specifications is a set of noise spectral density figures (at particular frequencies or plotted as a graph vs. frequency). Spectral noise density, e_n, at a given frequency is defined as the rms noise voltage in a 1Hz band surrounding a specified value of frequency. It is usually expressed in nanovolts per root hertz. The awkward units arise from the fact that it is noise power which is actually being characterized and e_n is proportional to the square root of the power spectral density.

A typical plot of noise voltage spectral density is shown below. At high frequencies, the shot noise dominates the total noise, while at low frequencies, the 1/f noise dominates. It is possible to graphically determine a useful figure of merit called the "1/f corner frequency" from this curve. This is done in much the same way as a lowpass filter response is approximated. Rather than determine a pole frequency from the intersection of the extensions of the 20dB/decade rolloff and the midband gain, the intersection of the 10dB/decade noise rolloff with the midband white noise density yields the 1/f corner frequency. Generally, the lower the 1/f corner frequency, the better the amplifier.



AD544/AD644 NOISE SPECTRAL DENSITY

If a curve is not supplied, usually a series of spot noise numbers at particular frequencies (10Hz, 100Hz, 1kHz, 10kHz) are given. These numbers are useful for direct comparison of noise characteristics of several amplifiers. Computation of total rms noise in a particular bandwidth requires that the shape of the spectral density curve be known. In the low frequency region, where the noise is primarily 1/f type, the noise at a particular frequency can be computed from the formula.

$$E_n = K\sqrt{\frac{1}{f}}$$

where K is the value of e_n at f = 1 Hertz.
The total l/f noise in a given bandwidth is given by

$$E_n = k\sqrt{\int_{f1}^{f2} \frac{df}{f}} = k\sqrt{\ln \frac{f2}{f1}}$$

Since total rms l/f noise is realted to the ratio of the low and high frequencies in the band of interest, it is possible to reduce this formula to the rule of thumb that a decade of bandwidth contributes an amount of noise equal to 1.52k (or, one octave contributes 0.83k). As an example, consider an amplifier with $e_n = 100nV/\sqrt{Hz}$ at 1Hz. The total l/f noise from 0.1 to 10Hz is therefore:

$$E_n = 0.1\mu V/\sqrt{Hz} \times 1.52\sqrt{\log \frac{10}{0.1}}$$

$$= 0.1 \times 1.52 \times \sqrt{2}$$

$$= 0.21\mu V$$

$$= 1.39\mu V \text{ p-p}$$

For white noise, the computation of total noise is also fairly straightforward. If ideal filters with infinitely steep skirts are used to determine the edges of a band containing constant noise density, the total rms noise can be expressed as:

$$E_n = \sqrt{\int_{f1}^{f2} e_n^2 \, df} = e_n\sqrt{f_2 - f_1}$$

Furthermore, if f_1, (the low frequency limit) is less than 10% of f_2, then f_2 can be ignored with about 5% error. Thus, if an amplifier exhibiting $10nV/\sqrt{Hz}$ white noise is observed in a filter with a steep cutoff at 10kHz the total noise will be

$$E_n = 10nV/\sqrt{Hz} \times \sqrt{10^4} \quad Hz$$

$$= 1\mu V \text{ rms}$$

$$= 6.6\mu V \text{ p-p}$$

Of course, ideal filters are difficult to obtain. Fortunately the measurement error induced by a single pole low pass filter is easy to compute. The noise in the spectrum above the filter's cutoff frequency has the effect of extending the filter's apparent corner frequency to 1.57 times the original f_c. Thus the low pass filter cutoff frequency should be chosen to be 0.66 f_h to observe total white noise in the bandwidth to f_h. Similarly, a 2 pole filter has an apparent corner frequency of 1.2 f_c.

Noise sources in op amps are considered to be uncorrelated, and can thus be added by the root-sum-of squares method. It is an interesting feature of this method that whenever two terms are being "RSS" added and one term is 3 times greater than the other, the smaller term can be ignored with little error. For example:

$$\sqrt{3^2 + 1^2} = \sqrt{10} = 3.16$$

$$\sqrt{3^2} = 3$$

ERROR $\approx$ 5%

The key points to remember about noise in op amps, then, are:

SUMMARY OF OP AMP NOISE SPECS

1. Low Frequency Noise Generally Follows a "1/f" (Actually $1/\sqrt{f}$) Characteristic. Total rms Noise in a 1/f Region can be Computed from $E_n = 1.52k\sqrt{\log \frac{f_2}{f_1}}$, Where $k = e_n$ at 1Hz.
2. High Frequency Noise Generally Follows a White Noise Characteristic. Total rms White Noise is Computed from $E_n = e_n\sqrt{f_2 - f_1}$ (or Simply $e_n\sqrt{f_2}$, if $f_2 \geqslant 10f_1$).
3. The "1/f Corner Frequency" can Serve as a Figure of Merit for Comparing Amplifiers.
4. Broadband Noise Test Circuits Should Use Filter Cutoff Frequencies Set for 2/3 of the Desired Bandwidth, to Allow for the Slope of the Filter's Roll-Off.
5. Uncorrelated Noise Sources Add in a Root-Sum-of-Squares Fashion.

The specifications defined in this section are thus far only component specs. It is necessary to examine the importance of each specification relative to the actual application and determine the possible tradeoffs.

2. TECHNOLOGICAL CONSIDERATIONS IN OPERATIONAL AMPLIFIERS

TECHNOLOGICAL CONSIDERATIONS IN OP AMPS

- Modules
- Hybrids
- Integrated Circuits

It is useful for the design engineer to know not only the types of products available, but also the technologies used to produce them. He can thus select an amplifier for a particular application from a particular category of amplifiers and have some familiarity with the probable idiosyncrasies of that amplifier.

COMPARISON OF TECHNOLOGIES USED IN OP AMP CONSTRUCTION

	ADVANTAGES	DISADVANTAGES
Discrete (Module)	• Highest Performance Widest Bandwidth Low V_{OS}, V_{OS} Drift Low I_B High Voltage • Can Use Any Component • Can be Trimmed by Component Selection • Easily Customized • Isolation Possible	• High Price • Physical Size
Hybrid	• Performance Nearly Equal to Modules • Can Use IC Op Amp as Building Block • Discrete Components can be Used Inside Package • Small Size	• Moderate-to-High Price
Monolithic	• Low Cost • Small Physical Size • Many "Standard" Types (Many Sources) • Wide Range of Specs Available	• Limited Performance Lower Bandwidth Higher I_B Higher V_{OS}, V_{OS} Drift Limited Supply Voltages

Modules

Several technologies are currently used to produce operational amplifiers. The highest performance amplifiers are those constructed in modular form from discrete components. The use of discretes permits selection of specialized components such as high voltage output stage transistors, ultra-low leakage FETs, and very high values of resistance. It is possible, in modular designs, to select resistors and capacitors at electrical test (prior to encapsulation) to "fine-tune" dc parameters (such as offset voltage) or ac parameters (such as settling time).

The disadvantages of modular technology are physical size and price. Since each module is individually constructed, large volume manufacturing is impractical and the manufacturing cost is relatively high. Still, for special applications requiring the highest possible level of performance, modular op amps offer an attractive alternative to "home-brew" designs since their specifications are guaranteed by the manufacturer. Examples of modular op amps include chopper-stabilized, varactor-bridge, electrometer and extremely wide bandwidth types.

TYPES OF MODULAR OP AMPS

- Chopper-Stabilized
- Varactor-Bridge Electrometers
- High Speed Amplifiers

Chopper-Stabilized Amplifiers

Chopper amps are used when it is necessary to amplify (or otherwise) extremely low level voltage signals. The chopper amplifier is internally ac-coupled—the actual differential input is chopped into a square wave which is demodulated and amplified. The ac coupling removes many of the dc errors associated with op amps, resulting in extremely low offset and drift.

CHOPPER AMPLIFIER FEATURES

Low Offset Voltage:	10μV
Low Offset Drift:	0.1μV/°C
Long Term Stability:	1μV/Year
High Open-Loop Gain:	10^7 V/V
Low Warm-Up Drift:	3μV

Electrometer Amplifiers

Varactor-bridge electrometer amplifiers are used when the highest possible input impedance and lowest bias currents are required. These amplifiers are also ac-coupled internally. The input signal is applied to a bridge containing low-leakage varactor diodes (voltage-variable capacitors) and excited by a high-frequency carrier signal. The input voltage unbalances the bridge and the resultant ac error signal is ac coupled to following stages where it is synchronously demodulated and amplified. The use of low leakage varactors produces input currents as low as 10 femtoAmperes (1 femtoAmp = 10^{-15} Amp). This low current is obtained at the expense of high offset voltage.

VARACTOR – BRIDGE ELECTROMETERS

Low Bias Current: 10fA (10^{-14} A)
Inverting Models
- Current-to-Voltage Conversion
- Gas Chromatographs
- Photomultipliers

Noninverting Models
- Follower-with-Gain
- pH Cells
- Electrolytic Chemical Process Monitoring

High Speed Amplifiers

High speed amplifiers can be readily built in modular form. Many of the limitations of IC construction do not apply here. For example, an IC amplifier may have speed limitations caused by shortcomings in the transistors produced by the manufacturer's fabrication process. A modular design, however, can use selected transistors with the required frequency response. Also, since many wideband amplifiers are used in video applications driving 75 ohm loads, high output current is necessary. The power required for such output characteristics is much more easily dissipated by the larger thermal mass of a module.

ULTRA FAST AMPLIFIERS

Fast Settling:	100ns to 0.1%
Slew Rate:	1000V/μs
Full Power Bandwidth:	10MHz
Output Current:	10mA

HYBRID AMPLIFIERS

HYBRID OP AMPS

Precision Low Bias Current FET-Input Types
Wide Bandwidth, Fast Settling Types

Many of the same benefits of modular constructions also apply to hybrid amplifier. As is the case with modules, is possible to combine components manufactured with different (and incompatible) technologies in a single package. The advantage of hybrid construction over modular construction are smaller physical size and lower cost. Hybrid technology is generally applied to op amps to provide improvements in input bias current, output drive capability, or bandwidth over monolithic or discrete designs.

HYBRID FET-INPUT OP AMPS

Low Bias Current:	to 75fA
Low Offset Voltage:	to 0.25mV
Low Noise:	to 3μV p-p, 35nV/$\sqrt{Hz}$
Low Drift:	to 3μV/°C
Moderate Cost:	$5 to $10 Range

Until recently, most FET-input amplifiers consisted of a precision matched FET differential amplifier followed by a monolithic op amp. While it is now possible to manufacture junction FETs with a bipolar-compatible process, the highest precision FET-input op amps are still made with hybrid technology. While it is possible to purchase a pair of discrete low-leakage FETs and follow this stage with a 741 op amp, better performance can usually be obtained from a hybrid unit. The hybrid, for example, has specifications which are guaranteed and tested by the manufacturer. Any required trims are usually also performed by the manufacturer. And, of course, a packaged hybrid amplifier takes up no more space than a 741, yet offers orders of magnitude increases in performance.

WIDEBAND HYBRID AMPLIFIERS

- Can Duplicate Modular Designs in Smaller Packages Using Discrete Transistors in Chip Form
- Suitable for Video Applications

Hybrid technology also allows an amplifier to be constructed from a collection of discrete high-frequency transistors. In fact, it is possible to duplicate a modular amplifier circuit in hybrid form using the same components as the module, but in unpackaged chip form. The Computer Labs Division of Analog Devices produces a variety of wideband hybrid amplifiers suitable for video applications.

MONOLITHIC IC OP AMPS

MONOLITHIC IC PROCESSES

Standard Bipolar

Advantages	Disadvantages
• Many Suppliers	• High I_B
• Low Noise	• Lateral PNP Limits Bandwidth
• Low V_{OS}, V_{OS} Drift	

Dielectric Isolated Bipolar

Advantages	Disadvantages
• Allows Wide Bandwidth PNP	• Limited Number of Suppliers
• Otherwise Similar to Standard Bipolar	• More Expensive
	• ESD-Sensitive

BIFET

Advantages	Disadvantages
• Allows High Breakdown JFET to be Fabricated on Bipolar IC	• Additional Process Step
	• Higher V_{OS}, V_{OS} Drift
• High Input Impedance	• Poorer CMRR
• Low I_B	• I_B Doubles Every 10°C Rise in Temperature

BI-MOS

Advantages	Disadvantages
• Uses MOSFET for Potentially Very High Input Impedance	• Protection Diode Leakage Defeats Low MOS I_B
• Inputs can Swing to Supply Rail	• High Noise

CMOS

Advantages	Disadvantages
• Low Power	• High Noise
• Logic Circuitry and Switches can be Added	• Limited Output Drive Capability
• Allows Fabrication of Monolithic Chopper-Stabilized Amplifier	• Limited Supply Voltage Range

By far the most widely used op amps are the monolithic IC types. A large variety of IC op amps is available from many different vendors. Over the years, improvements in both design and processing have contributed to the evolution of very high performance op amps. It is useful for the op amp user to at least be aware of the various technologies employed in IC op amp fabrication, since the op amp specifications required for a particular application will often dictate the best op amp technology to choose.

Standard Bipolar Process

The standard junction-isolated bipolar process used in the majority of op amps produces three basic transistors: a high quality vertical NPN transistor, a high quality vertical PNP transistor, and a somewhat lower quality lateral PNP transistor. The vertical PNP is of limited utility since its collector is always connected to the negative power supply. Thus the two transistors which can be used elsewhere in the amplifier circuit are the vertical NPN and the lateral PNP. The lateral PNP is very low performance (low β, low f_t) and is used primarily in biasing circuitry. It is the NPN, therefore, which is used in the actual signal path as much as possible. An amplifier which uses standard bipolar transistors has bias currents generally in the 100nA to 1μA range, reasonably low offset voltage and drift, and low noise. Example of these amplifiers include the 741 and 301 types.

Super-Beta

Super-Beta processing is an addition to the standard bipolar process. With one additional diffusion step, an NPN transistor and β of several thousand can be produced, reducing input bias current by an order of magnitude down to 10nA or less. The increased gain of the input stage improves open loop gain and common mode rejection, which are two of the more important specifications of precision amplifiers. Typical open loop gain of a super-beta op amp is several million, common-mode rejection over 100dB, and input offset voltage characteristics similar or superior to standard bipolar types. Examples of super-beta amplifiers include the 308, AD510 and AD517 types.

Dielectric-Isolated (DI) Bipolar

In conventional bipolar and super beta ICs, the individual transistors are isolated from each other by the use of reverse-biased p-n junctions. It is the parasitic capacitance of these junctions which limits the bandwidth of the lateral PNP transistors (and ultimately, the amplifier). The dielectric isolation (DI) process uses a thin oxide layer to provide the isolation between transistors. It then becomes possible to fabricate a high speed PNP transistor and therefore, a high speed amplifier.

The DI process is not without its limitations, however. The oxide layer is easily punctured by electrostatic discharge, resulting in device destruction. Another drawback is the fact that DI circuits require larger geometries than junction-isolated equivalent circuits, resulting in somewhat larger chip sizes.

BIFET

The BIFET process uses ion-implantation to produce a JFET with high breakdown voltage on a chip also containing standard bipolar devices. A pair of these JFETs can be used as input devices for an op amp, the added performance is gained at the expense of generally poorer offset voltage, drift, CMR, and noise specifications. Newer designs allow for factory trimming of BIFET op amp offset voltage and drift. Examplfes of precision BIFET type amplifiers include the AD542, AD544, AD547 and the dual AD642, AD644 and AD647.

BI-MOS

Since JFETs can be used for high-impedance input stages, it is tempting to consider MOSFETs for the same application. Some manufacturers have developed processes which permit MOSFETs to be included on a bipolar IC. Rather than junction leakages inherent in JFETs, MOSFETs ideally have only oxide leakages, which are much lower, potentially reducing input bias current. MOSFETs, however, are ESD sensitive and require protection diodes on the inputs. Very often, these diodes exhibit leakages which are at least as high as the input bias current of a JFET-input amplifier. MOSFETs further tend to be much noiser than JFETS in the audio frequency spectrum, and dc offsets are difficult to control. When MOSFETs are used in the output stage of an op amp, it becomes possible to swing the output very close to the power supply rails. In a conventional bipolar output stage, output swing is limited by saturation voltages and other effects. It is important to note, however, that a MOSFET output stage must be lightly loaded to minimize the effects of R_{ON}.

CMOS

Amplifiers constructed entirely of MOSFETs are also available. These amplifiers exhibit poor performance if built along classical op amp designs. Newer designs use CMOS switches and external capacitors to provide offset voltage cancellation similar to the methods used in chopper-stabilized amplifiers. These designs suffer from high noise, poor output drive characteristics, and limited supply voltage ranges.

Laser-Trimming

Laser trimming technology can be applied to any of the aforementioned amplifier types if thin-film resistors have been included on the chip. By trimming one resistor of a pair, it is possible to adjust the operating conditions in a differential input stage so as to reduce the offset voltage. This technique allows routine production of bipolar input amplifiers with guaranteed offset voltages as low as 25μV and high performance BIFET amplifiers with guaranteed offsets of 250μV. Amplifiers with trimmed offsets allow precision circuits to be produced without the need for external offset adjustments. External trims are often subject to potentiometer instability, mechanical shock effects, and accidental misadjustments.

"Zener-Zap" Trimming

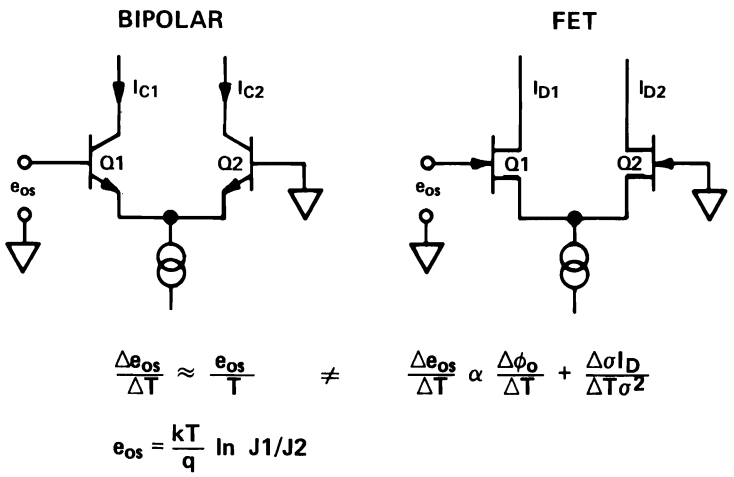
An alternate method of offset voltage trimming is called Zener-Zap trimming. In laser-trimming the emitter currents are varied in a bipolar differential stage by trimming resistances. In Zener-Zapping, a series of current sources (similar to a DAC) is digitally adjusted to provide the current balance which

produces the lowest offset voltage. When the correct combination of current sources is determined by the probing equipment, a high voltage pulse is applied to the desired current sources, permanently programming them.

The only disadvantage of Zener-Zapping is that the programmable current source requires a larger amount of chip area than a pair of thin-film resistors. It is thus not well suited for data converter linearity trimming. It has the advantage of not requiring the thin film deposition process step. The AD OP-07 is an example of a Zener-Zap trimmed op amp.

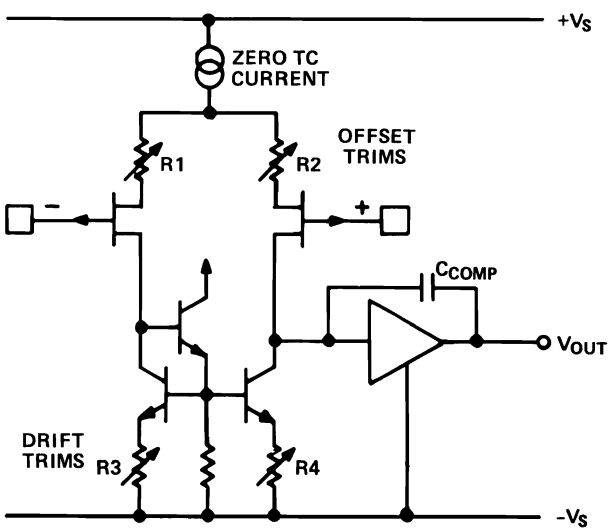
DRIFT TRIMMING

Bipolar input amplifiers have the property that the offset voltage drift is at a minimum when the offset voltage is zero. Thus a laser- or zener-zap trimmed bipolar op amp will inherently have low drift. BIFET op amps, however, have no such correlation between offset voltage and offset drift. As a result, many BIFET op amps feature drifts as high as $20\mu V/^{\circ}C$ or more, even if the initial offset has been trimmed to zero.



BIPOLAR VS FET OFFSET DRIFT

Drift trimming makes use of the fact that two terms influence the offset and only one affects the drift. By using a heated prober, it is possible to test an amplifier for offset voltage at 70°C, store that value in memory, then cool the wafer to 25°C and determine the drift. The current mirror stage can be trimmed to the correct value to null the drift, and one last trim can be performed to reduce the 25°C offset voltage without disturbing the drift. The AD547 and AD647 are examples of drift trimmed BIFET op amps. A simplified schematic of the input stage of these amplifiers appear below.



LOW DRIFT FET AMPLIFIER

SELECTING THE RIGHT AMPLIFIER FOR THE APPLICATION

1. Consider the Source
2. Analyze Effects of Various Op Amp Specs in the Application
3. Determine Environmental Variations
4. Don't Spend More (or Less) than Necessary

The actual application will often dictate whether a particular amplifier can be used. The process of selecting the "best" amplifier for an application involves a rigorous analysis of error sources—both in the amplifier and in the external components. It is important to analyze the characteristics of the input signal, the desired accuracy, and environmental conditions to which the circuit will be subjected. In this section, we will consider a series of applications and outline the amplifier selection process.

"WHAT DO YOU DO WHEN A 741* WON'T DO?"

A. Impossible – 741s Can Do Anything
B. Use A 741 Anyway and Hope Nobody Notices
C. Use A Dual 741 (Two Amps are Better than One)
D. Give Up and Take Up Computer Programming
E. Select an Amplifier with Specs Which Match the Application

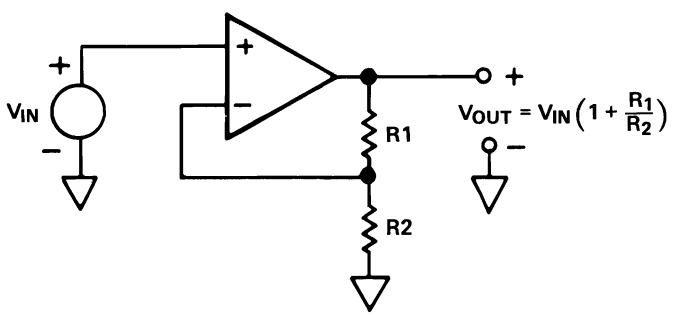
*Or 301A, 308A, 356A, or Whatever General-Purpose Op Amp You Use "Everywhere".

PREAMPLIFIER APPLICATIONS

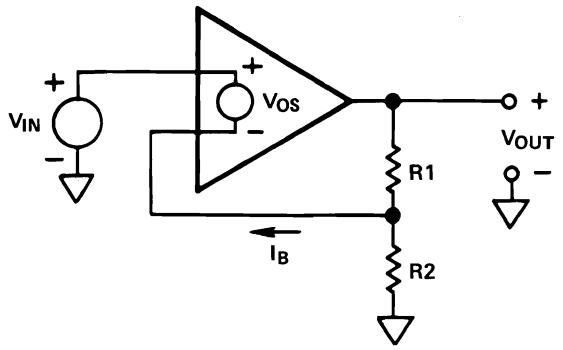
While operational amplifiers were originally intended for use inside analog computational circuits, where feedback networks allowed them to perform analog operations such as integration and differentiation, op amps have become widely used as low-cost gain stages. The choice of op amp in such applications is dependent upon the characteristics of the signal source, the gain stage and the desired accuracy.

Consider a preamplifier for a low level signal. Assuming a noninverting gain stage is built with an ideal op amp and ideal resistors, the output will then be equal to the input times one plus the resistor ratio.

Any input offset voltage in the op amp will appear as a voltage source in series with the signal, and will be amplified along with the signal. Any dc bias current will flow into the amplifier input through the equivalent resistance seen "looking back" from its input.

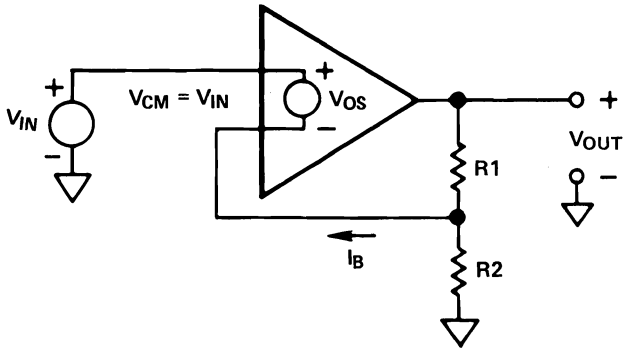


IDEAL NON-INVERTING GAIN STAGE



$$V_{OUT} = \left[V_{IN}\left(1 + \frac{R_1}{R_2}\right) + V_{OS}\left(1 + \frac{R_1}{R_2}\right) + I_B R_1 \right] = \left(1 + \frac{R_1}{R_2}\right)\left[V_{IN} + V_{OS} + I_B\left(\frac{R_1 R_2}{R_1 + R_2}\right)\right]$$

NON-INVERTING AMPLIFIER FIRST-ORDER ERRORS



$$V_{OUT} = \left[V_{IN}\left(1 + \frac{R_1}{R_2}\right) + V_{OS}\left(1 + \frac{R_1}{R_2}\right) + I_B R_1 + \left(\frac{V_{IN}}{CMRR}\right)\ 1 + \frac{R_1}{R_2} \right]$$

$$= \left(1 + \frac{R_1}{R_2}\right)\left[V_{IN} + V_{OS} + I_B\left(\frac{R_1 R_2}{R_1 + R_2}\right) + \left(\frac{V_{IN}}{CMRR}\right)\right]$$

NON-INVERTING AMPLIFIER SECOND-ORDER ERRORS

This generates an additional offset voltage (which is also amplified as if it were a signal). Interestingly, since the voltage produced by the bias current is equal to

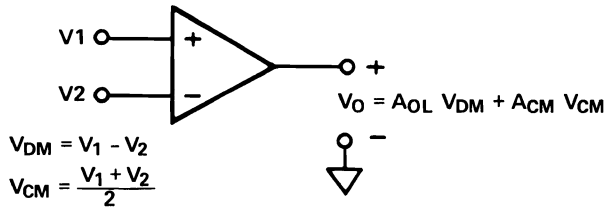
$$I_B \times \frac{R_1 R_2}{R_1 + R_2}$$

and the gain applied to this voltage is

$$\frac{R_1 + R_2}{R_2}$$

the net effect at the output is a term equal to $I_B \times R_1$.

An additional error arises in a noninverting amplifier due to common-mode effects. Although an ideal op amp is insensitive to common-mode inputs, real amplifiers do respond to common mode inputs. This error term can be modeled as an additional offset voltage equal to the common-mode voltage divided by CMRR. As an offset voltage, it is amplified by the same gain as the signal.



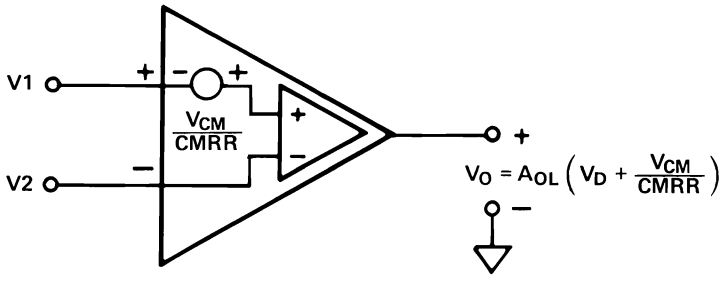
EFFECT OF COMMON MODE VOLTAGE

$$V_O = A_{OL}\, V_{DM} + A_{CM}\, V_{CM}$$

$$\text{Since CMRR} = \frac{A_{OL}}{A_{CM}}$$

$$V_O = A_{OL}\, V_{DM} + \frac{A_{OL}}{CMRR}\, V_{CM}$$

$$= A_{OL}\left(V_{DM} + \frac{V_{CM}}{CMRR}\right)$$

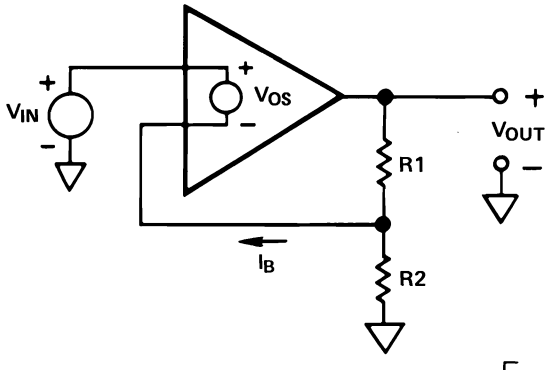


EQUIVALENT OFFSET VOLTAGE INDUCED BY COMMON MODE

Finite open loop gain adds yet another error. It can be shown that the actual gain of the circuit will be equal to the desired gain multiplied by

$$1 + \frac{1}{A_{OL}\,\beta}$$

where A_{OL} is the amplifier's open-loop gain and β is the voltage feedback ratio.

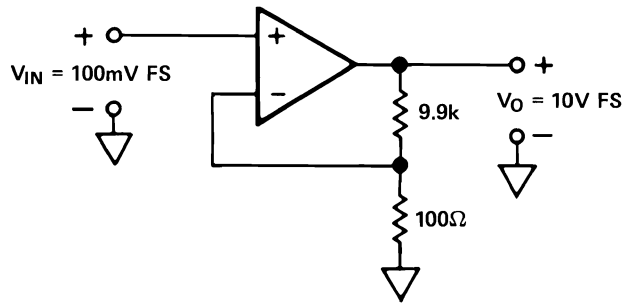


$$V_{OUT} = \left(\frac{R_1 + R_2}{R_1}\right)\left[V_{IN} + V_{OS} + I_B\left(\frac{R_1 R_2}{R_1 + R_2}\right) + \frac{V_{CM}}{CMRR}\right]\left[\frac{A_{OL}\,\frac{R_2}{R_1 + R_2}}{1 + A_{OL}\,\frac{R_2}{R_1 + R_2}}\right]$$

GAIN ERROR INTRODUCED BY FINITE A_{OL}

In order to appreciate the relative magnitudes of these errors, a numerical example is in order. Assume the circuit below is designed as a preamplifier to raise a 100 millivolt signal to 10 volts, and ideal resistors are available. It remains to choose the op amp. Compare an AD OP-07 with a standard 741 op amp for use in this application.

	AD741CH	ADOP-07CH
V_{OS}, Max	6mV	150μV
I_B, Max	500nA	7nA
CMR, Min	70dB	100dB
A_{OL}, Min	20,000V/V	1,200,000V/V



$$V_{OUT}\Big|_{741C} = (100)\left[0.1 - 0.006 - (500nA \times 100\Omega) - \frac{0.1}{3500}\right]\left[\frac{(20000)\left(\frac{1}{100}\right)}{1 + (20000)\left(\frac{1}{100}\right)}\right]$$

$$= 9.3922\left[\frac{200}{201}\right] V \quad (6.08\% \text{ ERROR})$$

$$= 9.3455V \ (6.54\% \text{ ERROR})$$

$$V_{OUT}\Big|_{OP\text{-}07C} = (100)\left[0.1 - 0.00015 - (7nA \times 100\Omega) - \frac{0.1}{100000}\right]\left[\frac{1.2 \times 10^6 \times \frac{1}{100}}{1 + (1.2 \times 10^6)\frac{1}{100}}\right]$$

$$= 9.98493\left[\frac{12000}{12001}\right] V \quad (0.15\% \text{ ERROR})$$

$$= 9.98409V \ (0.159\% \text{ ERROR})$$

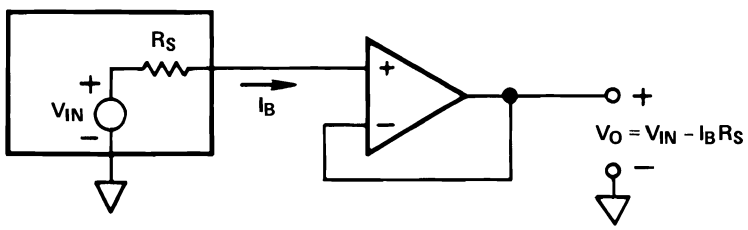
COMPARISON OF 741C AND OP-07C PERFORMANCE

Of course the largest error is due to offset voltage. It may appear that since this error can be reduced or eliminated by trimming, it can be neglected. However, temperature-induced offset drifts are not so easily corrected. It is also possible to reduce errors induced by bias current by matching the impedances seen at each input of the op amp. The resultant error term is now I_{OS} times the source resistance. However, CMRR-and-A_{OL}-induced errors can not be compensated because they are not constants. CMRR is often a nonlinear function of common-mode voltage. Input noise can also not be reduced, although noise has been ignored thus far in the discussion.

Noninverting gain stages are often used to buffer high impedance sources. In these applications, it is possible that bias current will be the primary error source. Consider the case of a pH or other ion-selective electrode, where the desired signal voltage is a few hundred millivolts but the source impedance can exceed 100 megohms ($10^8\Omega$).

In these applications, a hybrid FET-input op amp is the only practical choice. For example, if the amplifier is connected as a simple follower, the actual signal being amplified is

$$V_{IN}' = V_{IN} - I_B R_S$$



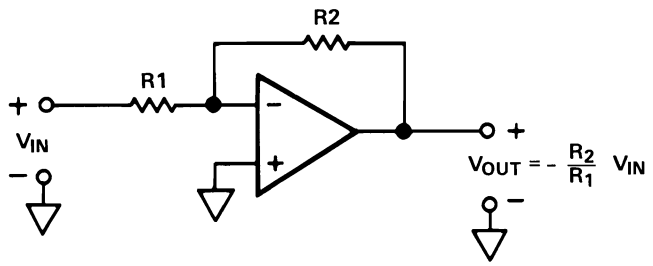
OP AMP	I_B	ERROR FOR R_S = 10MΩ
IDEAL	0	0
AD741	500nA	5V
AD OP-07	7nA	70mV
AD542	25pA	0.25mV
AD515	75fA	750nV

EFFECT OF BIAS CURRENT IN BUFFER AMPLIFIER

If a 741 op amp is used as the buffer amplifier for a 10MΩ source, an error of 500nA × 10MΩ = 5 volts will result. If a 50pA I_B BIFET amplifier is used, the error is reduced to 500μV. With a hybrid FET input op amp with 1pA bias current, a 10MΩ source can be buffered with only 10μV of additional error. Amplifiers such as the 1pA AD545 and 0.075pA AD515 are well suited to such applications.

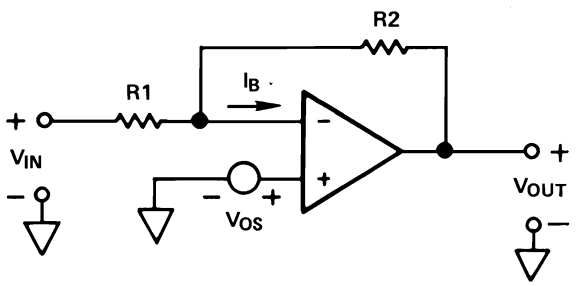
THE INVERTING AMPLIFIER

So far this discussion has been limited to noninverting amplifiers. Many circuits require a negative gain and op amps are easily used. The normal inverting amplifier operates by holding the noninverting input at zero volts, which causes the amplifier's output to drive the inverting input also to zero volts. If this node is at virtual ground, it is easy to prove that the current from the source is equal to V_{IN}/R_1 and the current from the output is V_{OUT}/R_2. Since these currents are equal and opposite (with an ideal op amp), the gain is simply $-R_2/R_1$.



IDEAL INVERTING AMPLIFIER

The error analysis is slightly different than for the case of the noninverting amplifier. Errors due to offset are actually amplified by a greater gain than is the actual signal. Since the input offset voltage can be



$$V_{OUT} = (V_{IN})\left(-\frac{R_2}{R_1}\right) + (V_{OS})\left(1 + \frac{R_2}{R_1}\right) + (I_B)\left(\frac{R_1 R_2}{R_1 + R_2}\right)\left(\frac{R_1 + R_2}{R_1}\right)$$

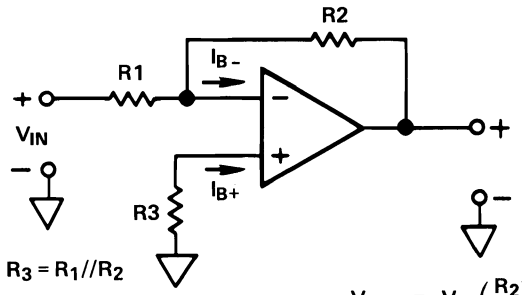
INVERTING AMPLIFIER WITH FIRST-ORDER ERRORS

modeled as a voltage source in series with one of the inputs, it is clear that the gain to this voltage is actually $(1 + R_2/R_1)$. For circuits where the desired signal gain is low (including gains less than unity), this increased offset gain can be troublesome.

NOTE THAT IN AN INVERTING AMPLIFIER:

1. **$V_{CM} \approx 0$ so CMRR is Not as Important as it is in a Noninverting Amplifier.**
2. **"Noise Gain" is Equal to Signal Gain Plus 1. Offset Voltage will be Amplified More than the Signal.**

Input bias current is another source of error. The bias current flows through a resistance equal to R_1 in parallel with R_2, creating an offset voltage which is amplified by a gain of $(1 + R_2/R_1)$, or a net output error of $I_b R_2$. It is common practice to add a resistance R_3 (equal to R_1/R_2) in series with the noninverting input, so that the I_b R terms generate a small common mode voltage which is rejected, and an offset voltage of I_{OS} R is the only error. Note that the application circuit must be capable of tolerating the common mode signal; furthermore, it is worth noting that I_{OS} must be significantly smaller than I_b for this technique to offer significant performance improvement. Since the ideal inverting amplifier operates at zero common mode voltage, common mode errors are zero.



$$V_{OUT} = -V_{IN}\left(\frac{R_2}{R_1}\right) + \left[(I_{B-}\,R_2) - (I_{B+}\,R_3)\left(\frac{R_1+R_2}{R_1}\right)\right]$$

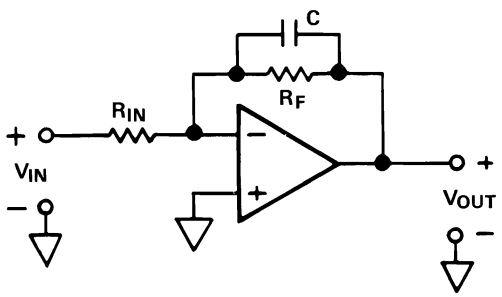
$$= -V_{IN}\left(\frac{R_2}{R_1}\right) + \left[(I_{B-}\,R_2) - \left(I_{B+}\,\frac{R_1\,R_2}{R_1+R_2}\right)\left(\frac{R_1+R_2}{R_1}\right)\right]$$

$$= -V_{IN}\left(\frac{R_2}{R_1}\right) + \left[(I_{B-} - I_{B+})\,R_2\right]$$

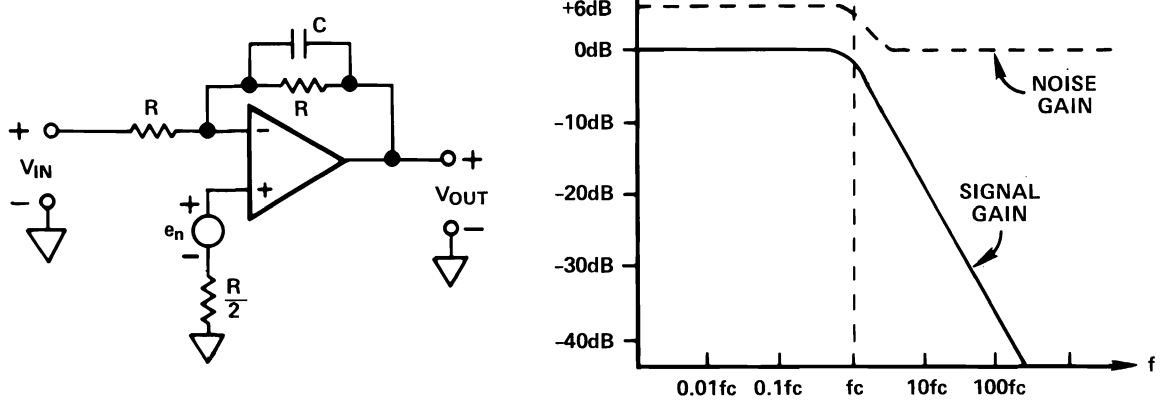
$$= -V_{IN}\left(\frac{R_2}{R_1}\right) + I_{OS}\,R_2$$

USE OF BIAS CURRENT CANCELLATION RESISTOR

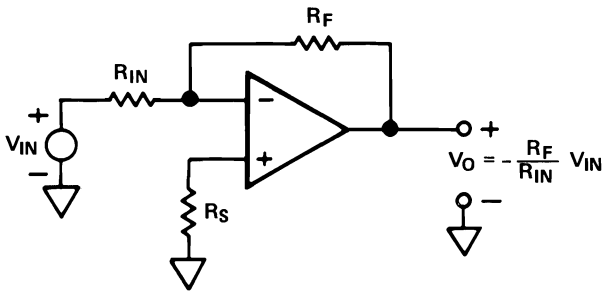
The useful dynamic range of any preamplifier is limited by the random noise generated within the circuit. When analyzing the contribution of noise to the output of an amplifier, it is important to consider the gain applied to the noise signal as a function of frequency. In the case of a unity gain inverting amplifier with an integrating capacitor as shown below, some problems arise from the difference in noise and signal gains.



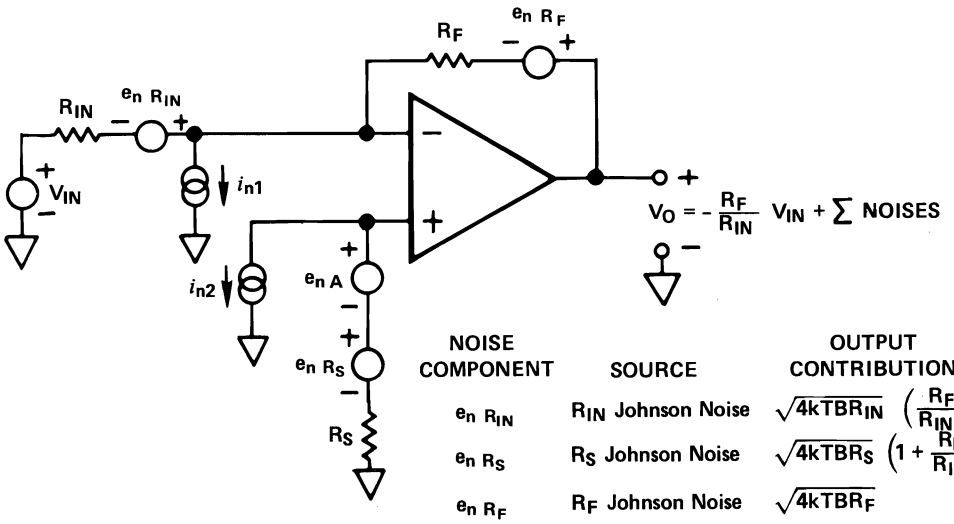
INVERTING AMPLIFIER
WITH INTEGRATING CAPACITOR



FREQUENCY RESPONSE OF UNITY-GAIN INVERTING AMPLIFIER



NOISELESS INVERTING AMPLIFIER



NOISE COMPONENT	SOURCE	OUTPUT CONTRIBUTION
$e_{n\,R_{IN}}$	R_{IN} Johnson Noise	$\sqrt{4kTBR_{IN}}\left(\frac{R_F}{R_{IN}}\right)$
$e_{n\,R_S}$	R_S Johnson Noise	$\sqrt{4kTBR_S}\left(1+\frac{R_F}{R_{IN}}\right)$
$e_{n\,R_F}$	R_F Johnson Noise	$\sqrt{4kTBR_F}$
$e_{n\,A}$	Amp V Noise	$e_n\left(1+\frac{R_F}{R_{IN}}\right)$
i_{n1}	Amp I Noise	$i_{n1}\,R_F$
i_{n2}	Amp I Noise	$i_{n2}\,R_S\left(1+\frac{R_F}{R_{IN}}\right)$

NOISE IN INVERTING AMPLIFIER

CHOOSING AN AMPLIFIER FOR LOW NOISE

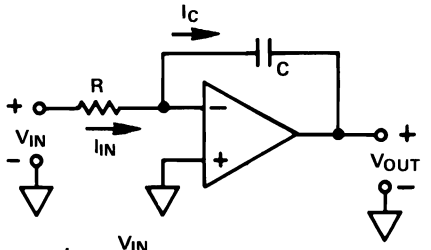
1. Examine Circuit Impedances.
2. Determine Noise Voltage Gain.
3. Trade Off Between Low Current Noise and Low Voltage Noise.
4. Note that the Desired Noise Performance May Be Physically Impossible if Impedances are too High.

FILTER APPLICATIONS

Operational amplifiers are often used in filter applications. While it is beyond the intended scope of this text to provide an in-depth study of active filters (since abundant literature already exists) some important details will be explored.

Integrators (Low Pass Filters)

The ideal integrator uses an op amp with a capacitive feedback path, and provides an output proportional to the integral of the input signal. Since the op amp will maintain both inputs at zero volts, the input current, I_{IN}, is equal to V_{IN}/R. Ideally, none of this current flows into the op amp input but charges the capacitor.



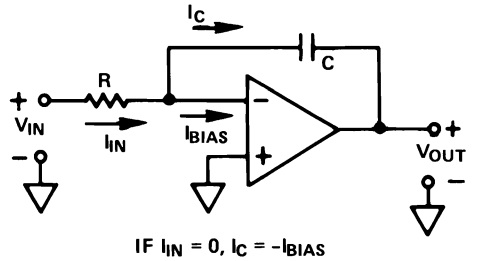
$$I_{IN} = \frac{V_{IN}}{R}$$

$$I_C = -C \frac{d\,V_{OUT}}{dt}$$

$$I_{IN} = I_C \therefore V_{OUT} = -\frac{1}{RC} \int V_{IN}\, dt$$

IDEAL INTEGRATOR/LOW-PASS FILTER

When this circuit is built with a real op amp, however, some current does flow into the input. This bias current will serve to charge the capacitor, delivering an output voltage even in the absence of an input signal. This output voltage will appear as a dc output drift with respect to time, and is equal to $(-I_B/C)$ volts per second. As an example of the relative magnitude of this drift, consider an amplifier with 100nA of bias current used in an integrator with a 1000pF integrating capacitor. The time drift due to bias current charging is 100 volts per second.



IF $I_{IN} = 0$, $I_C = -I_{BIAS}$

$$\frac{d\,V_{OUT}}{dt} = -\frac{I_{BIAS}}{C}$$

$$\frac{d\,V_{OUT}}{dt} = \frac{I_{BIAS}}{C}\,\frac{V}{SEC}$$

FOR C = 1000pF AND I_{BIAS} = 100nA

$$\frac{d\,V_{OUT}}{dt} = 100\,\frac{V}{SEC}\ !$$

INTEGRATOR WITH BIAS CURRENT

This means that the amplifier will saturate shortly after power is applied and the integrator function is lost.

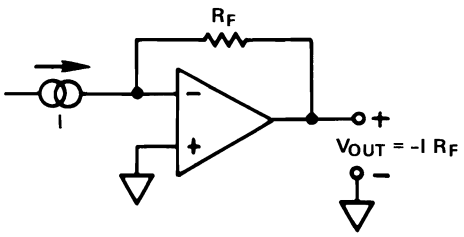
While this is a simple case, it does illustrate the fact that often-ignored dc parameters of op amps such as input bias currents can have a significant impact on active filter circuit performance. In general, a good routine for selecting an op amp for a filter application is to first assume the op amp is ideal and select appropriate pole and zero locations for the desired response characteristics. Once the capacitor and resistor values have been chosen, determine any adverse effects due to bias current and analyze the dc gain of the circuit to determine the effect of offset voltage. Keep in mind that even in ac-coupled stages, large dc offset gains can cause the stage to have a large dc output offset, resulting in clipping or saturation.

CURRENT-TO-VOLTAGE CONVERTERS

While some transducers deliver an output voltage proportional to some physical parameter, many transducers produce a current output. Such transducers include photodiodes, some temperature sensors, and a variety of biological probes. Very often, the currents produced are very small—on the order of nanoamps or less. Generally, signal conditioning of some type will be needed before such a signal is at all useful or accurately measurable.

While a resistor is a genuine current-to-voltage converter, it is generally not practical to force the current directly through a resistor and then attempt to measure it differentially. Furthermore, most current sources have a limited range of compliance voltage.

A more useful technique for conditioning a current signal uses an op amp and large feedback resistor. The input current source drives a constant terminal voltage (zero volts), and the current flow through the resistor to the op amp output. The output voltage is then equal to the input current times the feedback resistor.



CURRENT-TO-VOLTAGE CONVERTER

Clearly, amplifier input bias current will cause an error. Thus, FET-input amplifiers are most often used in current-to-voltage converter applications since they exhibit the lowest bias current (at room temperature). The best performance is available from hybrid FET-input op amps since they can feature lower bias currents than presently manufacturable monolithic types. Examples of such amplifiers include the AD515 and AD545.

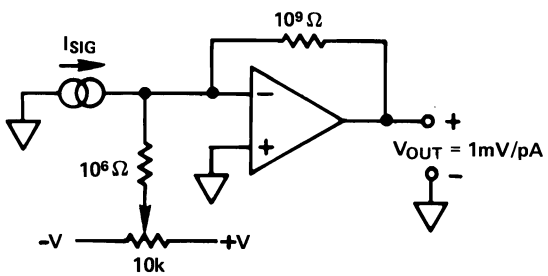
AD515 FEATURES

Ultra Low Bias Current: 0.075pA max (AD515L)
0.150pA max (AD515K)
0.300pA max (AD515J)
Low Power: 1.5mA max Quiescent Current (0.8mA typ)
Low Offset Voltage: 1.0mV max (AD515 K & L)
Low Drift: 15μV/°C max (AD515K)
Low Noise: 4μV p-p, 0.1 to 10Hz
Low Cost

AD545 FEATURES

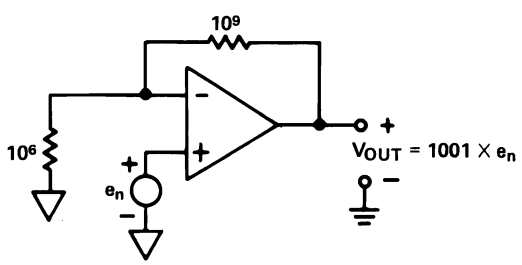
Low Offset Voltage: 0.5mV max (AD545L), 0.25mV max (AD545M)
Low Offset Voltage Drift: 5μV/°C max (AD545L), 3μV/°C max (AD545M)
Low Power: 1.5mA max
Low Bias Current: 1pA max (AD545K, L, M)
Low Noise: 3μV p-p, 0.1 to 10Hz
Low Cost

Some special considerations apply in the use of op amps in I/V converters. Very often, it is desirable to null out circuit offsets, either amplifier-generated or system generated (dark current, for example). At first glance, it would appear that the circuit shown below would suffice to generate a small leak current. However, this circuit will be found to produce very high drift and noise.



NULLING OFFSETS IN CURRENT-TO-VOLTAGE CONVERTER (WRONG WAY)

A closer look at the circuit shows a noise voltage gain of 1001, accounting for the large noise output and dc drift.



EQUIVALENT CIRCUIT FOR NULLED I/V CONVERTER

In an earlier preamplifier design example, it was recommended that a bias current cancelling resistor be used in the noninverting input of an op amp. While this is generally desirable, it can cause problems in I/V converter circuits. The large resistor values commonly used must be considered as noise generators. In many instances, the Johnson noise generated by a large resistor will exceed op amp-generated noise. For example, an ideal $10^{10}\Omega$ resistor produces $400nV/\sqrt{Hz}$ noise, or $8\mu V$ peak-to-peak in a 10Hz bandwidth. Having two resistors on the inputs will increase noise by $\sqrt{2}$, or 41%.

4. DESIGN TECHNIQUES FOR OPERATIONAL AMPLIFIER CIRCUITS

DESIGN TECHNIQUES FOR OP AMP CIRCUITS

Passive Component Selection
Bypassing/Decoupling/Grounding
Circuit Layout
Device Protection
Common Errors

In the presentation thus far, we have concentrated on the specifications of the op amp itself. It is important to recognize that often it is the passive components or even the circuit layout which will be the ultimate limitation on system performance. This section will concentrate on design techniques which will permit the user to achieve the highest performance possible from an op amp circuit.

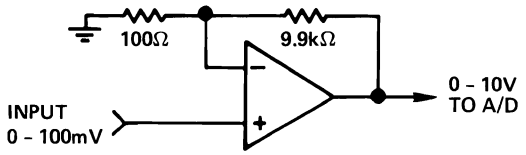
SELECTING PRECISION PASSIVE COMPONENTS

Resistors

The most basic electrical component is the resistor. The performance of a resistor in a circuit is (incompletely) described by Ohms Law, V=IR. To stop there is to invite problems. The most popular systems of today are based on 12-bit accuracy and performance; this dictates the ability to accurately define $2^{12} = 4096$ distinct levels. In order to assure unique determination of each level, each of those quantities must be accurate to ±1/2LSB. This means that errors or shifts in accuracy of as little a ±0.012% can, in some applications, degrade performance to an unacceptable level.

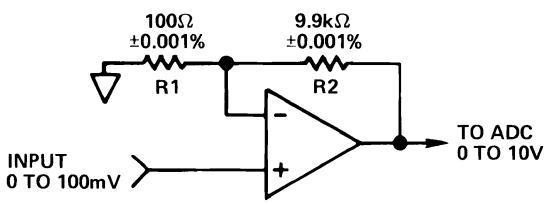
If, for example, one wishes to amplify a zero to 100mV input signal by a factor of 100 for conversion by a 12-bit A/D with a zero to 10 volt input range, the following circuit might be applied:

GAIN OF 100 STAGE



The initial tolerance of the resistors may be corrected by calibration or selection, thus the initial gain accuracy may be set to whatever tolerance is required (perhaps limited by the accuracy of the calibration instrumentation).

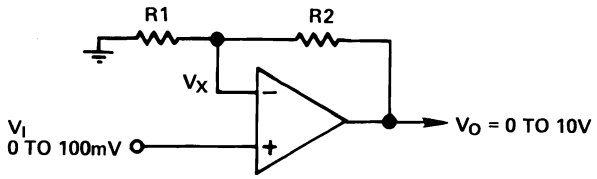
The next issue is stability over the operating temperature range. Most users will recognize that the absolute temperature coefficient of resistors is not very crucial as long as those two resistors have matching temperature coefficients. Carbon composition resistors with TCs in the order of 1500 parts per million per degree Celcius (ppm/°C) are obviously not suitable; even if the TCs could be matched to ±1% (not likely), the differential TC of 15ppm/°C would be inadequate. 1/2LSB (0.012%) corresponds to 120ppm; a temperature change of 8°C applied to these resistors would cause a gain shift as shown:



TC_1 (of R_1) = 1500ppm/°C
TC_2 (of R_2) = 1515ppm/°C
$TC_2 - TC_1 = \Delta TC$ = 15ppm/°C
(15ppm/°C)(8°C) = 120ppm
= 1/2LSB

TEMPERATURE EFFECTS X100 AMPLIFIER

It is relatively easy to buy metal film resistors that have absolute TCs between 10 and 100ppm/°C. It is also fairly routine to specify resistor pairs with TCs that track to within 2 to 10ppm/°C. Let us, for example, assume that we have purchased RN55C resistors with perfectly matched absolute TCs of 50ppm/°C. Will that solve the problem? We need more information.



$R_1 = 100\Omega, \pm 0.001\%, +50ppm/°C$
$R_2 = 9.9k\Omega, \pm 0.001\%, +50ppm/°C$
$\theta_{FA} = 125°C/W$

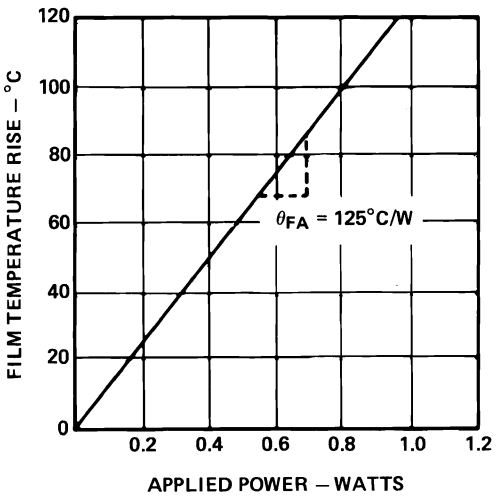
AT $V_I = 0V$, $V_O = 0V$, $V_X = 0V$
P_D IN $R_1 = P_D$ IN $R_2 = 0$
AT $V_I = 100mV$, $V_O = 10V$, $V_X = 100mV$

$$P_D \text{ IN } R_1 = \frac{(0.10)^2}{100\Omega} = 0.1mW$$

$$P_D \text{ IN } R_2 = \frac{(9.9)^2}{9.9k\Omega} = 9.9mW$$

R_1 WILL HEAT UP 0.0125°C
R_2 WILL HEAT UP 1.24°C
(1.24°C)(50ppm/°C) = 62ppm = 0.006% ERROR

TEMPERATURE-INDUCED NONLINEARITY



THERMAL RESISTANCE OF 1/4 WATT RN55-TYPE RESISTORS

This effect is not even linear: At half scale:

$V_I = 50mV$, $V_O = 5V$, $V_X = 50mV$

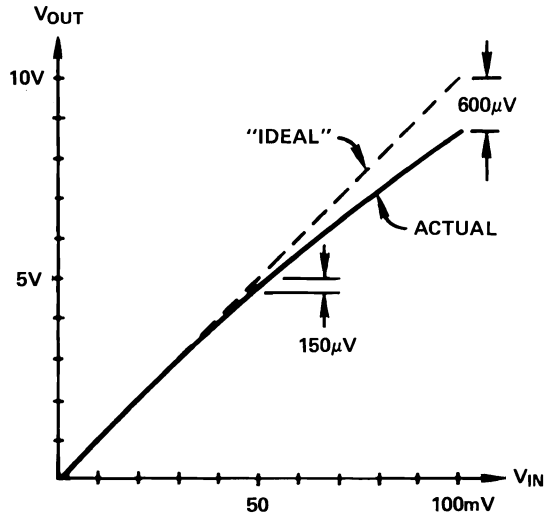
$$P_D \text{ IN } R_1 = \frac{(0.05)^2}{100\Omega} = 0.025mW$$

$$P_D \text{ IN } R_2 = \frac{(4.95)^2}{10k\Omega} = 2.48mW$$

R_1 WILL HEAT UP 0.031°C
R_2 WILL HEAT UP 0.30°C

(0.3°C)(50ppm/°C) = 15ppm

Since 3/4 of the error occurs over 1/2 of the operating range, the transfer function of such an amplifier circuit is nonlinear.



AMPLIFIER CIRCUIT TRANSFER FUNCTION

There are four major considerations in choosing resistors that solve this problem:

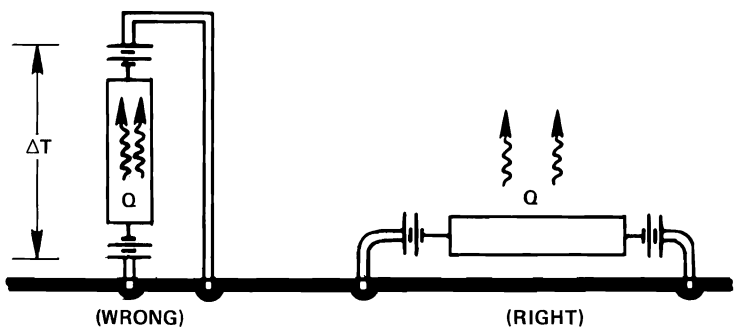
TEMPERATURE CONSIDERATIONS IN PRECISION RESISTORS

1. Closely matched temperature coefficients
2. Low absolute temperature coefficients
3. Low thermal resistance
   (Higher power rating – larger case)
4. Low voltage coefficient of resistance
5. Tight thermal coupling of matched resistors
   (One package – resistor network)

Wirewound resistors are often used in precision circuits. However, significant errors can be introduced by these resistors if they are not fully understood. Most precision wirewound resistors are available either normally or noninductively wound. The latter is preferable from the standpoint of minimal inductive reactance. These resistors still appear slightly inductive (on the order of 20 microhenries) for resistor values below 10kΩ. Resistor values above 10kΩ will actually exhibit shunt capacitance (5pF or so).

It is also necessary to consider the resistor termination, where the resistance wire is joined to the lead material. The junction of two dissimilar metals creates a thermal EMF, and this can be a problem in precision circuits.

Standard precision wire-wounds use a lead material called "Alloy 180" (77% Copper, 23% Nickel) which generates a thermal EMF of 42μV/°C when joined to the resistance wire. If the two terminations are maintained at the same temperature, no net error results. However, if the resistor is mounted vertically, it is unlikely that the top and bottom of the resistor will be at the same temperature. As the resistor dissipages power (as a result of signal voltage), heat will rise and create an error voltage.



MOUNTING TECHNIQUES FOR WIRE WOUND RESISTORS

Tinned copper leads (usually available on special order) reduce the thermal EMF to 2.5μV/°C, and may be a worthwhile option for precision circuits.

Selection of resistors employed in high impedance situations is critical. High-megohm resistors should be of the carbon film or deposited ceramic oxide to obtain the best in low noise and high stability performance. The best packaging for high-megohm resistors is a glass body sprayed with silicone varnish to minimize humidity effects. These resistors must be handled very carefully to prevent surface contamination.

A summary of the relative advantages and disadvantages of various resistors is tabulated below:

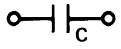
RESISTOR COMPARISON CHART

TYPE		ADVANTAGES	DISADVANTAGES
DISCRETE	Carbon Composition	Lowest Cost High Power/Small Case Size	Poor Tolerance (5%) Poor Temperature Coefficient (1500ppm/°C)
	Wire-Wound	Excellent Tolerance (0.01%) Excellent TC (1ppm/°C) High Power	Reactance May be a Problem Large Case Size Most Expensive
	Metal Film	Good Tolerance (0.1%) Good TC (<1 to 100ppm/°C) Moderate Cost	Must be Stabilized with Burn-In Low Power
	Bulk Metal or Metal Foil	Excellent to Leakage (to 0.005%) Excellent TC (to <1ppm/°C) Low Reactance	Low Power Very Expensive
	High Megohm	Very High Values (10^8 - $10^{14}\Omega$) Only Choice for Some Circuits	High Voltage Coefficient (200ppm/V) Fragile Glass Case Expensive
NETWORKS	Thick Film	Low Cost High Power Laser-Trimmable Readily Available Suitable for Hybrid IC Substrate	Fair Matching (0.1%) Poor TC (>100ppm/°C) Poor Tracking TC (10ppm/°C)
	Thin Film on Glass	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Low Capacitance	Not Suitable for Monolithic IC Construction Delicate Often Large Geometry Low Power
	Thin Film on Ceramic	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Low Capacitance Suitable for Hybrid IC Substrate	Often Large Geometry Not Suitable for Monolithic IC Construction
	Thin Film on Silicon	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Suitable for Monolithic IC Construction	Not Suitable for Hybrid IC Substrate Some Capacitance to Substrate Low Power
	Thin Film on Sapphire	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Laser-Trimmable Low Capacitance Suitable for Monolithic IC Construction	Higher Cost Low Power

Capacitors

A capacitor is another basic electrical component that can perform nonideally, thus compromising the performance of a precision circuit.

IDEAL CAPACITOR

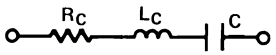


$$Z = \frac{1}{j\omega C}$$

$$Z \propto \frac{1}{C}$$

Since the most size and cost effective high-value capacitor is of the electrolytic type, it follows that such a capacitor is well suited to filtering low frequency noise:

ELECTROLYTIC CAPACITOR



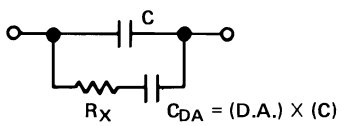
$$Z = R_C + j\omega L_C + \frac{1}{j\omega C}$$

As frequency increases, the reactive impedance of an electrolytic capacitor will decrease until the inductive reactance equals the capacitive reactance. Depending on the exact type of electrolytic capacitor used, that can occur at frequencies on the order of 1MHz. Obviously, a different type of capacitor is required for high frequency bypassing. Often recommended is an inexpensive, small, ceramic capacitor (0.01μF to 0.1μF). At 1MHz, the reactive impedance of a 0.1μF capacitor is 1.6Ω. But beware, cheap ceramic capacitors may not be all "C".

Ceramic capacitors are useful for many functions. Good NPO (negative-positive-zero TC) devices have temperature coefficients of ±30ppm/°C and are relatively inexpensive. But ceramic capacitors are not a universal cure-all; they have a dielectric absorption (D.A.) of between 0.1% and 1% or even more, depending on the composition of the ceramic dielectric used for construction.

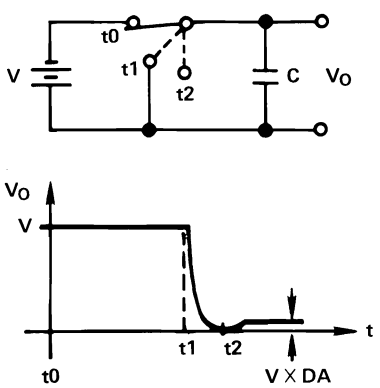
Dielectric absorption is just that; it is the charge absorbed into the dielectric that is not immediately added to or removed from the capacitor when rapidly charged or discharged. It can be modeled thus:

CAPACITOR WITH DIELECTRIC ABSORPTION

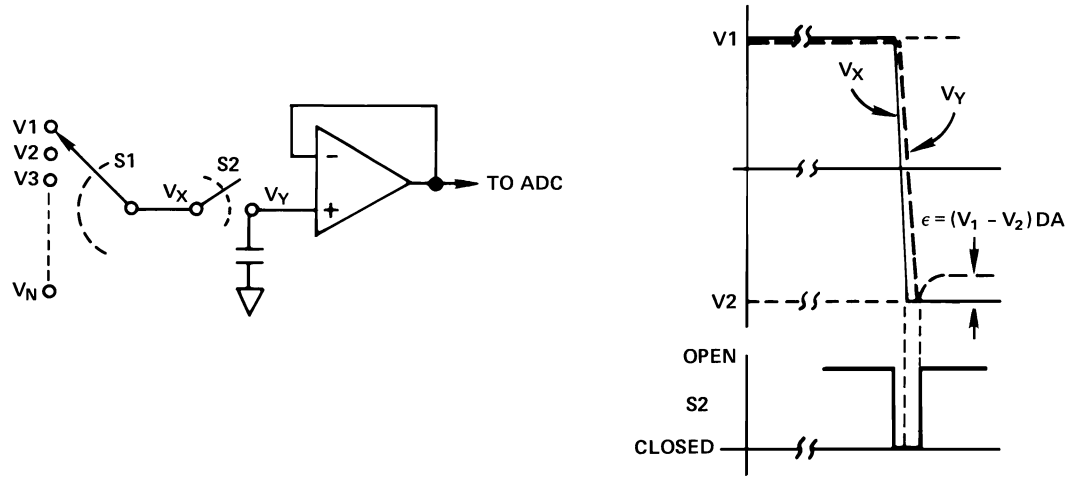


If the capacitor is charged slowly, C_{DA} will eventually charge to the same value as C. But unfortunately, good dielectrics have very high resistances, so while C_{DA} may be small, Rs is large and the time constant RxC_{DA} typically runs into the millisecond range. In fast-charge, fast-discharge situations, the effect of DA resemble "memory".

EFFECTS OF DIELECTRIC ABSORPTION



This effect can be very damaging in data acquisition systems where many channels with widely varying data are being sampled by a sample-and-hold prior to conversion.



D.A. IN A SAMPLE-AND-HOLD

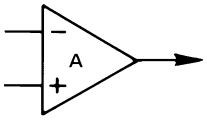
DECOUPLING, GROUNDING, AND ALL THAT

The best paper circuit designs often end up performing rather poorly when actually implemented. The source of much woe is often careless handling of grounds and power supply distribution. Most breadboards are brought up to full performance only after a long and often frustrating period of experimentation. While it is impossible to provide "cookbook" solution for every situation, some general rules may help in planning ahead and eventually troubleshooting ground headaches.

The first rule of arranging grounds and power distribution is to begin considering "ground" and "power" connections as the resistors and inductors they really are. As currents flow through these conductors, voltages will be produced. Knowing that these voltages exist and determining their effects is the first step toward eliminating the bulk of the problems in most systems.

Op Amp Signal Paths

The traditional op amp symbol shows a pair of differential inputs and a single output terminal. The problem with this symbol is no output reference point is shown. Clearly, any output voltage must be measured with respect to some point to which the amplifier has a reference, and neither input pin can serve that function (since the op amp is assumed to exhibit infinite common mode rejection). Therefore, the amplifier must have a fourth terminal.

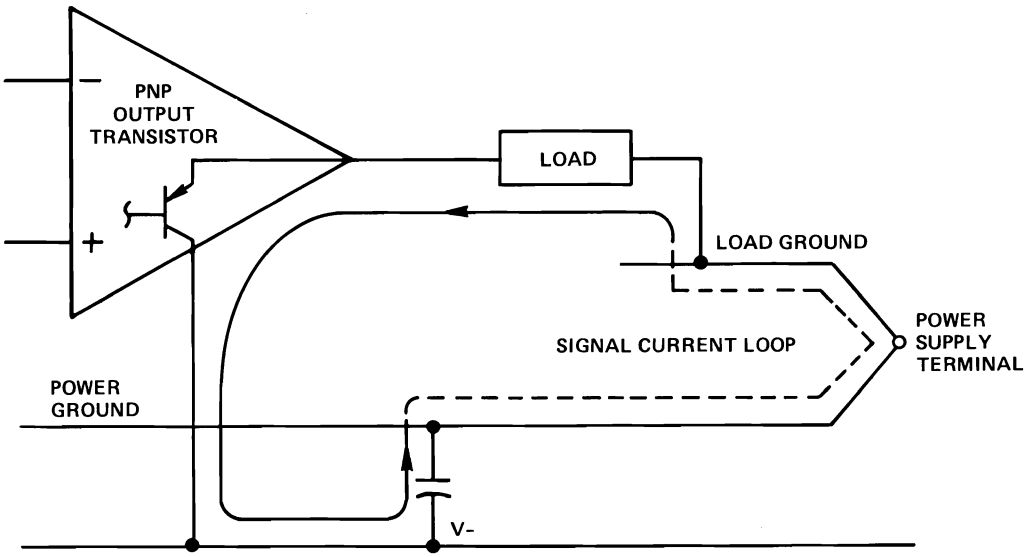


CONVENTIONAL "THREE TERMINAL" OP-AMP

Generally, the fourth terminal is "ground", since all voltages are assumed to be measured with respect to ground. Unfortunately, most op amps do not have a ground terminal, further confusing the issue. This dilemma is solved by assuming that the power supply lines represent a small-signal ground, and this assumption holds as long as these supply lines present a low impedance at all frequencies within the amplifier bandwidth. This is often not the case, and this is where the problems begin.

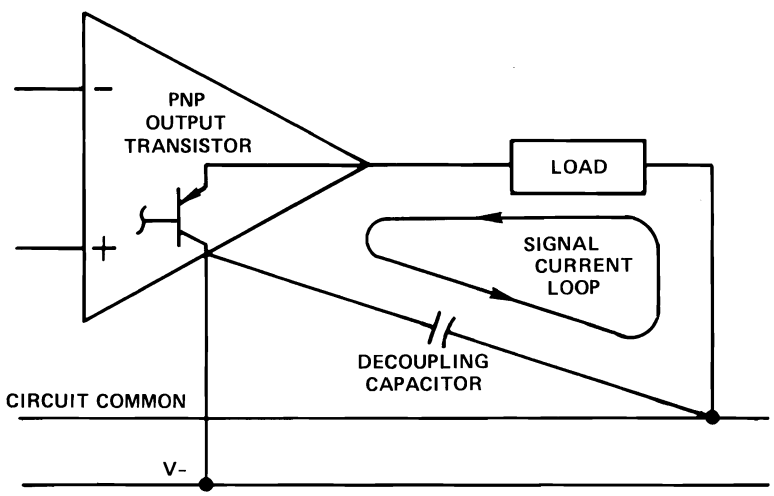
Consider the path through which signal current must flow in an op amp circuit. Current must flow from the power supply to the op amp, through the op amp, through the load, through the "ground" leads, and eventually back to the power supply. It is the voltage drops caused by the current flowing in the supply leads and ground impedances which can create havoc in a system. The traditional solution is "decoupling", a term only slightly less vague than "ground". Proper supply decoupling involves more than simply scattering capacitors around a circuit diagram.

An example of ineffective decoupling is the case in which an op amp drives a load which connects to a long ground line (returning to a power supply terminal), and the supply-decoupling for the amplifier returns to the power supply through another long line. The return path for load current is as long as or longer than the power supply lines powering the op amp. The "local" decoupling is not only ineffective, it may actually contribute to noise on the power-ground bus.



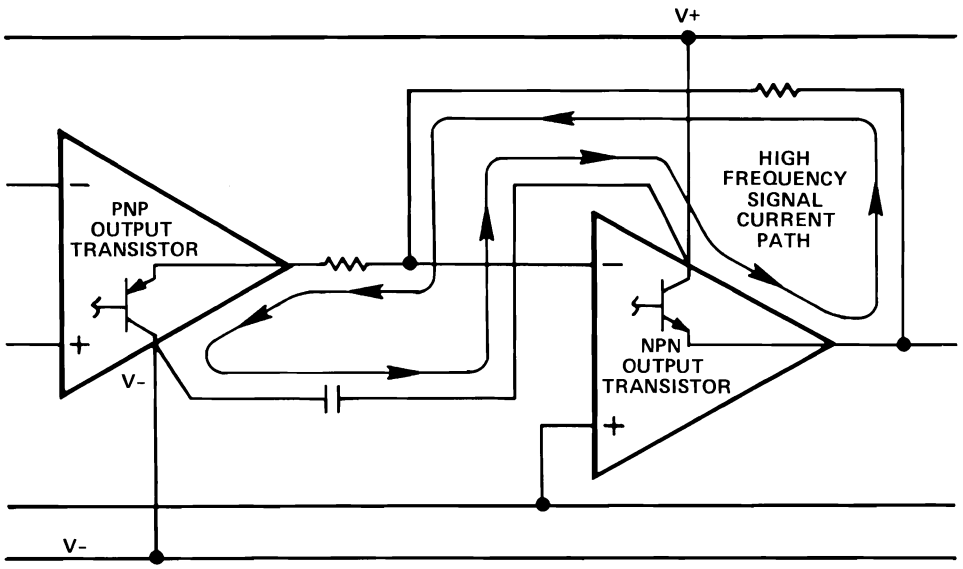
DECOUPLING FOR NEGATIVE SUPPLY INEFFECTIVE

The decoupling capacitor will be more effective it it connects by the shortest path between the load and the load-voltage control element. For example, an op amp swinging a resistive load circuit negative typically drives the load from an internal PNP transistor connected to V−. Decoupling the V− pin of the op amp to the low side of the load provides the most direct return path for high frequency currents and bypasses them around ground and power busses.



DECOUPLING NEGATIVE SUPPLY
OPTIMIZED FOR "GROUNDED" LOAD

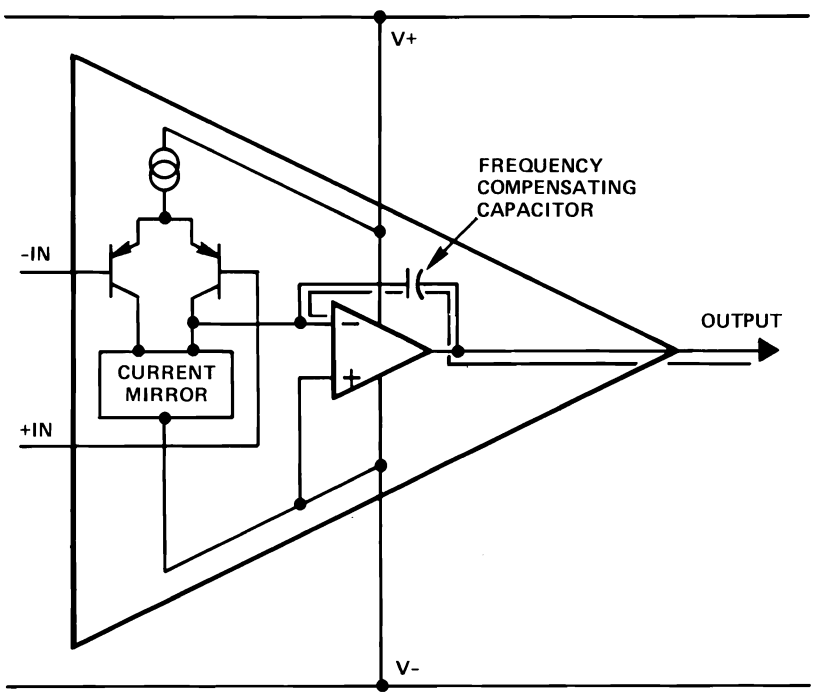
When the load situation is more complex, a little more thought is required. If the amplifier is driving a load that goes to a virtual ground, the actual load current does not return to ground. Rather, it must be supplied by the amplifier creating the virtual ground as shown in the figure. In this case, decoupling the negative supply of the first amplifier to the positive supply of the second amplifier closes the fast signal current loop without disturbing ground or signal paths.



DECOUPLING NEGATIVE SUPPLY
OPTIMIZED FOR "VIRTUAL GROUND" LOAD

The examples illustrated thus far have concentrated on decoupling techniques for the negative power supply. In reality, most op amps are indeed more sensitive to transients on one supply line than the other. To understand why, it is necessary to examine the inner workings of a typical IC op amp.

An op amp converts a differential input signal to a single-ended output signal. In many popular op amps the differential-to-single-ended conversion is done with respect to V−, and the resulting signal drives an integrator. The integrator characteristic is used to frequency-compensate the amplifier, and the integrator input is referred to the single-ended output, at V−, The integrator acts as a unity gain follower for fast signals applied to its noninverting (or reference) input. As a result, signals applied to the V− terminal have their high frequency components conveyed directly to the output. Signals having frequency components above the amplifier CLOSED-LOOP bandwidth will be transmitted from V− to the output with little or no attenuation.



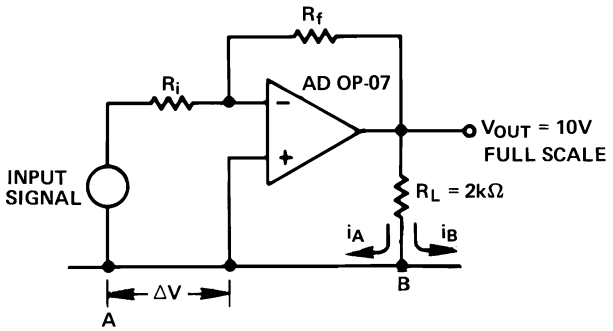
SIMPLIFIED "REAL" OP AMP

Some amplifiers have the integrator referred to the positive supply. In these amplifiers, of course, it is the positive supply which requires most care in decoupling. The table below details the integrator reference point for many Analog Devices products, both op amps and other products containing op amps.

Grounding

"Ground" in most electronic equipment is not an actual earth ground connection, but rather a common connection to which signals and power are referred. "Common" is a much better term for this connection, and implies (correctly) that this point must be made common. Recognizing that the impedances of ground interconnections will have voltages across them when currents flow through them is important to avoiding ground errors.

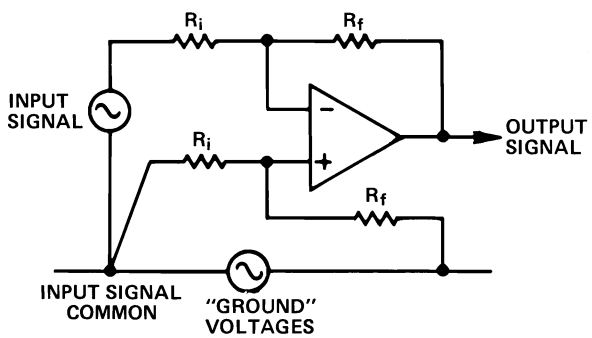
Consider the following situation: an AD OP-07 is used to amplify a low-level transducer signal as shown in the schematic below:



WHERE IS "GROUND"?

If the power supply ground is connected to point A, the load current must flow from the supply through the amplifier, load resistor, the wire connecting B and A, then back to the supply. If the wire from B to A is 22 gauge and 6 inches long, it presents a dc resistance of about 8 milliohms. While 8 milliohms may seem trivial with only 5mA of load current flowing, it does create a signal-dependent offset error of 40 microvolts if the power ground connects to point A. Obviously the advantage of using a precision amplifier is lost. Furthermore, this error represents positive feedback, and can cause the circuit to saturate, latch-up, or oscillate if the closed-loop gain is sufficiently high (250,000 in this example).

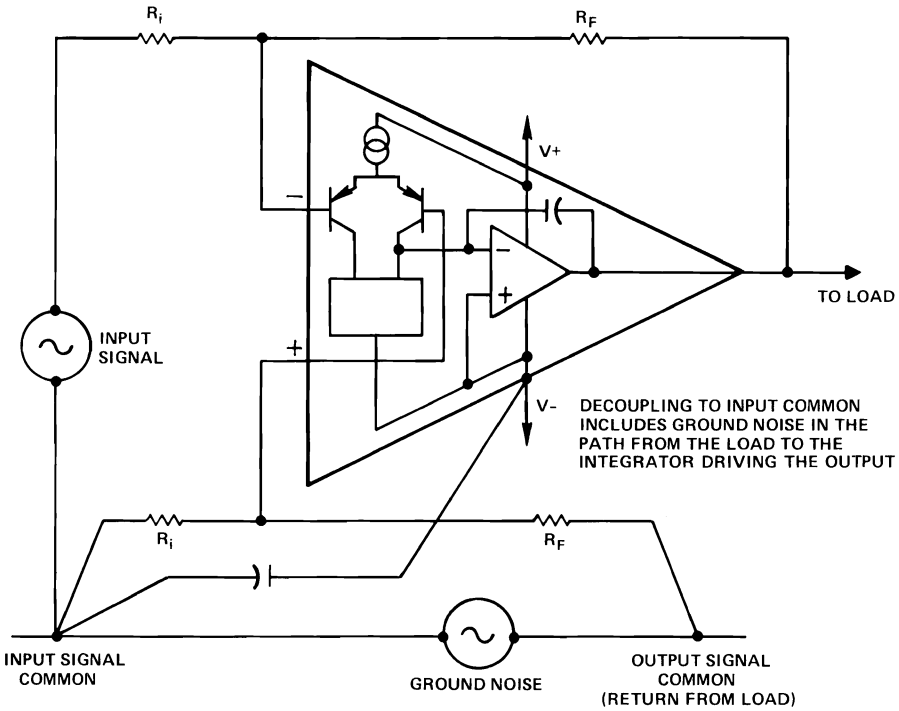
The solution is to connect the power ground to point B. This way, the shared path is eliminated. The exception to this solution is the case where the input signal source produces large currents which must return to the power supply. In this instance, the only solution is to resort to circuit structures which accept the fact that the voltage drops through certain interconnections are unavoidable. A subtractor amplifier as shown below can be used to reject errors due to grounding problems.



SUBTRACTOR AMPLIFIER
ELIMINATES GROUND PROBLEMS

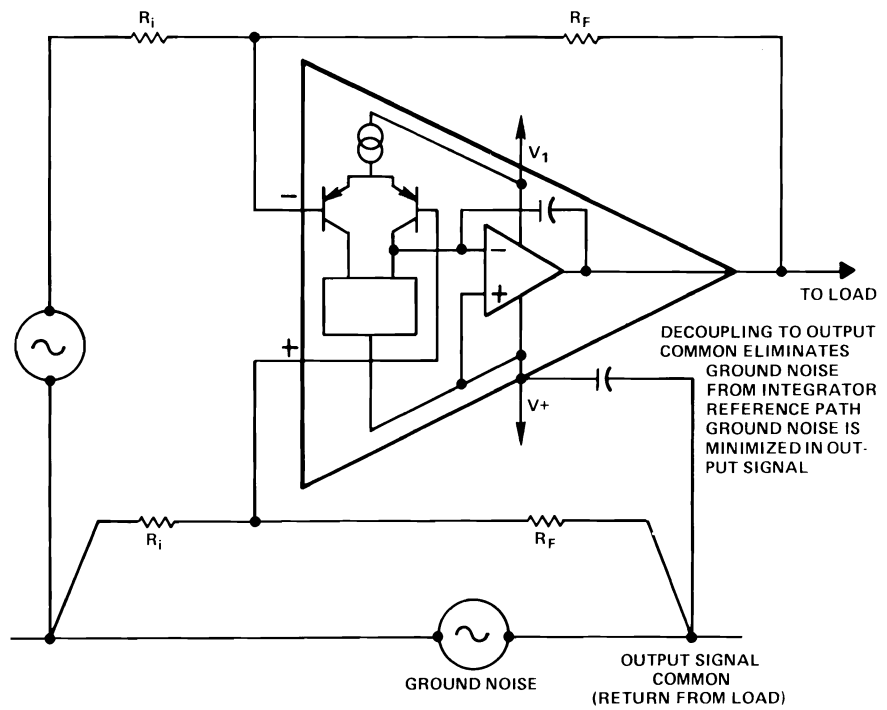
Bear in mind that even a perfect subtractor amplifier can fail to perform the intended function if it is poorly implemented. As will be discussed in the chapter on instrumentation amplifiers, resistor matching is critically important to realizing a subtractor. Furthermore, poor decoupling procedures can degrade the performance of a subtractor used to remove any high frequency ground noise.

Consider again the internal structure of an op amp. If a decoupling capacitor is inserted as shown from the amplifier's supply terminal to the signal common, the output signal high frequency path includes the ground noise that the subtractor was intended to eliminate. Another way of looking at the circuit is to consider the high frequency ground noise to be coupled directly into the negative supply lead of the amplifier, which has a high frequency gain of one to the output.



SUBTRACTOR AMPLIFIER INEFFECTIVE AT REJECTING GROUND NOISE

On the other hand, if the op-amp supply terminals are referred to the *output* signal common, no extraneous signals are coupled into the integrator. Any ground noise appears as a common-mode input signal and is reduced by the common-mode rejection of the amplifier, which is typically very much better than the negative-supply-voltage rejection at high frequencies.



SUBTRACTOR AMPLIFIER REJECTS GROUND NOISE

Printed Circuit Boards

PC boards are the "unseen components" in all precision circuit designs. Since the electrical characteristics of PC boards are rarely designed into a circuit, the overall effect is usually harmful to performance.

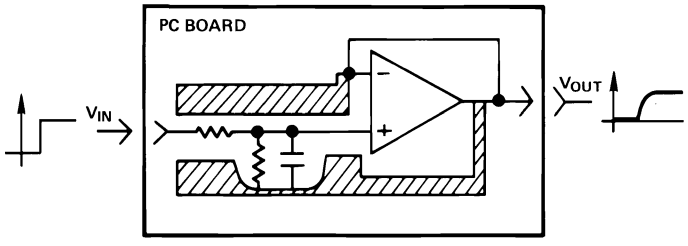
PC boards are usually intended to be a mechanical medium for interconnection and positioning of electrical components. From an electrical viewpoint, it offers the following advantages and disadvantages:

PRINTED CIRCUIT BOARD
ELECTRICAL OPPORTUNITIES AND PITFALLS

OPPORTUNITIES	PITFALLS
GROUND PLANES	LEAKAGE RESISTANCES
SHIELDS AND GUARDS	DIELECTRIC ABSORPTION
CLOSE PROXIMITY OF COMPONENTS	HYGROSCOPICITY
	TWO DIMENSIONAL LAYOUT (Less Flexible)
	STRAY CAPACITANCES
	"HOOK" (Capacitance Varies with Frequency)

Most designers rely on the reduction in size afforded by PC construction versus hand-wiring. While that may reduce noise pickup, the ability to apply shields and guards can be even more effective in improving circuit performance.

Placement of a guard track can preserve the high frequency response of a buffer amplifier by minimizing the differential voltage across parasitic impedances.



BOOTSTRAPPED BUFFER PRESERVES RESPONSE

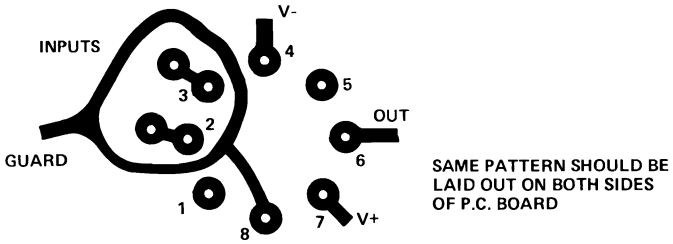
Ground planes and shields can be used to control capacitance on lines, reduce cross-talk and shield from noise.

On the negative side, the very two-dimensional nature of a PC board can become a barrier to proper circuit performance. If a hand-wired breadboard can, in its disorganized array, merely approach the desired performance, it is human nature to assume that "it will work in copper." Not so; in the breadboard, we can use air as a dielectric by suspending parts and wires in air, moving them anywhere we place. In PC design, we are much more restricted.

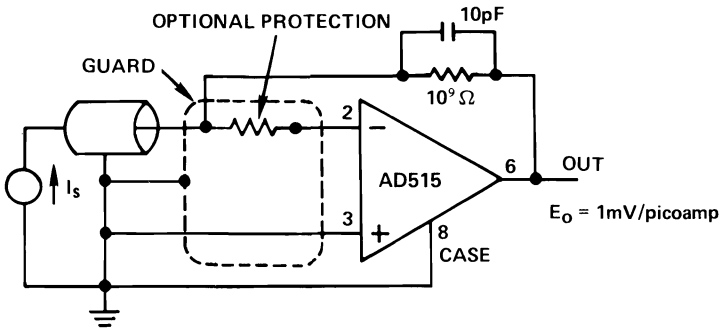
Conductors that carry small, high-precision or fast signals, or connect to high impedance terminations can cause problems in PC circuits by exposing those signals to parasitic resistances, capacitances or dielectric absorption. The effects of all of these parasitics would be the same as that of "real" components of the same type, ie, filtering, IXR drops, "memory", loading, etc. And, since PC material is hygroscopic, changes in humidity may cuase the contributions of these parasitic to vary!

When dealing with high impedance circuitry, such as low-level current measurement, circuit board layout can determine the success or failure of a circuit.

Most electrometer amplifiers (i.e., AD515, AD545) include a guard connection to the metal case of the device. This pin can independently be connected to a point at the same potential as the input terminals. Once again the idea is to minimize the differential voltage across parasitic circuit board impedances.

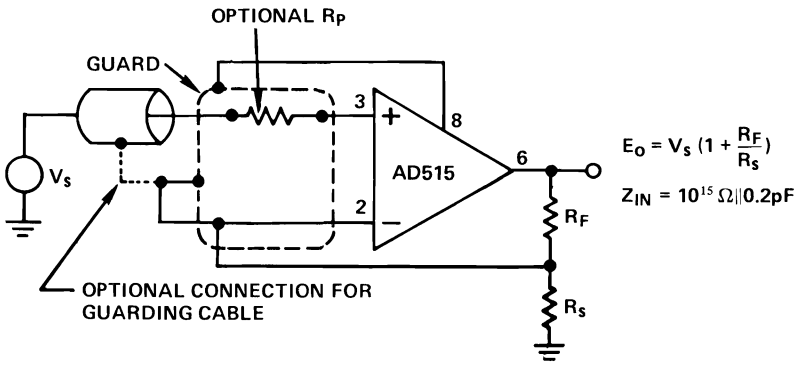


BOARD LAYOUT FOR GUARDING INPUTS



USE OF GUARD (INVERTING APPLICATION)

In an inverting application (including ground-referenced current-to-voltage converters), the guard should be connected to ground. In noninverting buffer applications, the feedback voltage is generally available from a lower impedance than the source voltage, and the guard should be connected to the appropriate feedback terminal.



USE OF GUARD (NON-INVERTING APPLICATION)

Another important concern for achieving and maintaining low leakage currents is complete cleanliness of circuit boards and components. Completed assemblies should be washed thoroughly in a low residue solvent such as TMC Freon or high-purity methanol followed by a rinse with deionized water and nitrogen drying. If service is anticipated in a high contaminant or high humidity environment, a high dielectric conformal coating is recommended. All insulation materials except Kel-F or Teflon will show rapid degradation of surface leakage at high humidities.

The following is a list of applications that may require special attention to PC considerations.

TYPICAL APPLICATIONS REQUIRING CAREFUL PRINTED CIRCUIT TECHNIQUES

- Electrometer Amplifiers
- Instrumentation Amplifiers
- Many Varied Signals Present
- 12-Bit Accuracy Required
- High Impedances
- RF or Fast-Rising Signals
- Fast Settling Required
- High Noise Environment
- High Humidity
- Impulse Response is Critical
- Low Capacitance Circuitry

Solutions are general in nature; not all apply in all instances. Below is a list of "helpful hints" that should be considered whenever PC problems are anticipated:

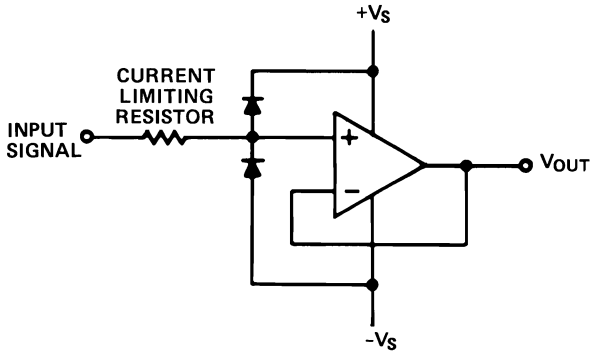
PRINTED CIRCUIT BOARD APPLICATION AIDS

- Improved PC Material
  (Teflon has low D.A., is highly moisture resistant, is stable over temperature)
- Qualify vendors and institute controls
- Bake the PC board to assure complete curing
- Critical conductors and components on Teflon standoffs and sockets.
- Ground planes and shields
- Guards for conductors with sensitive signals
- Low impedance designs where possible
- Breadboard must work better than required, operation must be fully understood
- Conformal coating – Beware! D.A. may cancel moisture resistance benefits
- Sensitive signals physically separated from digital logic
- Think like an electron – follow every track.

DEVICE PROTECTION

While most modern op amps are protected against in-circuit abuse, it is important to recognize the consequences of built-in and external amplifier protection schemes.

In monolithic op amps, catastrophic failure will generally result if any terminal voltage exceeds the supplies. If a circuit is to be built which may, under some circumstances (including power-up and power-down), present such voltages to the op amp, some protection is needed. Diodes, especially Schottky diodes are often used to protect amplifiers as shown below.



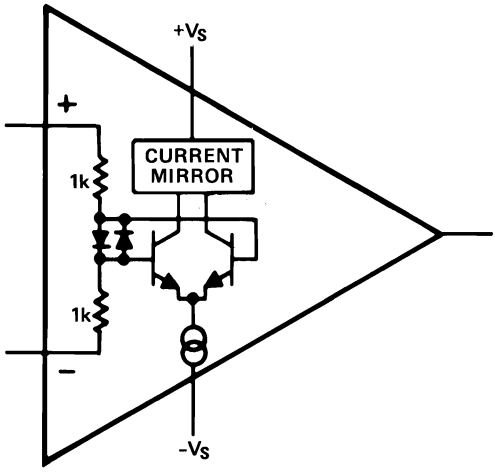
DIODE PROTECTION FOR OP AMP INPUT

Schottky diodes are preferable, since the overvoltage required to cause damage to an IC op amp is about the same as the forward voltage drop of a silicon diode. Schottky diodes, however, have a forward voltage only half that of a silicon diode, and will begin to conduct before a substrate diode turns on.

Diode protection has its pitfalls, however, All glass-encapsulated diodes are photo-diodes, and will begin to conduct if exposed to light. It is thus important that instruments using glass-packaged diodes be initially calibrated with the diodes exposed to the same light level as expected in actual operation.

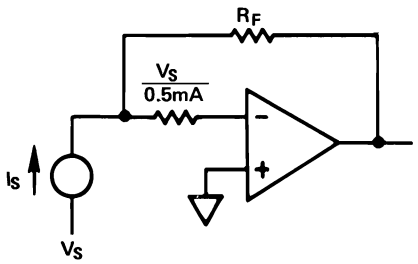
Many bipolar-input op amps use internal protection from excessive differential input voltages. In some instances, there may be no current limiting resistance.

One way to determine if a current-limiting resistor is included is to examine the voltage noise spec of the amplifier. Clearly, the Johnson noise of a protection resistor represents the minimum noise achievable by the op amp. A 1kΩ protection resistor generates $4nV/\sqrt{Hz}$ Johnson noise. Amplifiers with noise as low as this require external protection.



OP AMP INPUT PROTECTION (INTERNAL)

FET-input op amps effectively use the input JFET as the protection diode. External diode clamps are generally detrimental, since typical diode leakages exceed the input bias current in a modern FET-input op amp. However, external current limiting is in good taste to prevent overheating of the device in the event of an overvoltage. Such protection resistance is essential in many current sensing applications, where the current results from a potential of several hundred volts or more. This resistor is best placed inside the amplifier loop and chosen such that fault current is limited to 0.5mA or less.



PROTECTING I/V CONVERTER INPUT

Most op amp output stages include a mechanism to reduce the output if excessive current is frawn. Usually this current limiting reduces the maximum short circuit output current to about 25mA. However, it is good practice to consult the data sheet since some amplifiers (especially high-speed types) do not use current-limited output stages.

Section II

Special Purpose Amplifiers

Special Purpose Amplifiers

1) THE NEED FOR GAIN BLOCKS
2) LIMITATIONS OF OP AMPS
3) INSTRUMENTATION AMPLIFIERS
   - DESIGN TECHNIQUES
   - SPECIFICATIONS
   - APPLICATIONS
4) ISOLATION AMPLIFIERS
   - WHEN TO USE ISOLATION AMPLIFIERS
5) TRANSDUCER
   - TYPES
   - CHARACTERISTICS
   - INTERFACING
6) MONOLITHIC COLD JUNCTION COMPENSATION CIRCUIT

1. THE NEED FOR GAIN BLOCKS

The real world is characterized by deviations from the ideal; practical transducers rarely exhibit zero output impedances and convenient output ranges. Furthermore, environmental conditions usually complicate the process of data acquisition.

In the most simple situation, a transducer is connected directly to the data processing system; more often some amplification is required. Under laboratory conditions, this amplification may be provided by a simple op amp and a couple of resistors. Electrical interference, voltage drops caused by current through the resistance of leads from remote locations, nonlinear transducers, requirements for galvanic isolation and fluctuating temperatures often complicate the task of providing accurate amplification.

In this section, we will discuss various means of providing gain in an environment hostile to precision measurements. Instrumentation amplifiers will often serve those applications where isolation is not required and where extremely high common-mode voltages are not to be encountered. Isolation amplifiers are intended for use under those latter conditions.

WHY GAIN BLOCKS ARE REQUIRED

1) **Inconvenient Transducer Output Characteristics**
   - Format of Output (Capacitance, Resistance, Current, Voltage, etc)
   - High Output Impedances
   - Inconvenient Voltage Ranges
   - Unbalanced Outputs

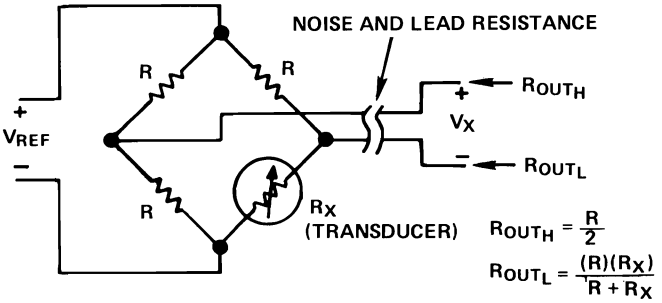
2) **Hostile Environmental Conditions**
   - Noise
   - High CMV
   - Remote Locations
   - Temperature Variances

3) **Requirements for Isolation**
   - Safety
   - Protection for Circuitry
   - Ground Loops

2. LIMITATIONS OF OPERATIONAL AMPLIFIERS

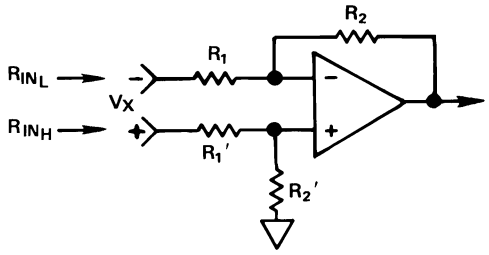
IC operational amplifiers are available with a wide variety of performance features. Costs are low for general purpose devices while increased precision and/or speed is available at slightly higher cost. Furthermore, the op amp is extremely versatile and can be configured to do more than simple amplification. Every analog circuit designer has at least a working knowledge of op amp techniques; this also serves to increase op amp usage. But in less than ideal situations, op amps have several serious shortcomings.

Practical transducer applications usually involve differential connections, nonzero source impedances and noise. A typical application is shown below:



PRACTICAL TRANSDUCER CIRCUIT WITH DIFFERENTIAL OUTPUT

It can be seen that the output impedance of such a circuit is nonzero and, in general, unbalanced. Lead resistance and noise pickup can not be totally avoided. A differential amplifier is required to sense output voltage, but a single op amp in a differential configuration is not well suited to such nonideal applications.



- Low Input Impedance
- Unbalanced Input Impedances
- Common Mode Rejection Depends on Resistor Ratio-Matching

OP AMP IN DIFFERENTIAL CONNECTION

For balanced gain, $G = \frac{R_2}{R_1} = \frac{R_2'}{R_1'}$

For balanced input impedance, $R_1' + R_2' = R_1$

To provide balanced impedance return paths for amplifier bias currents (to minimize offset voltage drift),

$$\frac{R_1 R_2}{R_1 + R_2} = \frac{R_1' R_2'}{R_1' + R_2'},$$

Furthermore, these mutually exclusive conditions are only valid for ideal transducers. Finite input impedances, even if balanced, can disturb unbalanced transducers; lead resistance further aggravates the situation.

Op amp common-mode rejection is typically between 60 and 90dB (some types, like the AD517, may have up to 110dB). This may not be sufficient to reject common-mode noise.

Nor is there galvanic isolation between input and output. Signal superimposed upon common-mode voltages in excess of ±10 volts can not be handled and if the common-mode input voltage exceeds supply voltage, the op amp might be destroyed.

3. INSTRUMENTATION AMPLIFIERS

An instrumentation amplifier (IA) is a precision differential voltage gain device that is intended for use when acquisition of a useful signal is difficult. IA's are characterized by high input impedances, low bias currents, high common-mode rejection, balanced differential inputs and stable, well characterized specifications. Gain is determined by pin strapping, user-selectable resistor or resistor pair. All other necessary precision components are internal thus allowing the manufacturer to guarantee a specified level of performance. The output is a single-ended; usually sense and output reference terminals are provided.

INSTRUMENTATION AMPLIFIER CHARACTERISTICS

1) High Input Impedances
2) Low Bias Currents
3) High Common-Mode Rejection
4) Balanced Differential Inputs
5) Stable, Well-Characterized Specifications
6) Gain Determined by User-Selectable Resistor or Resistor-Pair
7) Single-Ended Output

SPECIFICATIONS

The performance of an IA is described by its specifications. Some specifications are self-explanatory and are not unique to IA applications. Other specifications are very significant when precision amplification in a real-world environment is required; a discussion of such specs follows.

Gain Equation

The gain of an IA is determined by pin strapping of internal resistors or externally applied resistors. The specification of relationship between the desired gain and amplifier gain is called the gain equation.

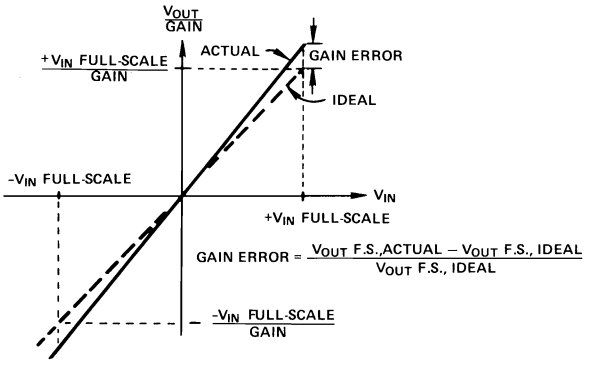
Gain Range

This specification indicates the range of gains that the manufacturer recommends for proper operation. The IA may indeed function at higher or lower gains, but the manufacturer does not guarantee any particular level of performance. In practice, lower gains may compromise stability while higher gains may be impractical due to increased noise and drift.

Equation Error

The number given by this specification describes maximum deviation from the gain equation. The user can

usually trim the gain or can compensate elsewhere in his design. If his data is eventually digitized and fed to an "intelligent system" (such as a microprocessor), he might be able to correct for gain errors by measuring a reference and multiplying by a constant.



GAIN ERROR

Gain vs. Temperature

These numbers give both maximum and typical deviations from the gain equation as a function of temperature. An intelligent system can correct for this with an "auto-gain" cycle (measure a reference and re-normalize).

Nonlinearity

Nonlinearity is defined as the deviation from a straight line on the plot of output versus input. The following figure shows the transfer function of a device with exaggerated nonlinearity. The magnitude of this error can be calculated thus:

NONLINEARITY CALCULATION

$$\text{N.L.} = \frac{\text{(ACTUAL OUTPUT)-(CALCULATED OUTPUT)}}{\text{RATED FULL SCALE OUTPUT RANGE}}$$

This deviation can be specified relative to any straight line or to a specific straight line. There are two commonly-used methods of specifying this straight line relative to the performance of a precision measurement device.

The "Best Straight Line" method of nonlinearity specification consists of measuring the peak positive and negative deviations and adjusting the slope of the device transfer function (by adjusting the gain and offset) so that these maximum positive and negative errors are equal. This method yields the best specifications but it is difficult to implement in that it requires that the user examine the entire output signal range to determine these maximum positive and negative deviations.

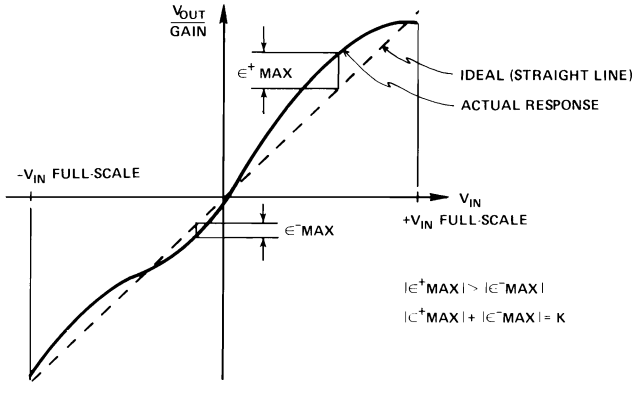
The "End-Point" method of specifying nonlinearity requires that the user perform his offset and/or gain calibration at the extremes of the output range. This is much easier to implement but may result in nonlinearity errors of up to twice those attained with best-straight-line techniques. This worst case will occur when the transfer function is "bowed" in one direction only.

Most linear devices, such as instrumentation amplifiers, are specified for best-straight-line linearity. The user must take this into consideration when evaluating the application error budget.

Nonlinearity errors are irreducible; in other words, these errors are neither fixed nor proportional to input or output voltage and can not be reduced by adjustment.

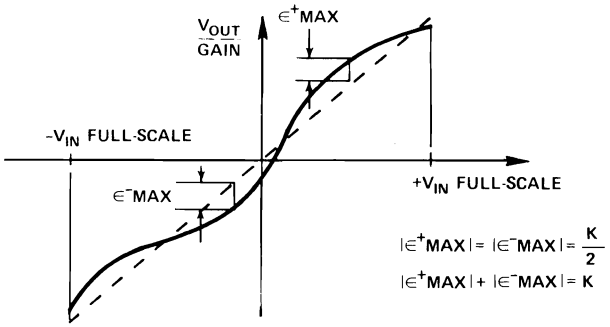
In some IA's, nonlinearity increases with gain.

NONLINEAR TRANSFER FUNCTION

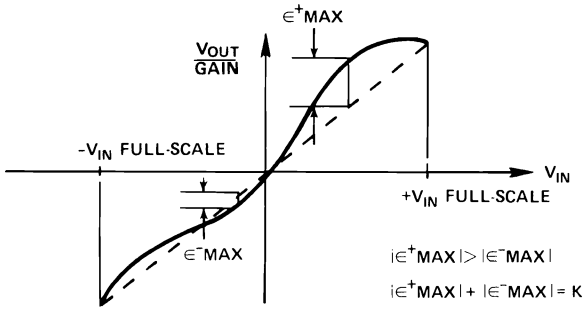


a). TRANSFER FUNCTION ILLUSTRATING EXAGGERATED NONLINEARITY.

NONLINEAR TRANSFER FUNCTION



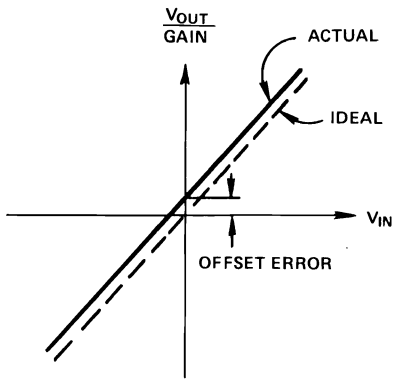
b). TRANSFER FUNCTION a.) AFTER CALIBRATION BY BEST-STRAIGHT-LINE METHOD.



c). TRANSFER FUNCTION a.) AFTER CALIBRATION BY END-POINT METHOD.

Voltage Offset

Initial voltage offset may be adjusted to zero but shifts in offset voltage could cause errors. Intelligent systems can often correct with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability. Voltage offset and offset drift comprise two components; input and output offset and offset drift. Input offset is that component of offset that is directly proportional to gain, i.e., input offset as measured at the output with G = 100 is 100 times greater than with G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by a drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which means that the effect on the output is "G" times larger. Voltage offset vs power supply is also specified at one or more gain settings and is also RTI.



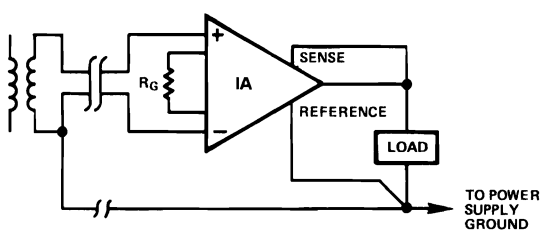
OFFSET ERROR

Input Bias Current

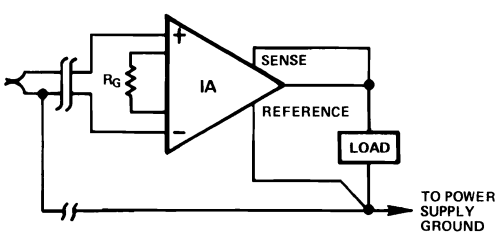
Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. FET input devices have lower bias currents, but those currents increase dramatically with temperature, doubling approximately every 10°C. Since bias currents can be considered as a source of voltage offset (when multiplied by source resistance), the change in bias currents is of more concern than the magnitude of the bias currents. Input offset current is the difference between the two input bias currents.

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground. Suitable connections are shown below. If it is impossible to provide a dc path for bias currents, an isolation amplifier will be required.

INDIRECT GROUND RETURNS FOR BIAS CURRENTS

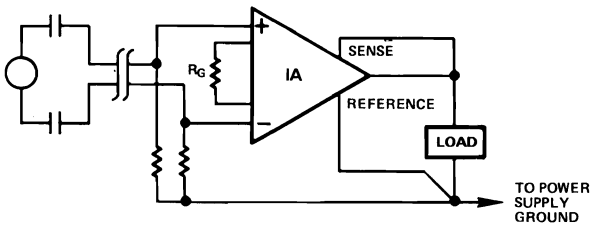


a). TRANSFORMER COUPLED



b). THERMOCOUPLE

INDIRECT GROUND RETURNS FOR BIAS CURRENTS

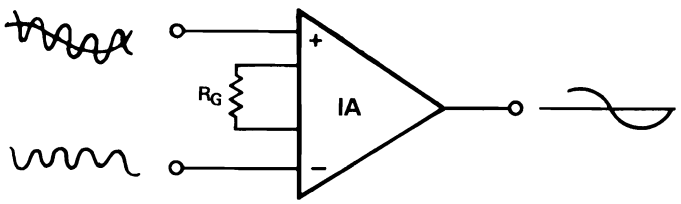


c). AC COUPLED

Common-Mode Rejection Ratio

The Common-Mode Rejection Ratio is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-Mode Rejection Ratio" (CMRR) is a ratio expression while "common-mode rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80dB.

In most IA's the CMRR increases with gain. This is because most designs have a front-end configuration that does not amplify common-mode signals. Since the standard for CMRR specifications is referred to the output (RTO), a gain for differential signals in the total absence of gain for common-mode output signals will yield to 1-to-1 improvement of CMRR gain. This means that the common-mode output error signal will not increase with gain; it does not mean that it decreases with gain! At higher gains, however, amplifier bandwidth decreases. Since differences in phase-shift through the differential input stage will show up as a common-mode error, CMRR becomes more frequency-dependent at high gain.



COMMON MODE REJECTION

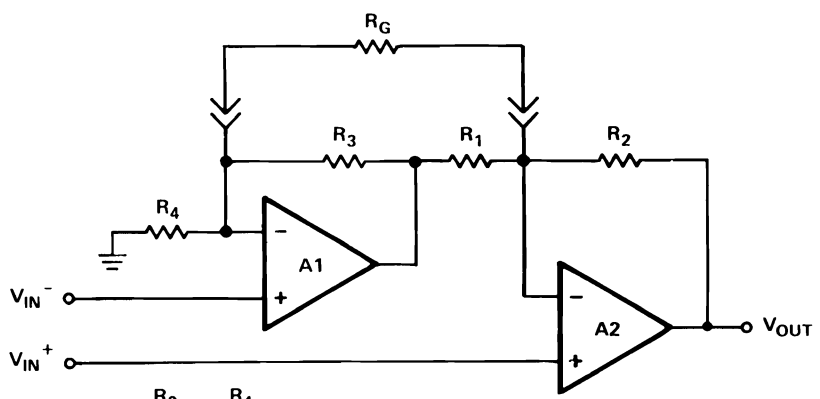
Settling Time

Settling time is defined as that length of time required for the output voltage to approach and remain within a certain tolerance of its final value. It is usually specified for a fast full scale input step and includes output slewing time. Since several factors contribute to the overall settling time, fast settling to 0.1% doesn't necessarily mean proportionally fast-settling to 0.01%. In addition, settling time is not necessarily a function of gain. Some of the contributing factors include slew rate limiting, under-damping (ringing) and thermal gradients ("long tails").

DESIGN TECHNIQUES

The most easily visualized IA configurations are based on IC op amps. The single-op-amp differential stage previously shown is the most simple IA design, but it lacks the performance required for precision applications.

There is a two-amplifier IA design that overcomes some of the weaknesses in the one-amp approach.



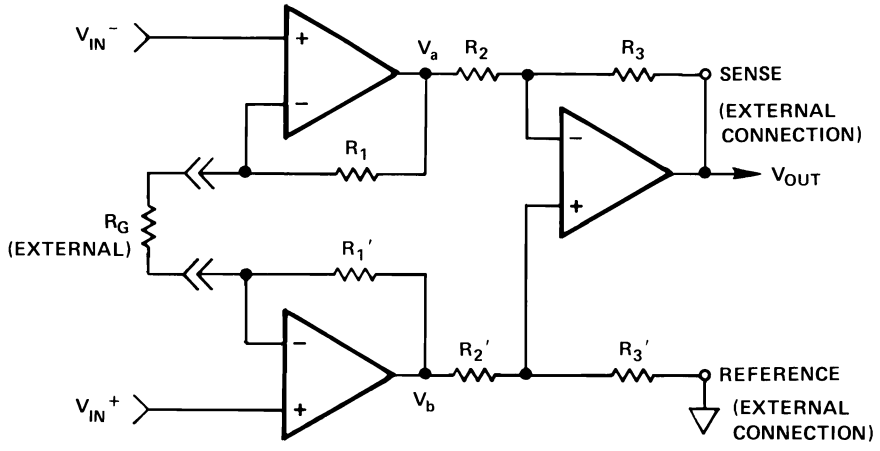
$$\text{IF } \frac{R_2}{R_1} = \frac{R_4}{R_3} \qquad V_{IN} = V_{IN}^+ - V_{IN}^-$$

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_2}{R_1} + \frac{2R_2}{R_G}$$

"TWO-AMPLIFIER" INSTRUMENTATION AMPLIFIER

Input resistance is high, thus permitting the signal sources to have unbalanced, nonzero output impedance. The major disadvantage of this design is that the common-mode voltage input range must be "traded-off" against gain range. A1 is called upon to amplify a common mode signal by the ratio $\frac{R_3 + R_4}{R_4}$ if $R_3 > R_4$, saturation of A1 could occur thus leaving no "headroom" to amplify the differential signal of interest. If $R_3 < R_4$, low gains can not be realized.

The most popular configuration for op-amp based instrumentation amplifiers is shown below.



"CLASSIC" 3 OP AMP INSTRUMENTATION AMPLIFIER

The transfer function of this circuit is:

$$V_{OUT} = (V_{IN}^+ - V_{IN}^-)\left(\frac{2R_1}{R_G} + 1\right)\left(\frac{R_3}{R_2}\right)$$

where $R_3 = R_3'$, $R_2 = R_2'$ and $R_1 = R_1'$

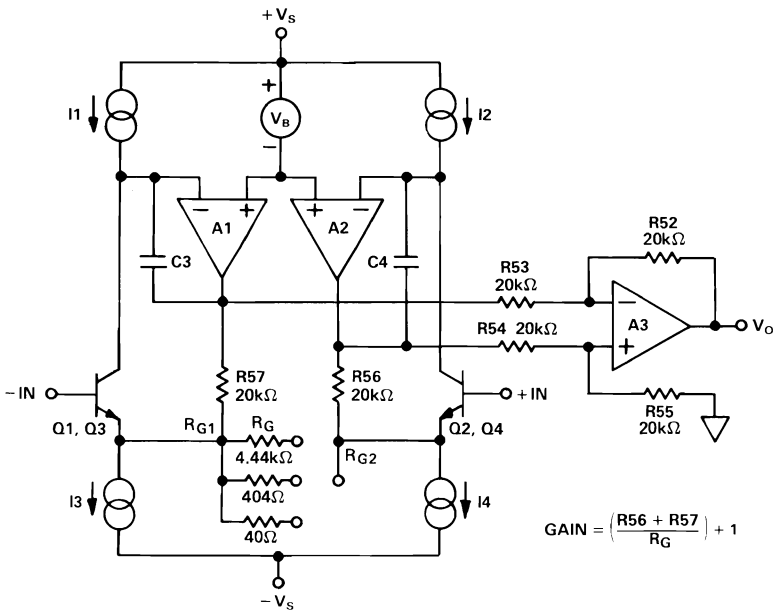
In this configuration, gain accuracy and CMR depends upon the ratio matching of R_2, R_2', R_3 and R_3'. It can be shown, however, that CMR does not depend on the matching of R_1 and R_1'.

Within limits, the user may take as much gain in the front end as he wishes (as determined by R_G) without increasing the common-mode error signal. Thus CMR will theoretically increase in direct proportion to gain, a very useful property. Furthermore, common-mode signals are only amplified by a factor of 1 regardless of gain (no common-mode voltage will appear across R_G, hence, no common-mode current will flow in it because the input terminals of an op-amp operating normally will have no significant potential difference between them). This means that large common-mode signals (within the op amp limits) may be handled independent of gain.

Finally, because of the symmetry of this configuration, first order common-mode error sources in the input amplifiers, if they track, tend to be cancelled out by the output stage subtractor. Examples of IA's thus configured include the AD522, AD524, AD612 and AD624. This product is characterized by its extremely high precision. IAs of this type may use either FET or Bipolar input operational amplifiers. FET input devices have very low bias currents and are well-suited for use with very high source impedance. FET input op amps, however, generally have poorer CMR than bipolar amplifiers because nongeometry-related mismatches usually cause larger input offset voltage drifts.

The AD524 and AD624 are monolithic instrumentation amplifiers based on the classic 3 op amp circuit. The advantage of monolithic construction is the closely matched components required to construct the preamp. The preamp section develops the programmed gain by the use of feedback concepts. The programmed gain is developed by varying the value of R_G (smaller values increase the gain) while the feedback forces the collector currents of Q1, Q2, Q3, Q4 to be constant which impresses the input voltage across R_G.

As R_G is reduced to increase the programmed gain, the transconductance of the input preamp increases to the transconductance of the input transistors. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000, thus reducing gain related errors to a negligible 30ppm. Second, the gain bandwidth product which is determined by C3 or C4 and the input transconductance, reaches 25MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of $4nV/\sqrt{Hz}$ at G = 1000.

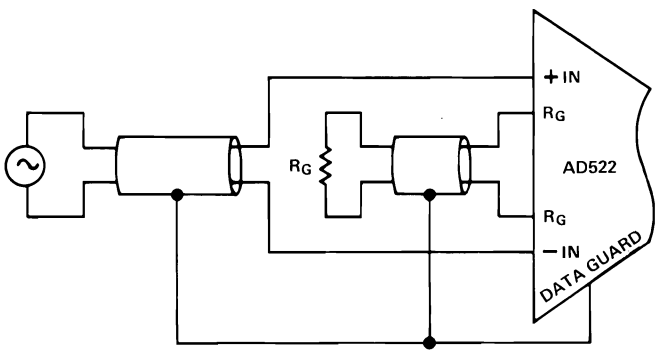


AD524/AD624 SIMPLIFIED SCHEMATIC

APPLICATION NOTES

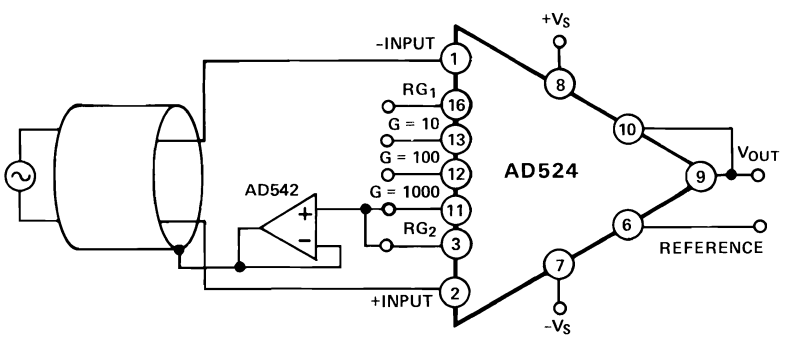
Data Guard

Signals from remote transducers are often transmitted to the IA through shielded cables. While this may reduce noise pickup, the distributed RC's in such cabling can cause differential phase shifts in those lines. When ac common-mode signals are present, these phase shifts will reduce common-mode rejection. The same effect will occur with remote R_G's located at the end of shielded cables. If the shields are driven by the common-mode signal, the cable capacitance is "boot-strapped" thus making the capacitance effectively zero for common-mode signals. The data guard output of the AD522 provides the common-mode component of the input signals and can be used to drive the shields of coaxial input cables and increase ac CMR. If not used, the data guard should be left unconnected.

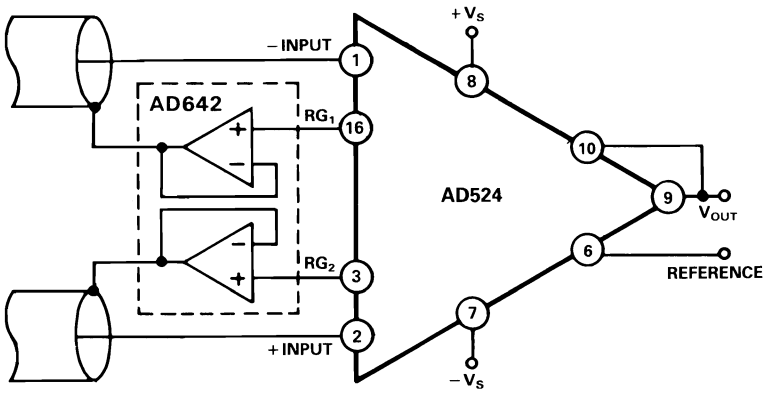


USE OF DATA GUARD OUTPUT

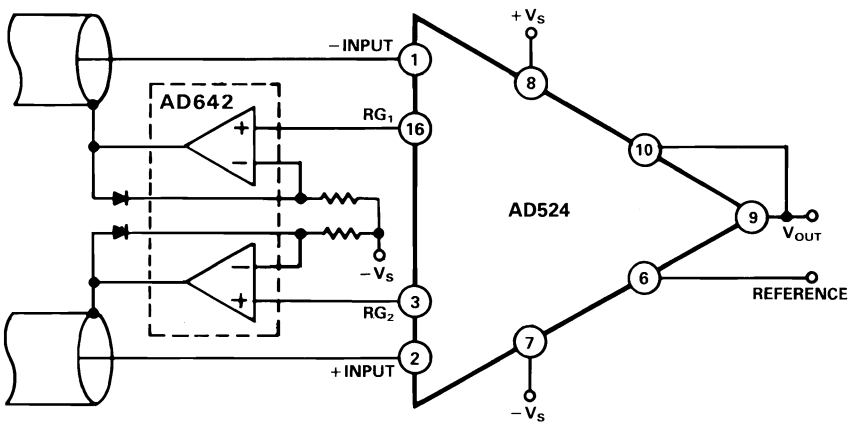
In some instrument amplifiers, due to pin limitations, the data guard is not available externally. The AD524 and AD624 are two such amplifiers. The common-mode voltage is available at R_{G2} and can be used by buffering it with a operational amplifier. The operational amplifier should be a FET input amplifier which has a very low bias current like the AD542 because the bias current flowing through the gain setting resistor will cause a gain error.



SHIELD DRIVER FOR G ⩾ 100



DIFFERENTIAL SHIELD DRIVERS



IMPROVED DIFFERENTIAL SHIELD DRIVER

PC boards are the "unseen components" in all precision circuit designs. Since the electrical characteristics of PC boards are rarely designed into a circuit, the overall effect is usually harmful to performance.

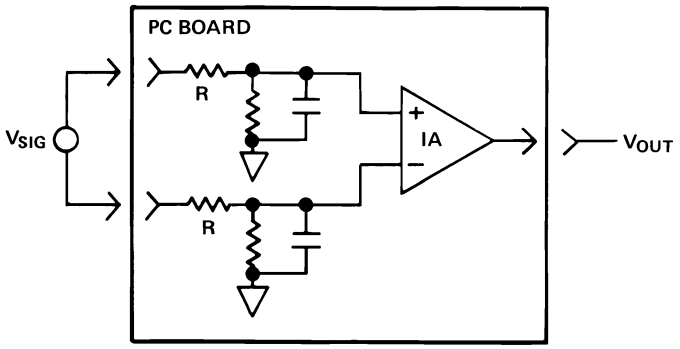
PC boards are usually intended to be a mechanical medium for interconnection and positioning of electrical components. From an electrical viewpoint, it offers the following advantages and disadvantages:

PRINTED CIRCUIT BOARD ELECTRICAL OPPORTUNITIES AND PITFALLS

OPPORTUNITIES	PITFALLS
GROUND PLANES	LEAKAGE RESISTANCES
SHIELDS AND GUARDS	DIELECTRIC ABSORPTION
CLOSE PROXIMITY OF COMPONENTS	HYGROSCOPICITY
	TWO DIMENSIONAL LAYOUT (Less Flexible)
	STRAY CAPACITANCES
	"HOOK" (Capacitance Varies with Frequency)

Most designers rely on the reduction in size afforded by PC construction versus hand-wiring. While that may reduce noise pickup, the ability to apply shields and guards can be even more effective in improving circuit performance.

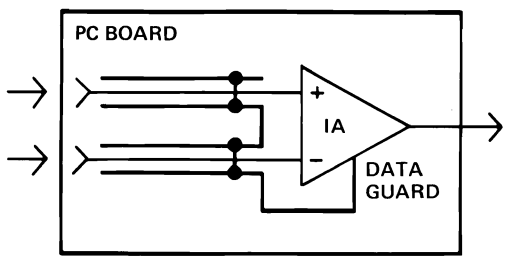
In some circuits, wiring capacitance and leakage resistance can degrade performance. In an instrumentation amplifier, ac common mode rejection is only as good as differential phase shift:



PARASITICS IN PRINTED CIRCUITS

Unequal drops across differing PC Board track resistances and differential phase shift due to varied stray capacitances can cause a decrease in common-mode rejection similar to the effect of a long input cable.

A Data Guard allows the common-mode rejection to be restored by guarding the inputs as shown below.



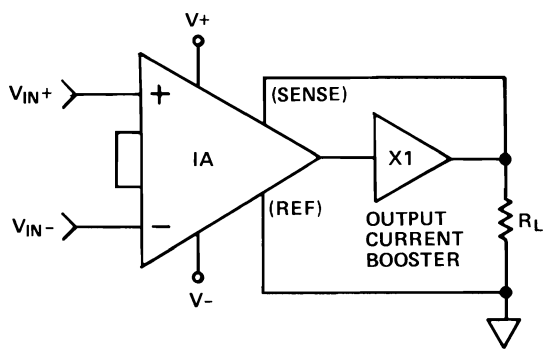
DATA GUARD "BOOTSTRAPS" PARASITICS FOR COMMON-MODE-SIGNALS

Thus the parasitic components of the PC board are "bootstrapped" for common mode signals. That is, if there is no voltage across the strays and leakages, then no current flows. Therefore, the effects of these parasitics are nil.

Sense Terminal

The sense terminal is the feedback point for the IA output amplifier. Normally it is connected to the IA output. If heavy load currents are to be drawn through long leads, IR drops can cause errors. The sense terminal can be wired to the IA output at the load thus putting IR drops "inside the loop" and virtually eliminating this error source.

Another use for the sense terminal is shown below:



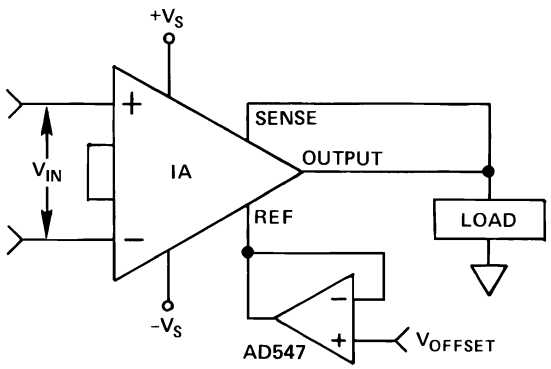
INSTRUMENTATION AMPLIFIER WITH OUTPUT CURRENT BOOSTER

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. A high-current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current boost without significantly degrading overall performance. Nonlinearities, offset and gain inaccuracies of the buffer are minimized by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

Reference Terminal

The reference terminal may be used to offset the output by up to ±10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset.

When the IA is of the three-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal. Any significant resistance from the reference terminal to ground increases the gain of the noninverting signal path thereby upsetting the common-mode rejection of the IA. An operational amplifier may be used to provide that low impedance reference point as shown below.



USE OF REFERENCE TERMINAL TO PROVIDE OUTPUT OFFSET

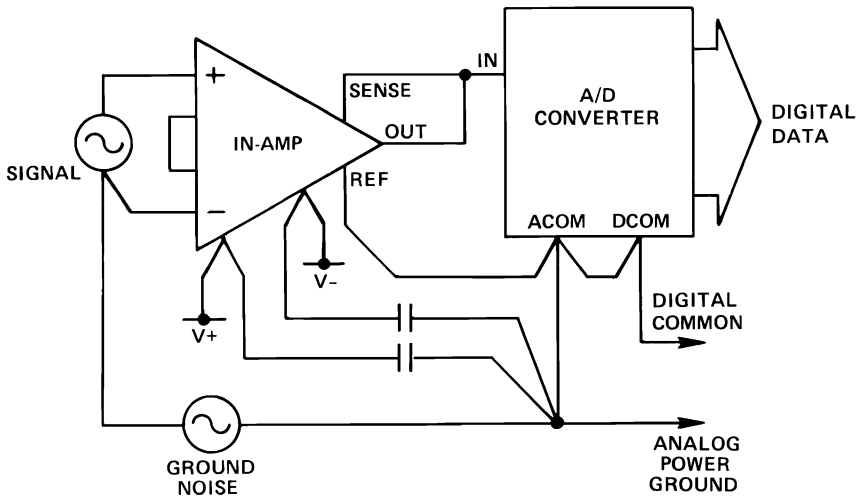
Grounding and Decoupling

Data acquisition components usually have two or more ground pins which are not connected together within the device but have to be connected to a ground system externally. Ideally, a single solid ground would be desirable and typically that's what's done. The result is that great amounts of effort and many decoupling components are spent attempting to correct problems created by poor ground-current management. In large systems and systems which combine high-level signals with low-level signals, "Ground" (or common bus) management becomes an important aspect of design. Allowing low-level analog signals to share conductors with logic returns or power connections is an invitation to trouble.

In large systems it is often impractical to rely on a single common point for all analog signals. In these cases, some form of differential amplifier is required to translate signals between grounding systems. A simple subtractor or instrument amplifier can often be used for this purpose. These circuits translate a signal which is referred to one ground system into a similar or amplified signal which is referred to a different ground system. The common-mode rejection of the amplifier is used to eliminate the effects of voltage differences between the two grounds or common points.

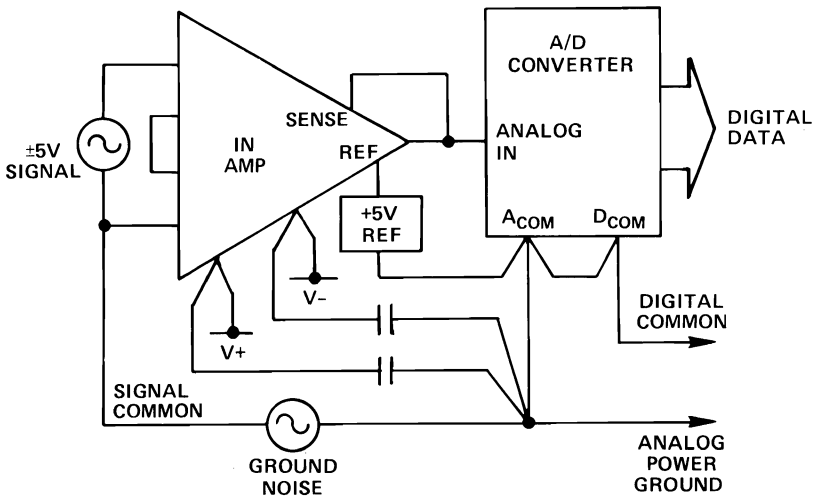
If an operational amplifier is used as a subtractor then the op amp should be powered from the load power, and/or decoupled with respect to load common. The reason for this can be deduced from the circuit architecture of the most-common types of op amps. An op amp converts a differential input signal to a single-ended output signal. In many popular op amps the differential-to-single-ended conversion is done with respect to V–, and the resulting signal drives an integrator. The integrator characteristic is used to frequency-compensate the amplifier, and the integrator input is referred to the single-ended output, at V–. The integrator acts as a unity gain follower for fast signals applied to its noninverting (or reference) input. As a result, signals applied to the V– terminal have their high frequency components conveyed directly to the output. Signals having frequency components above the amplifier CLOSED-LOOP bandwidth will be transmitted from V– to the output with little or no attenuation.

As discussed in Section I the noise-rejection performance of the subtractor depends on carefully matched source and feedback resistance ratios, it cannot be used in all situations. Whenever the source impedance cannot be controlled or is exceptionally high, the subtractor (or dynamic bridge) becomes impractical. In this situation, ground noise and other remote grounding difficulties can often be avoided by the use of an Instrumentation Amplifier. The "In-Amp" accepts differential input signals at its high-impedance input. It provides a fixed gain, which can be selected without introducing overall feedback that joins the input and output circuitry. The output signal is developed with respect to a reference terminal, which may be connected to the input common of a remote load-circuit.



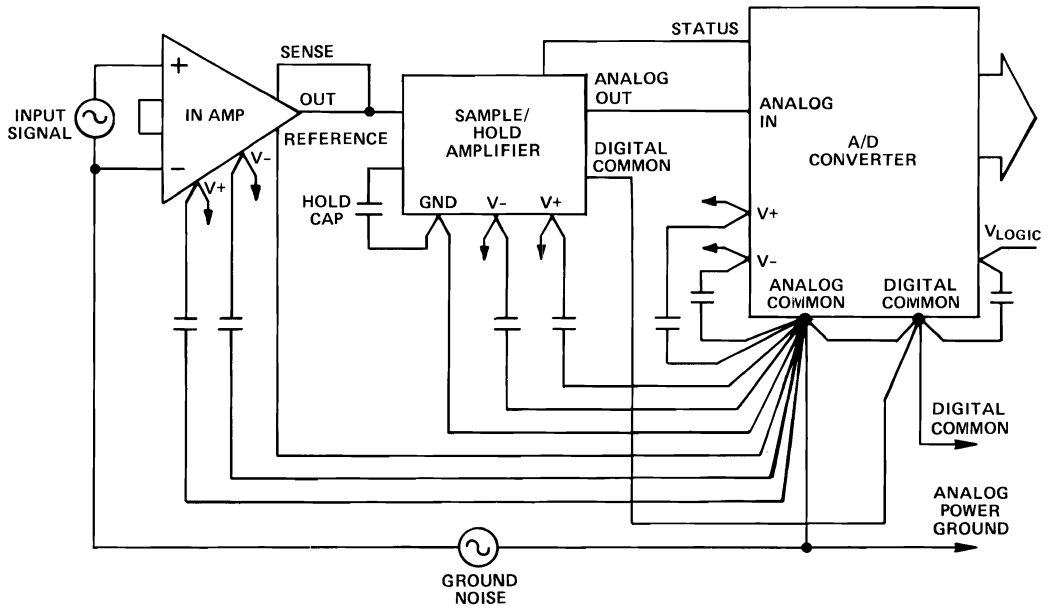
INSTRUMENTATION AMPLIFIER SIMPLIFIES SIGNAL CONDITIONING FOR A/D CONVERTER

Some In-Amps are quite versatile and can be adapted to provide additional functions while they isolate common returns. For example, one may desire to convert a bipolar input signal with a unipolar ADC. By referring the In-Amp output to a +5-volt point, the ±5-volt amplifier input signal will appear as a 0 to +10 volt signal to the converter. This extra feature can be provided without compromising the ground noise rejection of the system.



INSTRUMENTATION AMPLIFIER USED FOR BIPOLAR OFFSET AND ISOLATION

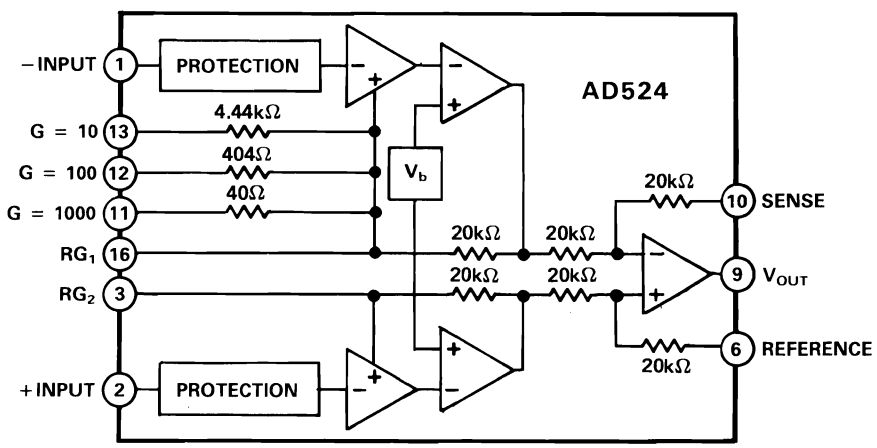
In a data acquisition system that contains instrument amplifiers, sample and hold ampliers and A/D converters the grounding problems become complex. In a complex system the analog subsystem should be powered by a supply with a local common return which may be connected to the digital common but does not share any current-carrying conductors. Ideally, there are no "foreign currents" which flow between the analog system and the digital system, except for those within the converter. If the two systems are joined only at the converter, the foreign currents share the shortest path, and their effect is minimized.



DATA ACQUISITION SYSTEM GROUNDING

AD524 FEATURES

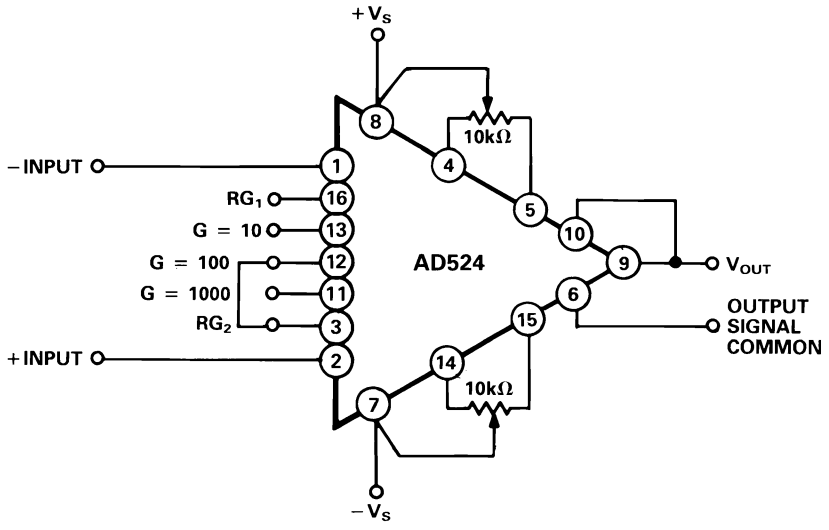
Low Nonlinearity: 0.005% (G = 1)
High CMRR: 130dB (G = 1000)
Low Offset Voltage: 50μV
Low Offset Voltage Drift: 0.5μV/°C
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 10, 100, 1000
Complete Input Protection, Power On – Power Off
No External Components Required
Internally Compensated



AD524 FUNCTIONAL BLOCK DIAGRAM

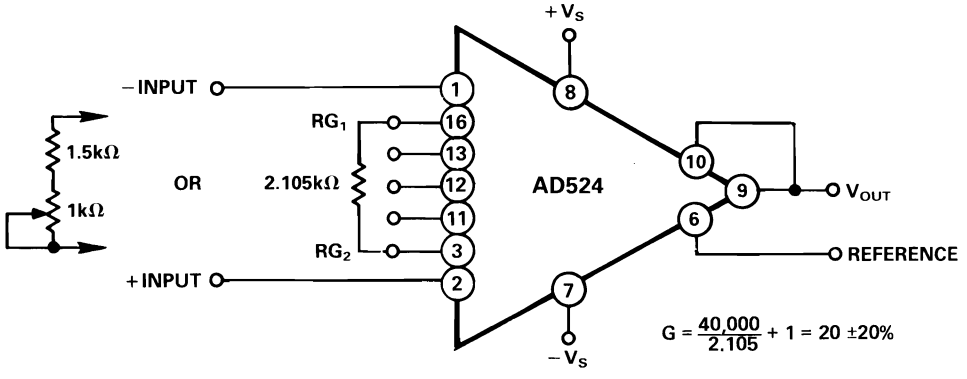
The AD524 provides for both input and output offset adjustments. This simplifies the calibration procedure in very high precision applications and minimizes offset voltage changes in switched gain applications. In switched gain applications the output offset is adjusted first at G = 1 then the input offset is adjusted at the highest programmed gain.

The AD524 has internal high accuracy pretrimmed resistors for pin programmable gains of 1, 10, 100 and 1000. One of the preset gains can be selected by pin strapping the appropriate gain terminal and RG_2 together.



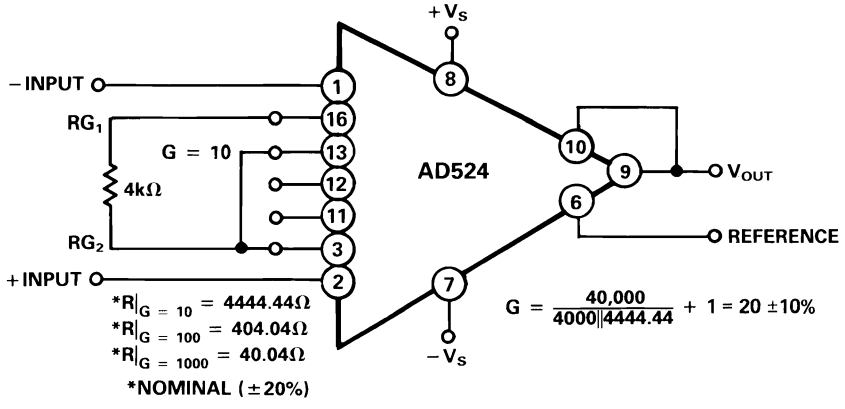
OPERATING CONNECTIONS FOR G=100

The AD524 can be configured for gains other than those that are internally preset, there are two methods to do this. The first method uses just an external resistor connected between pins 2 and 16 which programs the gain according to the formula G = 40k/RG. The external resistor RG should be a precision resistor with a low temperature coefficient. An external RG affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors. Gain accuracy is determined by the tolerance of the external RG and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the temperature coefficient of RG and the drift of the internal resistors (-50ppm/°C typ).



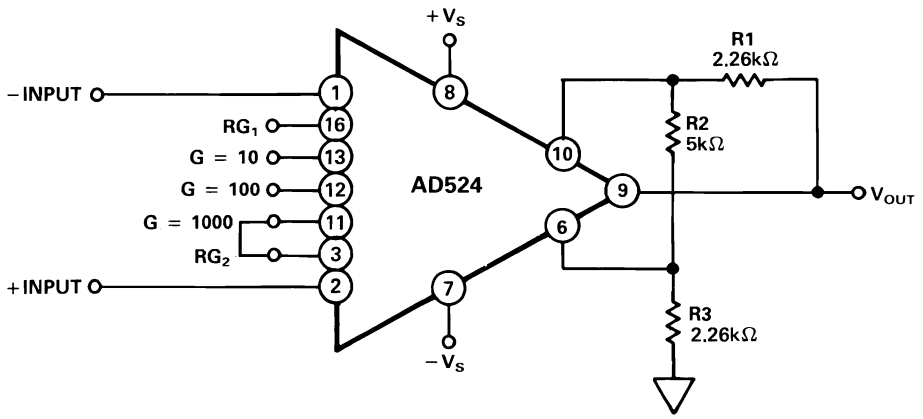
OPERATING CONNECTIONS FOR G = 20

The second technique uses the internal resistors in parallel with an external resistor. This technique minimizes the gain adjustment range and reduces the effects of temperature coefficient sensitivity.



OPERATING CONNECTIONS FOR G = 20, LOW GAIN T.C. TECHNIQUE

The AD524 may also be configured to provide gain in the output stage. The figure shows an H pad attenuator connected to the reference and sense lines of the AD524. R1, R2 and R3 should be made as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

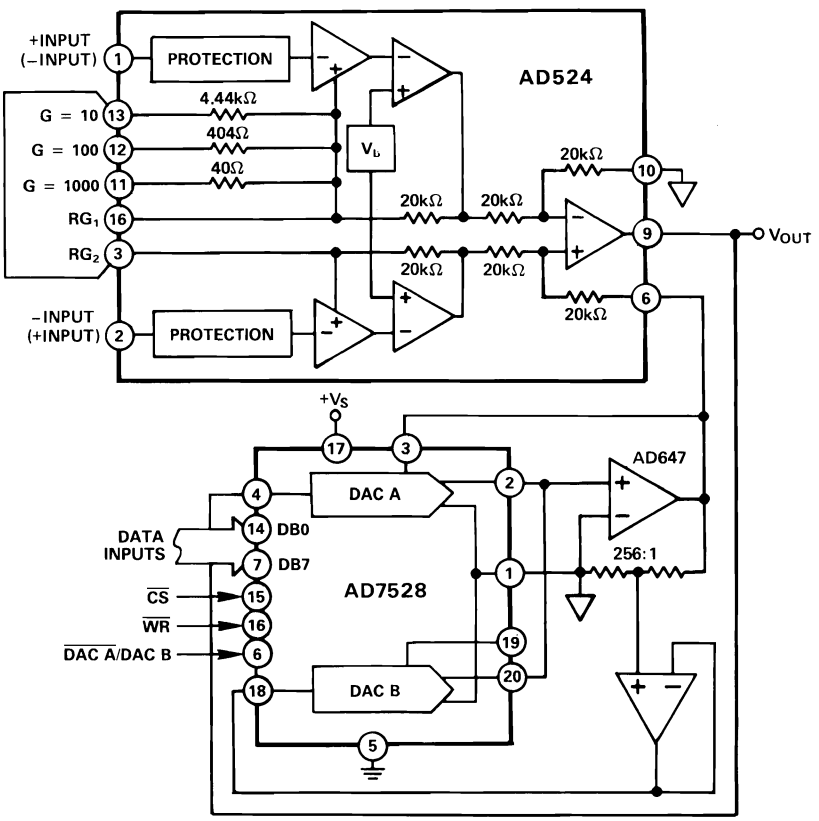


GAIN OF 2000

OUTPUT GAIN RESISTOR VALUES

OUTPUT GAIN	R2	R1, R3	NOMINAL GAIN
2	5kΩ	2.26kΩ	2.02
5	2.05kΩ	1.05kΩ	5.01
10	1kΩ	4.42kΩ	10.1

Another method to develop gain in the output amplifier is to use an active attenuator. The active attenuator presents a very low impedance to the sense and reference inputs, therefore, minimizing the degradation common-mode rejection. The AD7528 which acts essentially as switched resistive attenuators having high analog linearity and symetrical bipolar transmission are ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to a fine adjust (DAC B).



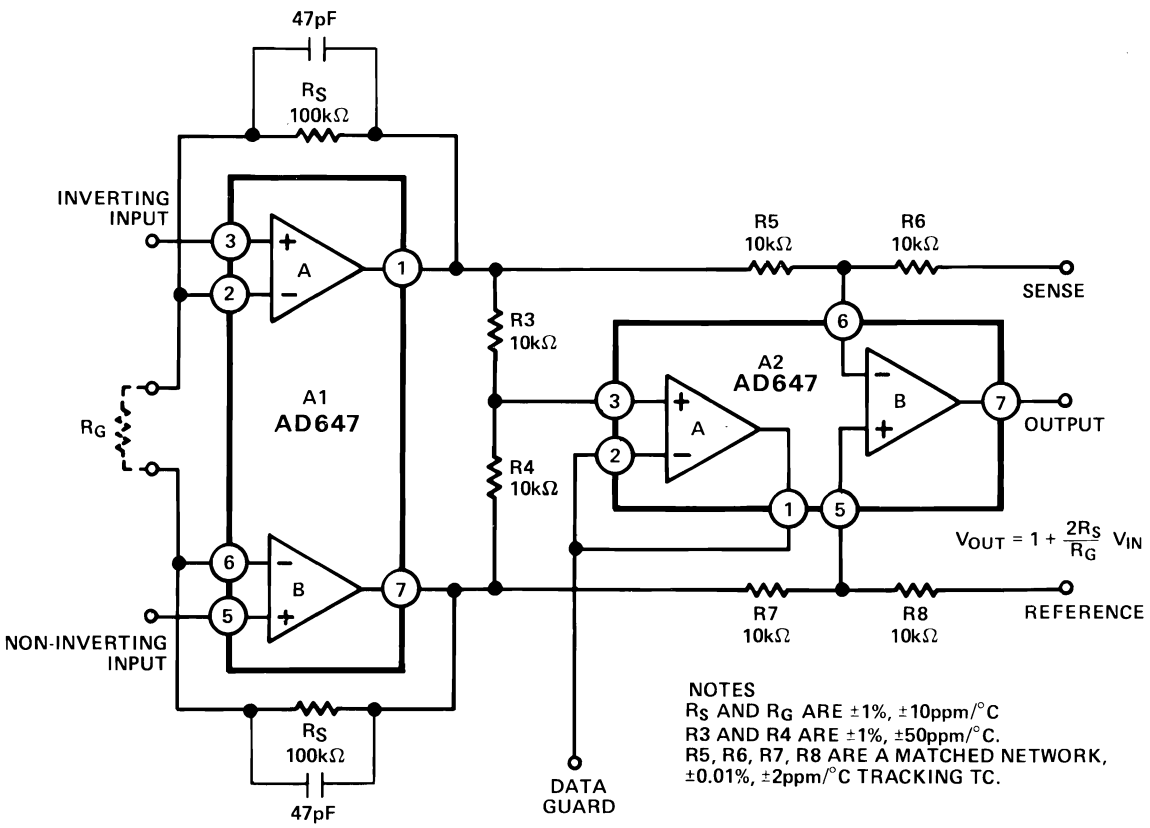
GAIN PROGRAMMING USING A DAC

DISCRETE INSTRUMENTATION AMPLIFIERS

Various forms of instrumentation amplifiers can be constructed using discrete operational amplifiers. The advantage of a discrete instrumentation amplifier is flexibility in design such as using FET input amplifiers for low bias currents or fast, precision amplifiers for wideband instrumentation amps. The disadvantage is that careful component selection is required.

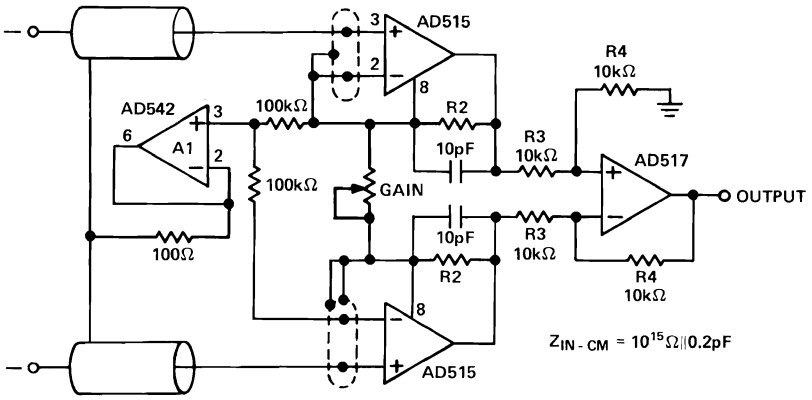
The "classic" 3 op amp instrumentation amplifier can be implemented using 2 dual FET input amplifiers for applications requiring low bias currents. In this application the matching characteristics of the two amplifiers are critical to ensure high performance. The use of an AD647L as the input amplifier A1, guarantees a maximum input offset voltage of 250μV, input offset voltage drift of 2.5μV/°C and bias currents of 35pA. The AD644 may be substituted for higher speed but the higher open-loop gain of the AD647 maintains higher linearity with high closed loop gains. A2 serves two less critical functions in the amplifier and, therefore, can be an AD647J. Amplifier A of A2 is an active data guard which increases ac CMRR and minimizes extraneous signal pickup and leakage. Amplifier B of A2 is the output amplifier of the instrumentation amplifier.

The external resistor characteristics are very critical to achieve the precision available from the AD647Ls in this configuration. Therefore, a great deal of care should be taken when selecting the resistors. CMRR will depend on the matching of resistors R5, R6, R7 and R8. For example a resistor mismatch of 0.1% results in a CMR of 66dB and 0.01% will yield a 86dB CMR. The gain drift and CMR over temperature is directly affected by the matching TC of the resistors used, therefore, a matched resistor network which tracks to ±2ppm/°C should be used.



PRECISION FET INPUT INSTRUMENTATION AMPLIFIER

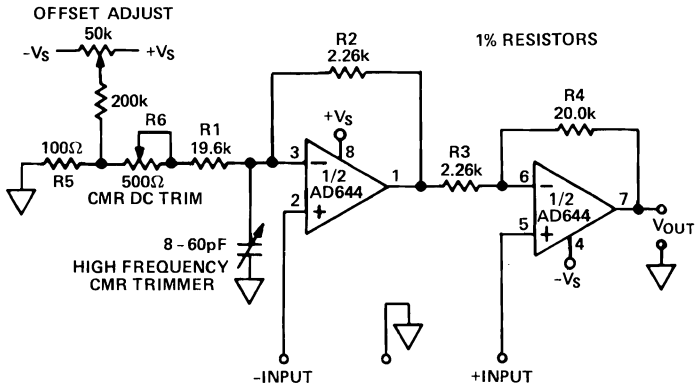
If even lower bias currents are required then an AD515L with 0.075pA bias currents should be used. The AD515 also delivers laser-trimmed offset voltage, low drift, low noise and low power.



(ALL RESISTORS OF SAME NUMBER SHOULD BE MATCHED ±0.1%)
(BUFFER A1 BOOSTS COMMON MODE Z_{IN} BY DRIVING CABLE SHIELDS AT COMMON MODE VOLTAGE AND NEUTRALIZING CM CAPACITANCE)

VERY HIGH IMPEDANCE INSTRUMENTATION AMPLIFIER

A two amplifier instrument amplifier built with an AD644 can provide high accuracy signal conditioning with high frequency input signals. The circuit will achieve an offset voltage drift of 10μV/°C, CMRR of 80dB over the range of dc to 10kHz and a bandwidth of 200kHz (-3dB) at 1V p-p output. The circuit can be configured for a gain range of 2 to 1000 with a typical nonlinearity of 0.01% at a gain of 10.



$$V_{OUT} = \left[\left(\frac{R_4}{R_3} + 1\right)\left(+V_{IN} + V_{OS2}\right) - \left(-V_{IN} + V_{OS1}\right)\left(\frac{R_4}{R_3}\right)\left(\frac{R_2}{R_1} + 1\right)\right]$$

INSTRUMENTATION AMPLIFIER WITH GAIN OF TEN

WIDE BANDWIDTH INSTRUMENTATION AMPLIFIER

4. ISOLATION AMPLIFIERS

Instrumentation amplifiers are restricted by the requirement that a return path for input bias currents must be provided. Furthermore, large common-mode voltages can damage IA input circuitry. When the application involves galvanic or ohmic isolation of input and output circuitry, an Isolation Amplifier is required.

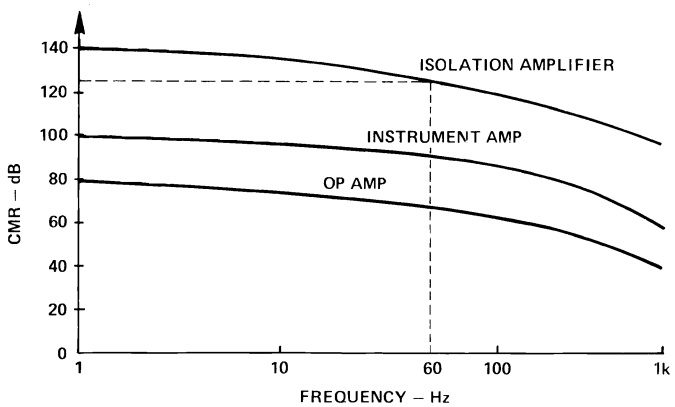
WHEN AN ISOLATION AMPLIFIER IS REQUIRED

- Measure Low Level Signals in the Presence of High CMV.
- Eliminate Measurement Errors Caused by Disturbances on the Source Ground Network (from High Current Transients, etc.)
- Avoid Ground Loops and Their Attendant Pickup Problems. (No Need to Provide a Return Path for Bias Currents.)
- Protect Processing Circuitry from Damage from Large CMV Levels at Both Input and Output.
- Provide Patient-Safe Interface.

Ohmic and Galvanic Source Isolation

The isolation amplifier's floating input design provides complete decoupling between the source and amplifier output and power terminals. This offers other benefits beyond the high common-mode rejection.

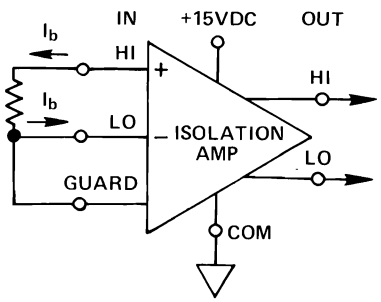
Low capacitance and leakage from input to common gives very high CMR virtually independent of source imbalance.



TYPICAL CMR VS FREQ WITH 1kΩ SOURCE IMBALANCE FOR VARIOUS TYPES OF DEVICES

No Bias Current

The front end circuitry of isolation amplifiers is fully floating and, therefore, no net bias current flows in the input leads. As shown below, the bias current of the LO input is supplied by the HI input. Thus, the isolator does not require connections to the source ground in order to establish the input bias current flow and, therefore, is not affected by disturbances on the source ground system.



ISOLATORS REQUIRE NO NET BIAS CURRENT

SELECTING AN ISOLATOR

Isolation amplifiers may be used to advantage in a limitless number of situations, but the vast majority of applications fall into one of three categories: Medical, Industrial (process control) and Instrumentation (data acquisition).

Medical

Medical amplifiers must first and foremost protect the patient from leakage currents and amplifier fault currents in excess of 10 microamps rms. It is just as important to be sure that the amplifier will not be damaged by a 5kV defibrillator pulses; if an amplifier monitoring a patient's heartbeat should fail during defibrillation, the medical team may continue to defibrillate the patient in the belief that the heart has not re-started (while, in fact, it is the amplifier that has failed). Continued defibrillation can kill the patient.

Industrial

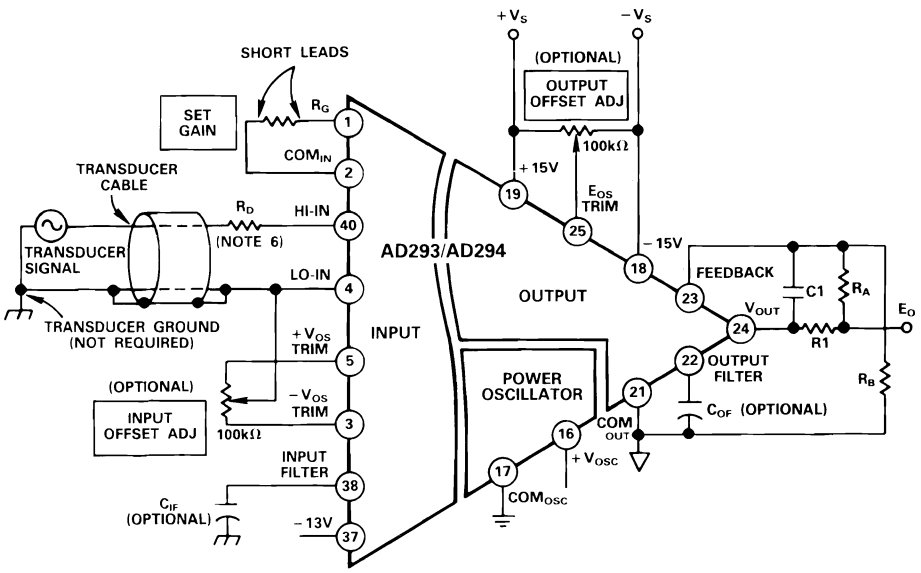
Industrial amplifiers must provide accurate signal gain while rejecting common-mode noise and eliminating ground loops. Industrial malfunctions may cause power-line voltages to be imposed on low-voltage signal lines. The industrial isolator should not be destroyed by such mistreatment, but more important, it must protect the expensive computer on the other end of the line from errant high voltage surges.

Instrumentation

Instrumentation (data acquisition) applications may not involve the extreme hazards of medical or industrial applications, but the precision required may demand the features of an isolator. Twelve bit systems require accuracies of ±0.01% and are therefore quite susceptible to ground loops or common-mode interference. Isolation amplifiers can eliminate ground loops and offer better common-mode rejection than conventional data amplifiers.

AD293/AD294 FEATURES

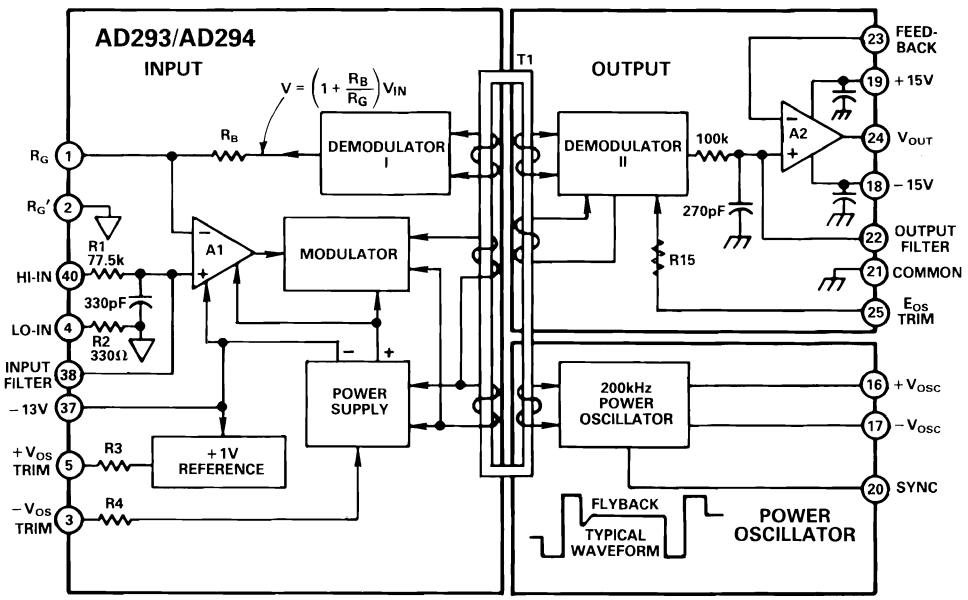
High Common-Mode Voltage:
AD293 ±2500V Peak
AD294 ±8000V Peak
Nonlinearity: ±0.05% max
Adjustable Input & Output Gain: 1V/V to 1000V/V
Meets UL STD 544 Leakage: 2.0μA max @ 115V ac, 60Hz



AD293/AD294 CONNECTION DIAGRAM

Design

The AD293/AD294 isolation amplifier is divided into three isolated sections—input, output, and power-coupled together by a single transformer. A power oscillator (which may be powered by system power or a separate power source) furnishes isolated power to the input amplifier, plus a carrier, which is modulated by the amplified input signal, coupled across the isolation barrier to the output section, demodulated, and buffer-amplified by a system-powered output amplifier.



SIMPLIFIED BLOCK DIAGRAM OF THE AD293/AD294

5. TRANSDUCERS INTERFACING

Ideally, a transducer should have a high level output, zero source impedance, low noise and be relatively linear, however they are not. Through the previous portion of this section we've characterized instrumentation and isolation amplifiers, in this portion we'll outline 2 techniques for measuring physical phenomina. The emphasis will be on solutions to problems.

COMMON TRANSDUCERS SUMMARIZED

TEMPERATURE

TYPE	ELECTRICAL I/O CHARACTERISTICS	COMMENTS
Thermocouples	Low source impedance, typically 10Ω. Voltage-output devices. Output shift is 10's of microvolts/°C. Outputs typically in the millivolts at room temperature.	Low voltage output requires low-drift signal conditioning. Small size and wide temperature range are advantages. Requires reference to a known temperature. Nonlinear response.
Platinum and other RTD's	Resistance changes with temperature. Positive temperature coefficient. Typical impedance (0°C) 20Ω to 2kΩ. Typical sensitivities 0.1%/°C to 0.66%/°C, depending on material.	Highly repeatable. Good linearity over wide ranges. Requires bridge or other network for typical interface.
Thermistors	Resistance changes with temperature. Negative temperature coefficient. Typical impedances (25°C) of 50Ω to 1MΩ available. Sensitivity at 25°C is about 4%/°C. Linearized networks available with with 0.4%/°C sensitivity.	Highest sensitivity among common temperature transducers. Inherently nonlinear (exponential function) but accurate linearized networks available.
Semiconductor sensors	Voltage, current, or resistance functions. Voltage types (diodes) require excitation current. Current types (AD590) require excitation voltage. Resistive types (bulk silicon) may use either type of excitation.	Many devices are uncalibrated and require significant signal conditioning. AD590 is calibrated, linear, and requires minimal signal conditioning.

FORCE

TYPE	ELECTRICAL I/O CHARACTERISTICS	COMMENTS
Strain gages (metal)	Resistance shifts with applied strain. Almost always used in bridge configuration. Typical impedance levels of 120Ω and 350Ω. Typical change is 0.1% over the whole range.	Resistance change with strain small compared to initial value of device resistance. Requires high-quality low-level signal conditioning.
Strain-gage bridge, load cell	Voltage output with applied strain. Requires excitation potential or current to drive the bridge. Typical excitation is from 5 to 15 volts.	Small voltage outputs require low-drift signal conditioning with good common-mode rejection to achieve any degree degree of precision. Output is linear.

FORCE
(Continued)

TYPE	ELECTRICAL I/O CHARACTERISTICS	COMMENTS
Semiconductor strain gages	Bridge types are assembled from individual gages and have a voltage output. Bridge requires excitation, typically 5V to 15V.	More output than metal strain gages, but with increased nonlinearity and sensitivity to temperature.
Piezoelectrics	True charge output device. Modeled as voltage source in series with capacitor. Physical input change produces corresponding charge change. AC and transient response only. Typical upper frequency limit is 20 to 50kHz. Typical output is 10^{-7} coulombs full-scale.	Requires low-bias-current charge amplifier configurations for signal conditioning. Responds to ac signals only.

PRESSURE

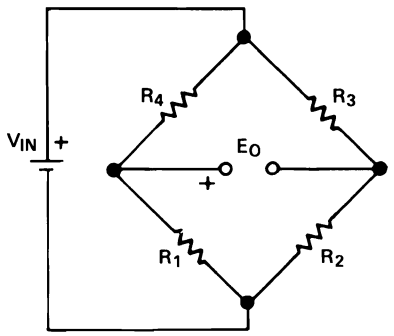
TYPE	ELECTRICAL I/O CHARACTERISTICS	COMMENTS
Rheostat/potentiometer	Resistance or ratio-of-resistance output. Requires voltage or current excitation. Typical impedance 500Ω to 5kΩ.	High-level easy-to-condition outputs are typical due to significant resistance or ratio
Strain gage	Resistance shift (single gage) or voltage output (strain-gage bridge). Requires excitation potential or current.	Small resistance change. Low-level signal requires good signal-conditioning amplifiers.

FLOW

TYPE	ELECTRICAL I/O CHARACTERISTICS	COMMENTS
Pressure-based	See PRESSURE transducers	Pressure types measure flow by measuring ΔP between static and flow-caused pressure, or pressure drop across a constriction. Differential pressure transducers are used to avoid common-mode pressure errors. Response is nonlinear.
Frequency-output types: paddle wheels, rotary types, vortex types	Digital output derived from frequency output are common. Optical or magnetic pickups provide non-invasive measurements. Photocell has 100Ω to 100MΩ on-to-off ratio. Magnetic employs switching or open-collector transistor.	Some types are directly logic-level compatible. Others require impedance and/or voltage amplification, level-shift, and buffering before signal is usable.

Bridge Circuits

The figure shows the common Wheatstone bridge (actually developed by S. H. Christie in 1833). In its simplest form, a bridge consists of four two-terminal elements connected to form a quadrilateral, a source of excitation (voltage or current)—connected along one of the diagonals, and a detector of voltage or current—comprising the other diagonal. The detector, in effect, measures the difference between the outputs of two potentiometric dividers connected across the excitation supply.



$$E_O = \frac{R_1}{R_1+R_4} V_{IN} - \frac{R_2}{R_2+R_3} V_{IN}$$

$$= \frac{\frac{R_1}{R_4} - \frac{R_2}{R_3}}{\left(1+\frac{R_1}{R_4}\right)\left(1+\frac{R_2}{R_3}\right)} V_{IN}$$

AT BALANCE, $E_O = 0$ IF $\frac{R_1}{R_4} = \frac{R_2}{R_3}$

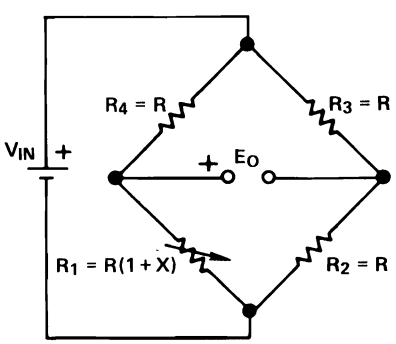
BASIC BRIDGE CIRCUIT—VOLTAGE EXCITATION AND VOLTAGE READOUT

A bridge measures an electrical property of a circuit element indirectly, ie., by comparison against a similar element. The two principal ways of operating a bridge are as a null detector and as a device that reads a difference directly in voltage or current.

When $R_1/R_4 = R_2/R_3$, the resistance bridge shown in the Figure is at a *null*, irrespective of the mode of excitation (current or voltage, ac or dc), the magnitude of excitation, the mode of readout (current or voltage), or the impednace of the detector. Therefore, if the ratio R_2/R_3 is fixed at K, a null is achieved when $R_1 = K R_4$. If R_1 is unknown and R_4 is an accurately determined variable resistance, the magnitude of R_1 can be found by adjusting R_4 until null is achieved. Conversely, in transducer-type measurements, R_4 may be a fixed reference and a null occurs when the magnitude of the measurand is such that R_1 is equal to $K R_4$.

Null-type measurements are principally used in feedback systems, involving electromechanical and/or human elements. Such systems, as noted in the previous chapter, seek to force the active element (strain gage, RTD, thermistor, mechanically coupled potentiometer) to balance the bridge by influencing the parameter being measured. Because the null is independent of the excitation, the null mode may also be used to discriminate between the two polarities of ouptut, i.e., as a *comparator*. In such applications, the *polarity* of the off-null signal might be of greater significance than its *magnitude* (for example, if the level of a tank is below a preset value, a valve is caused to open to fill the tank.

For the majority of transducer applications employing bridges, the *deviation* of one or more resistors in a bridge from an initial value must be measured as an indication of the magnitude (or a change) of the measurand. The figure shows a bridge with all resistances nominally equal; but one of them (R_1) is variable by a factor, (1 + X), where X is a fractional deviation around zero, as a function of (say) strain. As the equation indicates, the relationship between the bridge output and X is not linear, but for small ranges of X it is sufficiently linear for many purposes. For example, if V_{IN} = 10V, and the maximum value of X is ±0.002, the output of the bridge will be linear to within 0.1% for a range of outputs from 0 to ±5mV, and to 1% for the range 0 to ±50mV (±0.02 range for X).



$$E_O = \frac{R(1+X)}{R+R(1+X)} V_{IN} - \frac{1}{2} V_{IN}$$

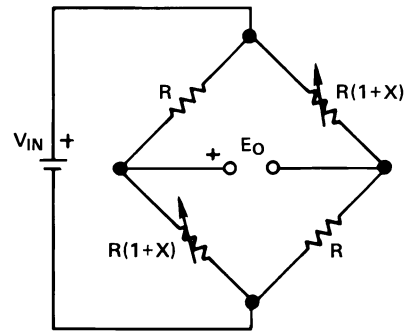
$$= \frac{2+2X-2-X}{2(2+X)} V_{IN}$$

$$= \frac{V_{IN}}{4} \cdot \frac{X}{1+\frac{X}{2}}$$

$$\cong \frac{V_{IN}}{4} X \text{ FOR } X \ll 1$$

BRIDGE USED TO READ DEVIATION OF A SINGLE VARIABLE ELEMENT

The *sensitivity* of a bridge is the ratio-to-the-excitation-voltage of the maximum expected change in the value of the output; in the examples given in the last paragraph, the sensitivities are ±500μV/V and ±5mV/V. The sensitivity can be doubled if two identical variable elements can be used, e.g., at positions R_3 and R_1, as shown in the figure. An example of such a pair is two identically oriented strain-gage resistances aligned in a single pattern. Note that the output is doubled, but the same degree of nonlinearity exists.



$$E_O = \left[\frac{R(1+X)}{R+R(1+X)} - \frac{R}{R+R(1+X)}\right] V_{IN}$$

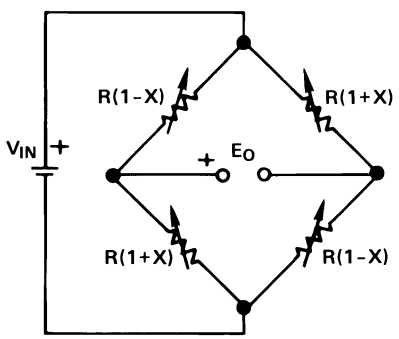
$$= \frac{X}{2+X} V_{IN}$$

$$= \frac{\frac{V_{IN}}{2} \cdot \frac{X}{2}}{1+\frac{X}{2}}$$

$$\cong \frac{V_{IN}}{2} X \text{ FOR } X \ll 1$$

BRIDGE WITH TWO VARIABLE ELEMENTS

In special cases, another doubling of the output can be achieved. The figure shows a bridge consisting of four resistors, two of which increases and two of which decrease in the same ratio. Two identical two-element strain gages, attached to opposite faces of a thin carrier to measure its bending, could be electrically configured in this way. The output of such a bridge would be four times the output for a single-element bridge; furthermore, the complementary nature of the resistance changes would result in a *linear* output.



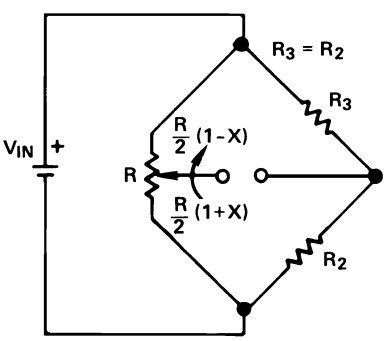
$$E_O = \left[\frac{R(1+X)}{2R} - \frac{R(1-X)}{2R}\right] V_{IN}$$

$$= \left[\frac{1+X-1+X}{2}\right] V_{IN}$$

$$= X\, V_{IN}$$

ALL ELEMENTS VARIABLE

The figure shows a bridge employing a zero-centred potentiometer to constitute two adjacent arms; the position of the potentiometer is a measure of the physical phenomenon. Since it is a 2-variable-element version of the output is twice that of the single-element bridge, and it is linear.



$$E_O = \left[\frac{\frac{R}{2}(1-X)}{R} - \frac{1}{2}\right] V_{IN}$$

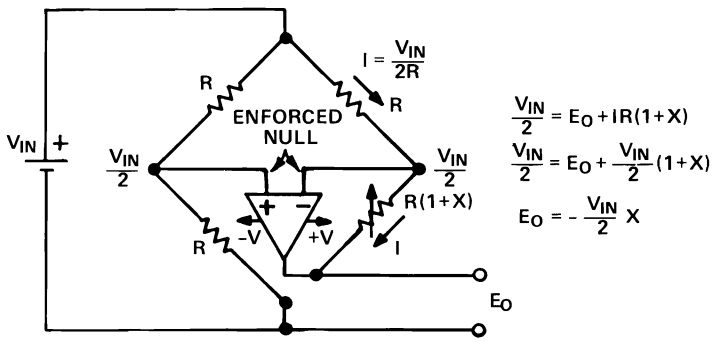
$$= \frac{R-XR-R}{2R} V_{IN}$$

$$= \frac{V_{IN}}{2} X$$

LINEAR POTENTIOMETER AS VARIABLE ARM

A distinction should be recognized between the linearity of the bridge equation and linearity of the transducer response to the phenomenon being sensed. For example, if the active element is a potentiometer, a bridge used to implement the measurement would be adequately linear; yet the output could still be nonlinear due to the pot's nonlinearity.

Manufacturers of transducers employing bridges address the nonlinearity issue in a variety of ways, including keeping the resistive swings in the bridge small, shaping complementary nonlinear response into the active elements of the bridge, using resistive trims for first-order corrections, and a variety of proprietary magical techniques. A bridge can, of course, be linearized by making it less sensitive (e.g., by making the initial ratios, R_4/R_1 and R_3/R_2, large), but the tradeoff of sensitivity for linearity is painful.

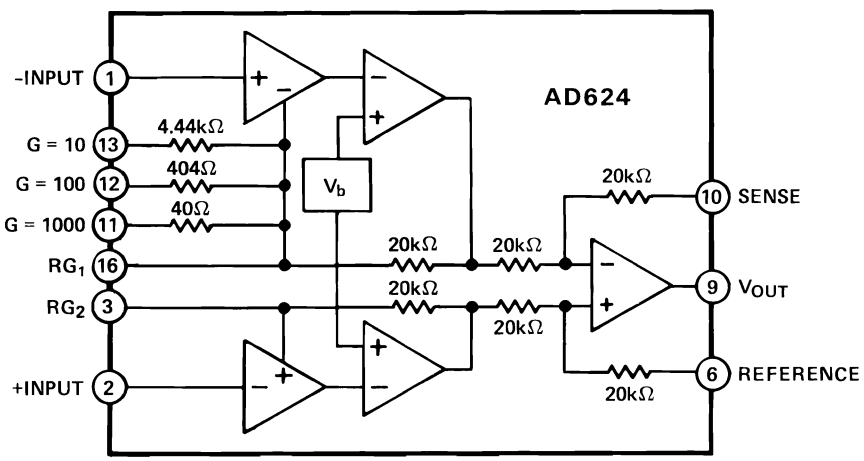


ACTIVE BRIDGE

The figure shows an active bridge in which an op amp produces a null by adding a voltage in series with the variable arm. That voltage is equal in magnitude and opposite in polarity to the incremental voltage across R_X, and it is inherently linear with X. Since it is an op-amp output, it can be used as a low-impedance output point for the bridge measurement. This active bridge has a gain of two over the standard one-active-element bridge, and the output is linear, even for very large values of X.

AD624 FEATURES

Low Nonlinearity: 0.002% (G = 1)
High CMRR: 130dB (G = 1000)
Low Offset Voltage: 50μV
Low Offset Voltage Drift: 0.25μV/°C
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 10, 100, 1000
No External Components Required
Internally Compensated
Low Noise: 0.2μV p-p



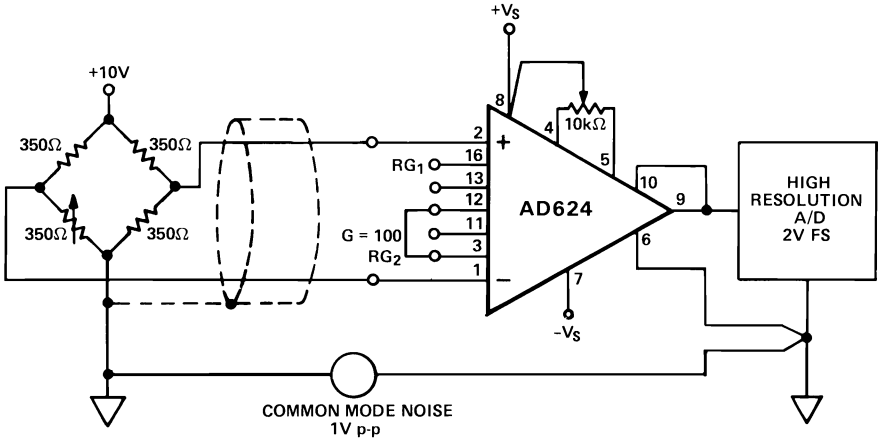
AD624 FUNCTIONAL BLOCK DIAGRAM

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD624 is required to amplify the output of an unbalanced transducer.

The figure shows a differential transducer, unbalanced by 100Ω, supplying a 0 to 20mV signal to an AD624. The output of the IA feeds a high resolution A to D converter with a 2.0 volt input voltage range. There is 1 volt of peak-to-peak 0 to 10Hz noise on the ground return appearing as a common-mode signal at the inputs of the IA. The operating temperature range is 0 to +70°C, the change in temperature (ΔT) is 70°C - 25°C = 45°C. The AD624 initial calibration is performed at 25°C for both gain and offsets.

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (51ppm = 0.005%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.005%.



TYPICAL BRIDGE APPLICATION

AD624 ERROR ANALYSIS

Error Source	AD624L Specifications	Calculation	Initial Effects on Accuracy	Reducible Effects on Accuracy	Irreducible Effects on Accuracy
Gain Error	±0.1%	±0.1% = 1000ppm	1000ppm	1000ppm	–
Gain Instability	10ppm/°C	(10ppm/°C)(45°C) = 450ppm	–	450ppm	–
Gain Nonlinearity	±0.003%	±0.003% = 30ppm	–	–	30ppm
Input Offset Voltage	±50μV, RTI	±50μV/20mV = ±2500ppm	2500ppm	2500ppm	–
Input Offset Voltage Drift	±0.25μV/°C	(±0.25μV/°C)(45°C) = 11.25μV 11.25μV/20mV = 562.5ppm	–	562.5ppm	–
Output Offset Voltage	±1.0mV	±1.0mV/2V = 500ppm	500ppm	500ppm	–
Output Offset Voltage Drift	±20μV/°C	(±20μV/°C)(45°C) = 900μV 900μV/2V = 450ppm	–	450ppm	–
Bias Current – Source Imbalance Error	±10nA	(±10nA)(100Ω) = 1μV 1μV/20mV = 50ppm	50ppm	50ppm	–
Bias Current – Source Imbalance Drift	±100pA/°C	(100ppm/°C)(100Ω)(45°C) = 0.45μV 0.45μV/20mV = 22.5ppm	–	22.5ppm	–
Offset Current – Source Imbalance Error	±10nA	(±10nA)(100Ω) = 1μV 1μV/20mV = 50ppm	50ppm	50ppm	–
Offset Current – Source Imbalance Drift	±100pA/°C	(100pA/°C)(100Ω)(45°C) = 0.45μV 0.45μV/20mV = 22.5ppm	–	22.5ppm	–
Offset Current – Source Resistance – Error	±10nA	(10nA)(175Ω) = 3.5μV 3.5μV/20mV = 87.5ppm	87.5ppm	87.5ppm	–
Offset Current – Source Resistance – Drift	±100pA/°C	(100pA/°C)(175Ω)(45°C) = 0.78μV 0.78μV/20mV = 39ppm	–	39ppm	–
Common Mode Rejection 5Vdc	120dB	120dB = 1ppm × 5V = 5μV = 250ppm	250ppm	250ppm	–
Common Mode Rejection	120dB	120dB = 1ppm × 10V = 1μV = 50ppm	–	–	50ppm
Noise, RTI (0.1 – 10Hz)	0.2μV p-p	0.2μV p-p/20mV = 10ppm	–	–	10ppm
Noise, RTO (0.1 – 10Hz)	20μV p-p	20μV p-p/2V = 10ppm	–	–	10ppm
		Total Errors	44375ppm	5984ppm	101ppm

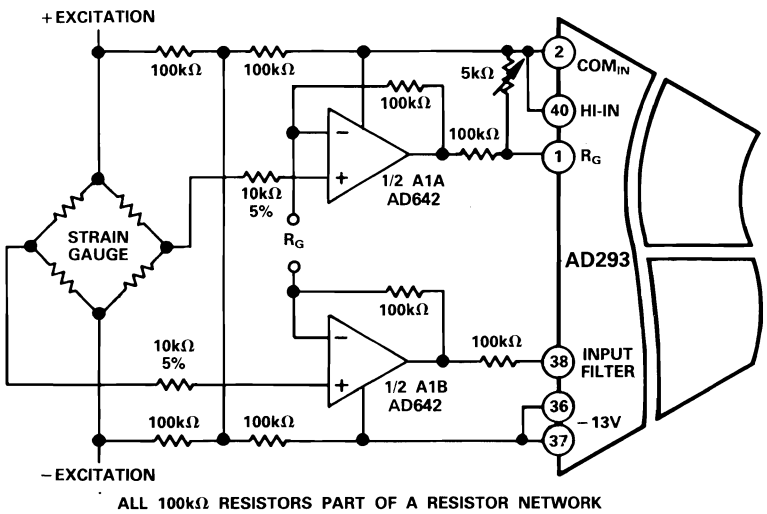
The preceding table lists all applicable error sources and their corresponding effects on accuracy. Initial errors are defined as those errors that can be reduced to a negligible amount by performing an initial calibration.

Reducible errors include these initial errors along with other errors that occur during normal operation that may be corrected by an adaptive or "intelligent" system. For example, changes in gain or offset may be measured during an auto-zero/auto-gain cycle by measuring two known voltages (a precision reference and ground, for example).

Irreducible errors are errors which can not be readily corrected either at initial calibration or in use.

ISOLATED INDUSTRIAL APPLICATIONS

As illustrated in the figure, the AD293 can be applied where differential signal sources are used such as an isolated strain gauge. With a third wire connected to the common mode potential of that source, a common mode current is forced to flow through the third wire and through the isolation barrier; thus, sparing the differential input wires the necessity of conducting the common mode current. In this manner, the isolator is responsive to only the differential inputs while ignoring the passage of common mode currents. Input gain is selected via RG and determined by the input gain formula.



ISOLATED STRAIN GAUGE USING FRONT END OF AD293

BRIDGE LINEARIZATION

If one arm of Wheatstone bridge varies from its nominal value by a factor, (1 + 2w), the voltage or current output of the bridge will be (with appropriate polarities and scale factors):

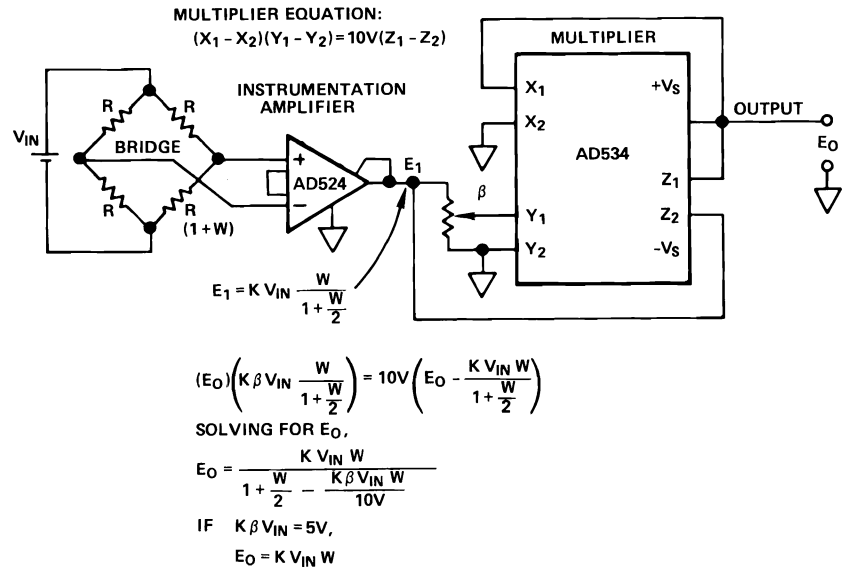
$$y = \frac{w}{1 + w}$$

Linear response requires very small values of w (to make the denominator essentially independent of w) and, as a consequence, preamplification.

The circuit shown enables large-deviation bridges to be used without losing linearity or resorting to high attenuation. The circuit computes the inverse of the bridge function, i.e.,

$$w = \frac{y}{1 - y}$$

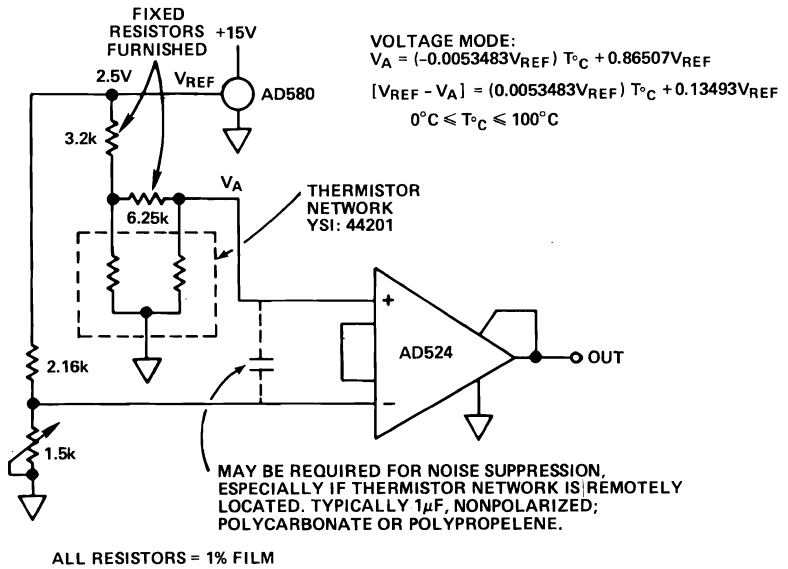
Depending on which arm of the bridge varies, it may be necessary to reverse the polarity of the X connections. Any resistive, linearly responding transducer (one or more legs of the bridge proportional to the phenomenon being measured) may profit from the application of this circuit. Examples include position servos, linear thermistors, platinum-resistance-wire sensors, pressure transducers and strain gages.



BRIDGE LINEARIZATION USING ANALOG MULTIPLIER

THERMISTOR INTERFACE

In the figure, a thermistor is used in the potentiometric mode. Both the sensor and the offset network are supplied by a 2.5V reference. The differential of the voltages is read out by an instrumentation amplifier, which may be connected for the desired gain and output configuration.



INSTRUMENTING LINEARIZED THERMISTORS – VOLTAGE MODE

THERMOCOUPLE APPLICATIONS

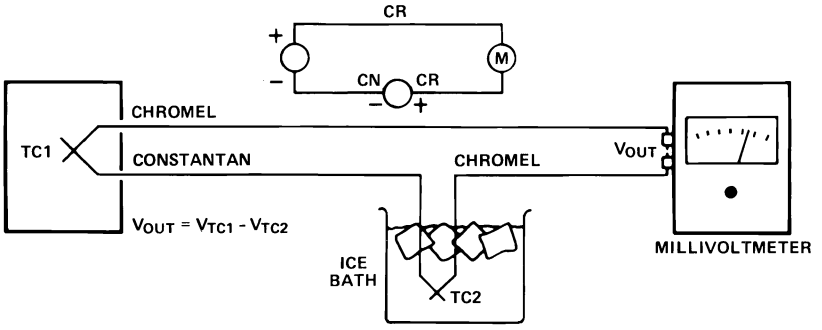
Thermocouples are economical and rugged; they have reasonably good long-term stability. Because of their small size, they respond quickly and are good choices where fast response is important. They function over temperature ranges from cryogenics to jet-engine exhaust and have reasonable linearity and accuracy.

Because the number of free electrons in a piece of metal depends on both temperature and composition of the metal, two pieces of dissimilar metal in isothermal contact will exhibit a potential difference that is a repeatable function of temperature. In general, these voltages are small. The table 1 lists a number of standard thermocouples, their useful temperature range, and the voltage swing over that range; it can be seen that the average change of voltage with temperature ranges from 7 to about 75μV/°C.

SOME COMMON THERMOCOUPLES

Junction Materials	Typical Useful Temp Range (°C)	Voltage Swing Over Range (mV)	ANSI Designation
Platinum-6% Rhodium – Platinum-30% Rhodium	38 to 1800	13.6	B
Tungsten-5% Rhenium – Tungsten-26% Rhenium	0 to 2300	37.0	(C)
Chromel – Constantan	0 to 982	75.0	E
Iron – Constantan	-184 to 760	50.0	J
Chromel – Alumel	-184 to 1260	56.0	K
Platinum – Platinum-13% Rhodium	0 to 1593	18.7	R
Platinum – Platinum-10% Rhodium	0 to 1538	16.0	S
Copper – Constantan	-184 to 400	26.0	T

Since *every pair* of dissimilar metals in contact constitutes a thermocouple (including copper/solder, about 3μV/°C and Kovar/rhodium), and since a useful electrical circuit requires at least two contacts in series, measurements with thermocouples must be implemented in a manner which minimizes undesired contributions of incidental thermocouples and provides a suitable reference.



SIMPLE TEMPERATURE MEASURING CIRCUIT USING AN ICE BATH AT THE REFERENCE JUNCTION. THERMOCOUPLE MEASUREMENTS ARE INHERENTLY DIFFERENTIAL.

Because thermocouples are low-level devices, signal conditioning is not a trivial matter. The millivolt-level signals call for low-drift relatively expensive electronics if resolutions better than 1°C are required. Linearity in many types is poor, but the relationships are predictable and repeatable, so either analog or digital techniques can be used for linearizing downstream.

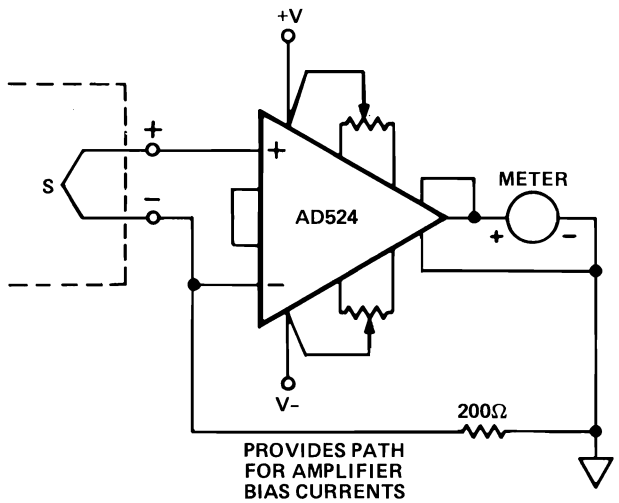
Providing a suitable temperature reference and minimizing the effects of unwanted thermocouples may prove challenging. Techniques include physical references (ice-point cells at +0.01°C, which are accurate and easy to construct but unwieldy to maintain); ambient-temperature reference junctions (acceptable so long as the ambient temperature range in the vicinity of the reference junction is smaller than the desired resolution of the temperature being measured); and electronic cold-junction compensators, which provide an artificial reference level and compensate for ambient temperature variations in the vicinity of the reference junction (this technique requires careful attention to both the electronics and the physical configuration at that location).

AMBIENT-REFERENCED THERMOCOUPLES

As we have noted, thermocouples require cold-junction compensation if they must resolve temperature changes with precision better than the ambient temperature range at the cold junction. However, for high-temperature measurements to within a few percent, the cold junction may often be profitably left at room ambient.

Suppose, for example, that a Type S thermocouple is used to measure temperatures of the order of 1500°C within a furnace, and the ambient temperature of the cold junction is 25°C ±15°C. Since the sensitivity of the thermocouple is 12μV/°C at 1500°C, and a change from 10°C to 40°C at the cold junction produces a change of 180μV in the net output voltage, the equivalent ΔT at the active junction is 15°C for a full-scale change at the cold junction, or 1% of 1500°C.

In the figure, an instrumentation amplifier is used to reject common-mode noise. If there is no conductive return path from the thermocouple, resistance may be used (as shown) to provide a path for the amplifier's bias currents.



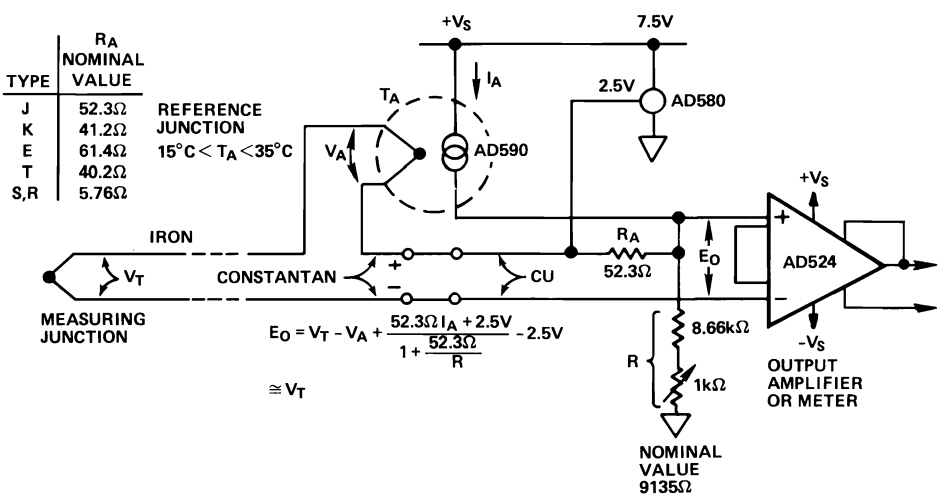
THERMOCOUPLE PREAMPLIFIER USING AD524

COLD-JUNCTION COMPENSATION

If ambient temperature variation of the cold junction can cause significant error in the output of a thermocouple pair, there are two alternatives: maintain the cold junction at constant temperature, by some such technique as an ice bath or a thermostatically controlled oven, or subtract a voltage that is equal to the voltage developed across the cold junction at any temperature in the expected ambient ambient range.

The figure shows a simple application, in which the variation of the cold-junction voltage of a Type J thermocouple—iron(+)—constantan—is compensated for by a voltage developed in series by the temperature-sensitive output current of an AD590 semiconductor temperature sensor.

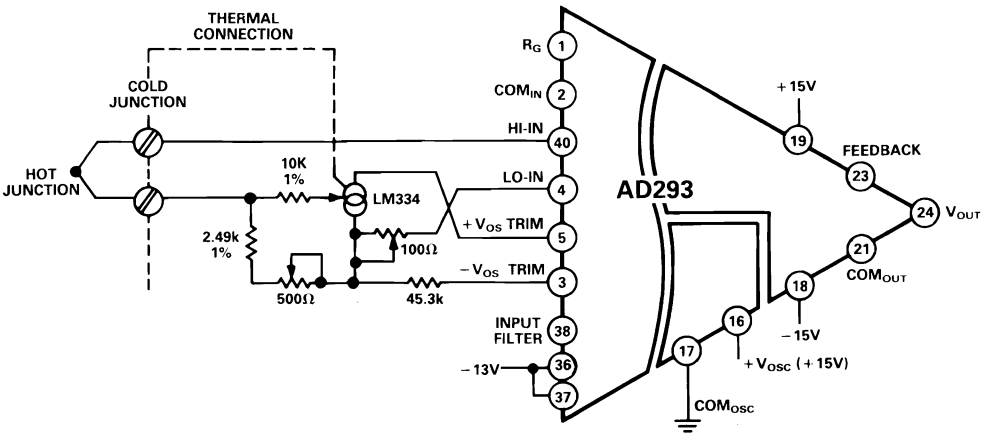
The circuit is calibrated by adjusting R_T for proper output voltage with the measuring junction at a known reference temperature and the circuit near 25°C. If resistors with low tempcos are used, compensation accuracy will be to within ±0.5°C, for temperatures between +15°C and +35°C. Other thermocouple types may be accommodated with the standard resistance values shown in the table. For other ranges of ambient temperature, the equation in the figure may be solved for the optimum values of R_T and R_A. If an instrumentation amplifier is used, gain and offset specifications should be appropriate for the temperatures being measured, the required precision, and the sensitivity of the thermocouples employed.



COLD-JUNCTION COMPENSATION

ISOLATED TEMPERATURE MEASUREMENT AND COLD JUNCTION COMPENSATION

The AD293 can be used for isolated temperature measurements while providing cold junction compensation. With the circuitry connected as shown, the LM344 must be thermally connected to the cold junction terminal for an accurate temperature measurement to be made of this terminal. The 500Ω potentiometer will set the gain accuracy while the 100Ω potentiometer establishes offset trimming. Using this configuration, accurate temperature measurements of the industry's popular J type thermocouple can be made with the AD293 providing the added isolation feature.



ISOLATED TEMPERATURE MEASUREMENT
& COLD JUNCTION COMPENSATION

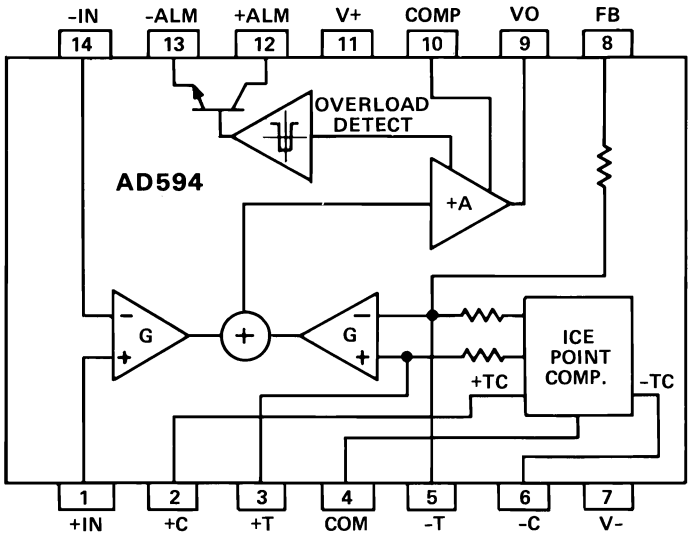
6. MONOLITHIC COLD JUNCTION COMPENSATION CIRCUIT

AD594 FEATURES

- Low Impedance Voltage Output 10mV/°C
- Internal Ice Point Compensation
- Wide Power Supply Range: +5V to ±15V
- Low Power: 1mW
- Thermocouple Failure Alarm
- Laser Wafer Trimmed to 1°C Calibration Accuracy
- Set Point Mode Operation
- Self Contained Centigrade Thermometer Operation
- High Impedance Differential Input

The AD594 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a pre-calibrated amplifier to produce a high level (10mV/°C) output directly from a thermocouple signal. Pin strapping options allow it to be configured as a linear amplifier-compensator or as a switched output set point controller using either fixed or remote set point control. It can be configured to directly amplify its compensation voltage, thereby converting it to a standalone centigrade temperature transducer with a low impedance voltage output.

The AD594 includes a Thermocouple Failure Alarm which indicates if one or both thermocouple leads become open. The alarm output has a flexible format which includes TTL drive capability.



AD594 FUNCTIONAL BLOCK DIAGRAM

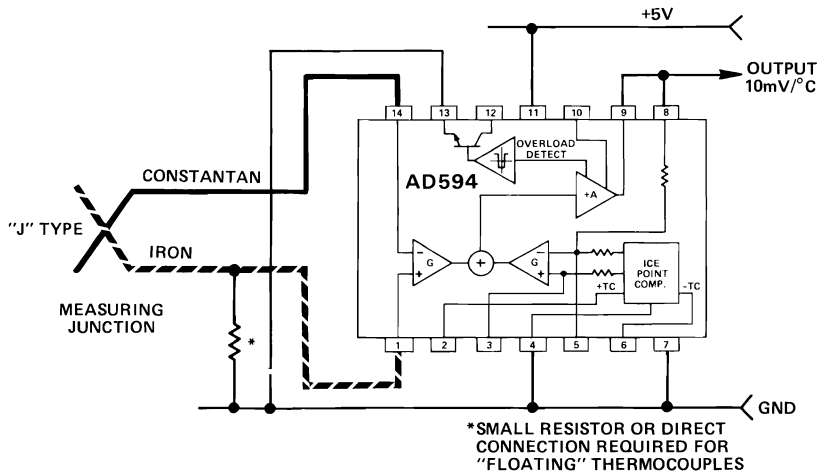
The AD594 behaves like two differential amplifiers, the outputs of which are summed and used to control a high gain amplifier, as shown in the block diagram. In normal operation, the main amplifier output, at pin 9, is connected to the feedback network, at pin 8. Thermocouple signals applied to the floating input stage, at pins 1 and 14, are amplified by gain G of the differential amplifier and then are further amplified by A in the main amplifier. The output of the main amplifier is fed back to a second differential stage in an inverting connection. The feedback signal is amplified by this stage and is also applied to the main amplifier input by way of the summing circuit. Because of the inversion, the amplifier feedback signal is effectively subtracted from the amplified thermocouple input signal. The high gain of the main amplifier will cause the feedback to be driven to reduce this difference signal to a small value.

The two differential amplifiers are made to match and have identical gains, G. As a result, the feedback signal which must be applied to the right hand differential amplifier will very precisely match the thermocouple input signal when the difference signal has been reduced to zero. The high gain, A, of the main amplifier assures a small difference, so that the feedback network must be driven to produce a replica of the thermocouple input signal at the right hand differential stage. The feedback network is trimmed so that the effective gain to the output, at pins 8 and 9, results in a voltage of 10mV/degree of thermocouple excitation.

In addition to the feedback signal, a cold junction compensation voltage is applied to the right hand differential amplifier. The compensation is a differential voltage proportional to the Celsius temperature of the AD594. This signal disturbs the differential input so that the amplifier output adjusts to restore the input to equal the applied thermocouple voltage.

The compensation is applied through the gain scaling resistors so that its effect on the main output is also 10mV/degree. As a result, the compensation voltage adds to the effect of the thermocouple voltage a signal directly proportional to the difference between 0 Celsius and the AD594 temperature. If the thermocouple reference junction is maintained at the AD594 temperature, the output of the AD594 will correspond to the reading which would have been obtained from amplification of a thermocouple referenced to an ice bath.

In order to operate properly the AD594 must have the thermocouple input within both the normal mode signal and common-mode operating range. A normally connected thermocouple within the common-mode operating range will meet these requirements. If one or both thermocouple input terminals are opened, however, an amplifier overload will result. The AD594 includes an input overload detector which switches on an alarm "transistor". This "transistor" is actually a current limited output buffer, but can be used, up to the limit, as a switch transistor for either pull-up or pull-down operation of external alarms.

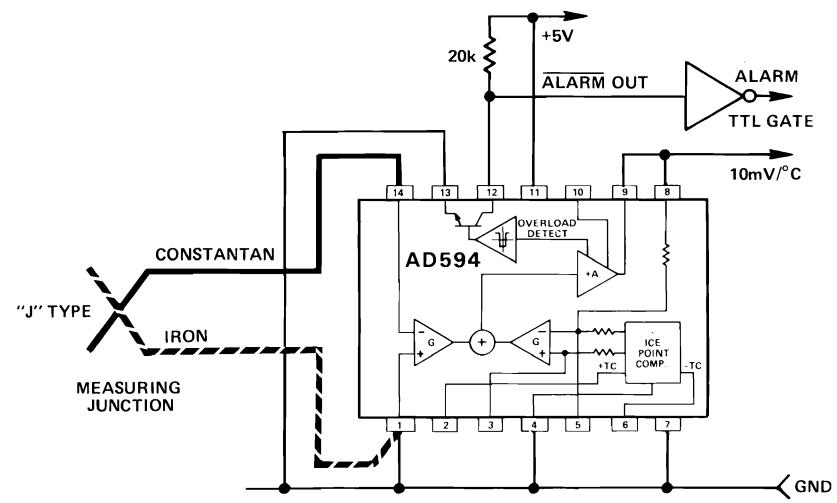


BASIC AD594 CONNECTIONS
SINGLE SUPPLY-POSITIVE TEMPERATURE

The AD594 is completely self contained with the interconnections shown in the figure will provide a direct output from type J thermocouples measuring from 0 to +300°C. The measuring thermocouple wires connect to pins 1 and 14 of the AD594, either directly or through intervening connections. The connections at which the thermocouple wires terminate forms the reference junction. This junction should be kept at the same temperature as the AD594 since this is the junction compensated by the ice point reference in the AD594. If the thermocouple is not directly connected to pins 1 and 14, the intervening connections must both be made of the same material.

In this single supply application the V- connection at pin 7 is strapped to power and signal common, pin 4. When the alarm is unused, pin 13 must connect to either pin 4 or pin 7 (common or V-). The positive 5 volt supply connects to pin 11. Any convenient supply voltage from +5 to +30 volts may be used, however, the lower the supply voltage the lower will be the power consumption. It is important to minimize power consumption so that self heating of the circuit can be neglected.

The output can be taken from pin 9. The pre-calibrated feedback network which connects to pin 8 is strapped to the output to provide a 10mV/°C nominal output scale.



USING THE AD524 ALARM OUTPUT

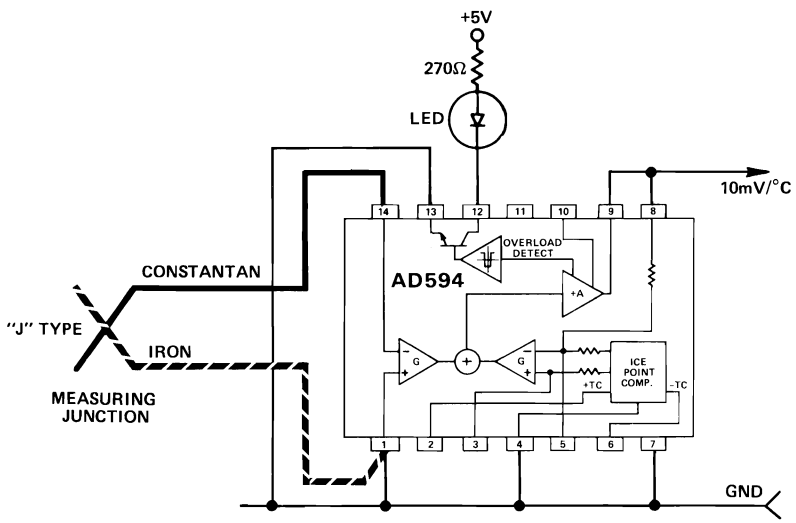
In all applications of the AD594 the -ALM connection, pin 13, should be constrained so that it is not more positive than (V+) -4V. This can be most easily achieved by connecting pin 13 to either common on pin 4 or V- on pin 7. For most applications which use the alarm signal, pin 13 will be "grounded"

to pin 4 and the signal will be taken from +ALM on pin 12. In this configuration the alarm transistor will be off in normal operation and the 20k pull up will cause the +ALM output on pin 12 to go high. If one or both of the thermocouple leads are interrupted, the +ALM will be driven low. As shown, the signal is compatible with the input of a TTL gate which can be used as a buffer and/or inverter.

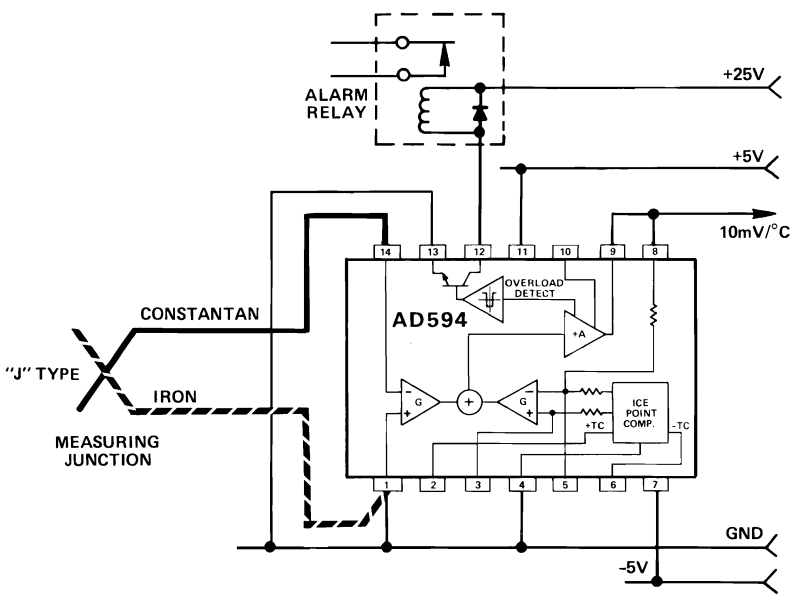
Since the alarm is a high level output it maybe used to directly drive an LED or other indicator. The 270Ω resistor will limit current in the LED to about 10mA. The resistor may be omitted, since the alarm output transistor is current limited to about 20mA. In this case, however, the transistor will operate in a high dissipation mode. As a result, the temperature of the circuit will rise well above ambient and the cold junction compensation will be affected. This will create a problem only if normal operation is required to resume immediately after recovery from an alarm condition.

Whenever the alarm circuit is activated, some self heating should be anticipated. The time required for the chip to return to ambient temperature will, of course, depend on the power dissipation of the alarm circuit, the nature of the thermal path to the environment, and for short intervals the alarm duration.

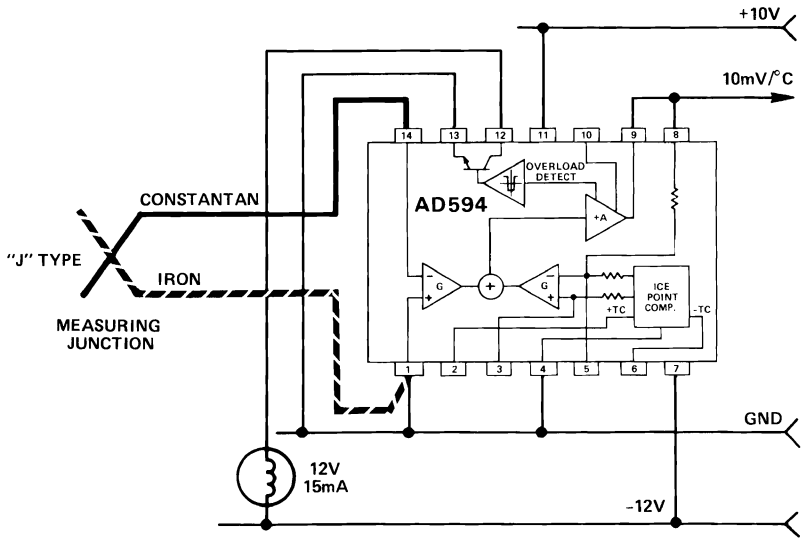
The alarm can be used with both single and dual supplies. It can be operated above or below ground. The "collector" and "emitter" of the output "transistor" can be used in any of normal switch configuration. The collector (+ALM) should not be allowed to become more positive than the V- voltage plus 36V, however, it may be permitted to be more positive than V+. The emitter (-ALM) voltage should be constrained so that it does not become more positive than 4 volts below the V+ which is applied to the circuit, to insure normal operation.



LED INDICATOR

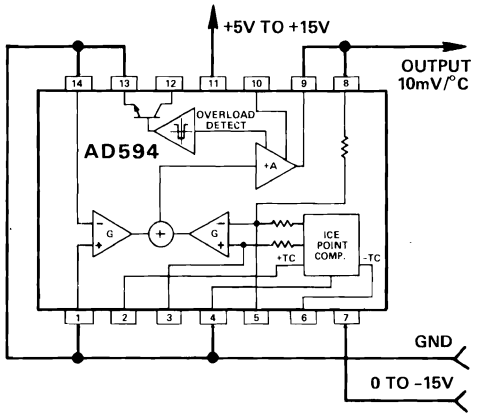


ALARM RETURNED TO THIRD SUPPLY VOLTAGE



-ALM DRIVES NEGATIVE REFERENCED LOAD

The AD594, contains a temperature reference which is internally offset to zero Celsius for use as cold junction compensation for a thermocouple. Without the thermocouple attached, this reference indicates the temperature of the IC and the self-contained fixed-gain amplifier can be made to scale up this signal for a 10mV/°C output. This arrangement as shown is a three-terminal (voltage output) temperature sensor referred to zero. Note that if negative temperature indications are desired, a negative supply should be connected to pin 7 of the device.



AD594 AS A STAND-ALONE CENTIGRADE THERMOMETER

Section III

Analog Computational Circuits

Analog Computational Devices

1. Analog Data Processing
2. Logarithmic Properties of Silicon Junction Devices
3. Multiplier/Dividers
   - Design Techniques
   - Practical IC Multiplier/Dividers
   - Applying Variable-Transconductance IC Multiplier/Dividers
4. Dedicated Computational Circuits
   - rms-dc Converters

1. ANALOG DATA PROCESSING

In this age of the digital computer, there is a growing tendency to rely on digital intelligence to process information. There are many instances, however, when such computational power is unnecessary, inefficient or even inadequate for performance of particular measurement or control functions.

ANALOG PROCESSING SHOULD BE USED WHEN DIGITAL PROCESSING IS:

- Unnecessary
- Inefficient
- Inadequate

Digital signal processing in a real-world environment entails the use of A to D and D to A converters, extensive digital hardware and software and, perhaps, costly displays. In many instances, such involvement is extravagant.

DIGITAL PROCESSING IS UNNECESSARY WHEN:

- Simple Human Control is Available
- Minimal Amounts of Data are to be Processed
- Display Accuracies of 1 to 5% are Adequate

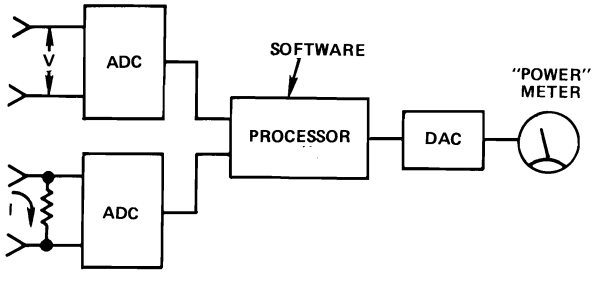
Cases where digital processing is unnecessary are numerous. Automotive applications, such as fuel gage readouts and engine monitoring, are typical.

DIGITAL PROCESSING IS INEFFICIENT WHEN

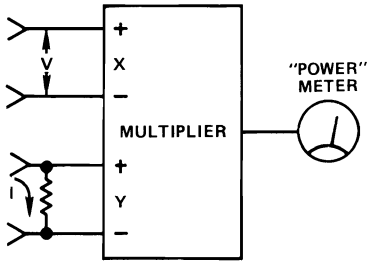
- Limited Amounts of Data are to be Processed
- Digital Hardware is not in the System and Analog Processing Components are Available
- 1 to 5% Accuracies are Adequate
- A Large Dynamic Signal Range is Involved
- Complex or Transcendental Functions Must be Performed

Even small systems may have a requirement for storing and processing vast quantities of data. Complex decision-making tasks based on many data inputs will usually demand some form of digital intelligence and memory, but in small systems, cost and size limitations prevent unlimited expansion of these capabilities.

An example of wasted digital capacity might be a simple power monitor. To convert voltage and current into the format required by a digital processor would require two analog-to-digital converters. Forming the V X I product requires memory, machine time and software. A digital readout or a digital-to-analog converter and a meter will be necessary to display the results. A simple analog multiplier and an inexpensive meter will perform the same task in a more direct and cost-effective manner. If calibration is required, a simple adjustment will replace a software change thus permitting interchangeability.



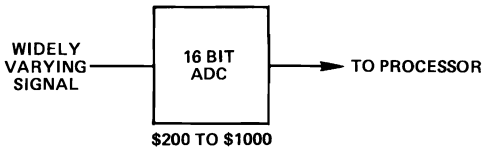
DIGITAL POWER MONITOR



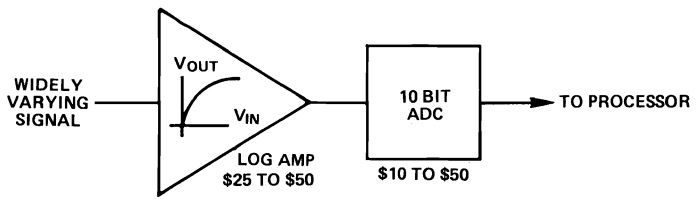
ANALOG POWER MONITOR

Another common example of efficient use of analog data processing involves signal measurement over a wide dynamic range.

A 16-bit converter has 65,536 codes and can thus produce an output resolvable to 96dB. But a 16-bit ADC can cost $1000. Six decades of log conversion, as supplied accurately by most logarithmic amplifiers, can provide 120dB of dynamic range for less than $100.



ALL-DIGITAL, HIGH DYNAMIC RANGE MEASUREMENT



ANALOG/DIGITAL HIGH DYNAMIC RANGE MEASUREMENT

When a complex arithmetic or transcendental function is to be performed, digital signal processing is often considerably less efficient than equivalent analog computation. This is particularly true of functions which are digitally evaluated using series expansions. While a microprocessor may consume precious execution time computing a logarithm, analog computational devices can unload a central processor and perform such operations in real time.

Other applications where analog signal conditioning techniques may improve system efficiency by reducing digital capacity requirements are listed below. While many of these functions can be implemented in the digital domain, analog processing may be better suited to overall system requirements.

PROCESSING TASKS THAT CAN BE PERFORMED IN THE ANALOG DOMAIN

- **Modulation**
- **Filtering**
- **Companding**
- **Automatic Gain Control**
- **Root-Mean-Square Calculations**
- **Complex Waveform Generation**
- **Scaling and Calibration**

There are circumstances which dictate the use of analog processing.

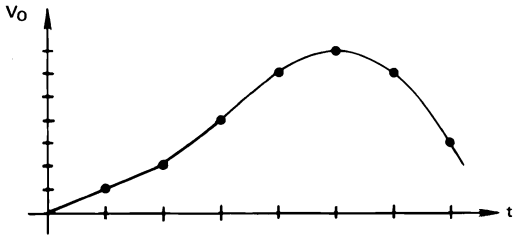
DIGITAL PROCESSING IS INADEQUATE WHEN:

- **Real-World Signal Acquisition is the Problem**
- **Continuous Data is Required**
- **Processing Must Be Performed in Real-Time**

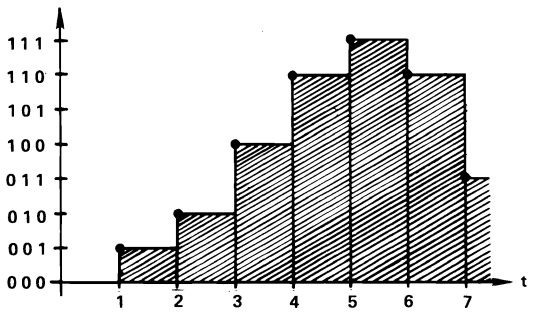
Number-crunching capacity alone can not always solve the problem of extracting small signals from vast quantities of noise. Selective amplification is usually required regardless of how the resulting information is to be processed. This subject is covered in detail in another section of this seminar program.

Digital systems do not process data in real time; data conversion and machine cycle time introduce delays. While the finite bandwidth of a real analog signal conditioning element may limit the processing rate, real-time processing is possible.

Quantized or digitized data exhibits an inherent degree of "coarseness". Even multi-bit converters produce steps and glitches in magnitude and time. Even when high accuracy is not necessary, recognition of small changes may require continuity.



CONTINUOUS ANALOG SIGNAL



MSB	0	0	0	1	1	1	1	0
	0	0	1	0	1	1	1	1
LSB	0	1	0	0	0	1	0	1

QUANTIZED (DIGITIZED) SIGNAL

Most devices that perform analog computation provide a "nonlinear" transfer function. Unfortunately, this characteristic is frequently used to describe the entire class of computational devices. In the minds of those familiar with linear amplifiers and converters, "nonlinear devices" are undesirable, exhibiting an unpredictable input-output relationship. The opposite is true, however; although the input-output transfer function of a computational device is not linear ($V_{OUT} \neq K\ V_{IN}$), it is certainly predictable to a specified degree of accuracy.

2. LOGARITHMIC PROPERTIES OF SILICON JUNCTION DEVICES

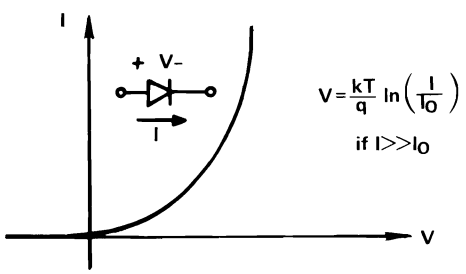
With few exceptions, the operation of computational devices is based on the logarithmic properties of silicon junctions. An "ideal logarithmic diode" has the current-voltage relationship:

AN "IDEAL LOGARITHMIC DIODE" HAS THE CURRENT-VOLTAGE RELATIONSHIP:

$$I = I_O\ (e^{qV/kT} - 1)$$

where:

I is the current through the diode
V Is the voltage across the diode
q is a constant equal to the unit charge, 1.60219×10^{-19} coulombs
k is Bolzmann's constant, 1.38062×10^{-23} joules/°Kelvin
T is the absolute temperature (in °Kelvin)
I_O is the extrapolated current for $E_O = V = 0$ Volts



$$V = \frac{kT}{q} \ln\left(\frac{I}{I_O}\right)$$

if $I >> I_O$

THE DIODE CURVE

Several "rules-of-thumb" are useful to remember when dealing with logarithmic devices. At or near "room temperature", we can assume the following:

DIODE APPROXIMATIONS

$$\frac{kT}{q} = 26\text{mV (exact at 28.58°C)}$$

$$\frac{kT}{q} \ln(10) = 60\text{mV (exact at 29.25°C)}$$

This simplifies the diode expression to:

$$V = 60\text{mV} \log \frac{I}{I_O}$$

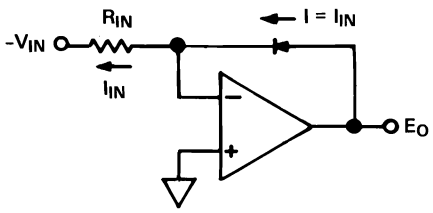
or V increases 60mV every time current increases by a factor of 10

It is also useful to remember that the "constant", $\frac{kT}{q}$, changes approximately 3400 parts per million per degree Celsius (ppm/°C) at +25°C.

$$\frac{d}{dT}\frac{kT}{q} \cong 3400\text{ppm/°C}$$

@ 25°C

Such a diode may be connected in the feedback path of an operational amplifier as shown below.



$$E_O = \frac{kT}{q} \ln\left(\frac{I_{IN}}{I_O}\right) \cong 0.06 \log \frac{V_{IN}}{R_{IN}\, I_O}$$

if $I_{IN} >> I_O$

DIODE LOG AMP

In real circuits, however, performance is not so predictable.

The logarithmic performance of general purpose diodes is limited at the high end by ohmic bulk resistance which produces an additional voltage drop, IR_B. The diode equation then becomes:

$$E_O = \frac{kT}{q} \ln\left(\frac{I}{I_O}\right) + IR_B$$

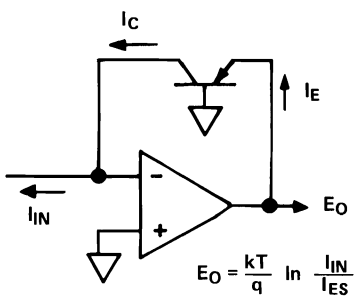
$$\frac{kT}{q} \ln\left(\frac{I}{I_O}\right) + IR_B$$

At the low end, diffusion currents flow in surface inversion layers and generation-recombination effects in space-charge regions will cause a scale factor error, m.

$$E_O = m\frac{kT}{q} \ln\left(\frac{I}{I_O}\right), 1 \leqslant m \leqslant 4.$$

That scale error, m, can vary in magnitude and value of voltage at which m changes (within a family of devices). This makes general-purpose diodes impractical for accurate log operations over more than 1 or 2 decades.

If a grounded-base transistor replaces the diode on the feedback path of the operational amplifier, the following circuit results:



GROUNDED-BASE TRANSISTOR LOG AMP

From the Ebers and Moll equations[1] it can be shown that

$$E_O = \frac{kT}{q} \ln\left(\frac{I_{IN}}{I_{ES}}\right) - \frac{kT}{q} \ln \alpha_N$$

for $I_{IN} >> I_{ES}$

Where I_{ES} is the emitter saturation current
α_N is the forward current-transfer ratio
(not $\alpha = \frac{I_C}{I_E}$ = grounded-base current gain)

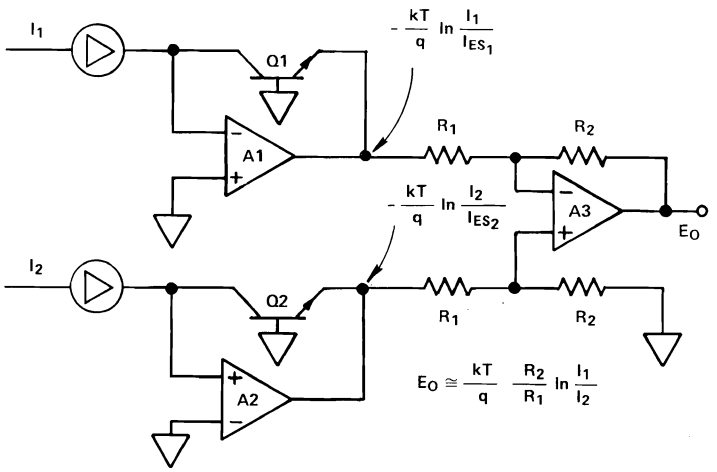
Typically, I_{ES} is in the order of 10^{-13} or less for the silicon planar transistors used for log operations. α_N is nearly unity over a wide range of currents thus minimizing the contribution of the $\frac{kT}{q} \ln \alpha_N$ term, leaving $E_O = \frac{kT}{q} \ln\left(\frac{I_{IN}}{I_{ES}}\right)$.

The major limitation of the simple circuits discussed thus far is their temperature sensitivity; kT/q changes 0.34%/°C in the vicinity of 25°C and αI_{ES} differs from device to device and doubles every 10°C.

For two matched transistors (V_{be} match at constant collector current and temperatures), the αI_{ES} ratio tends to be constant over temperature

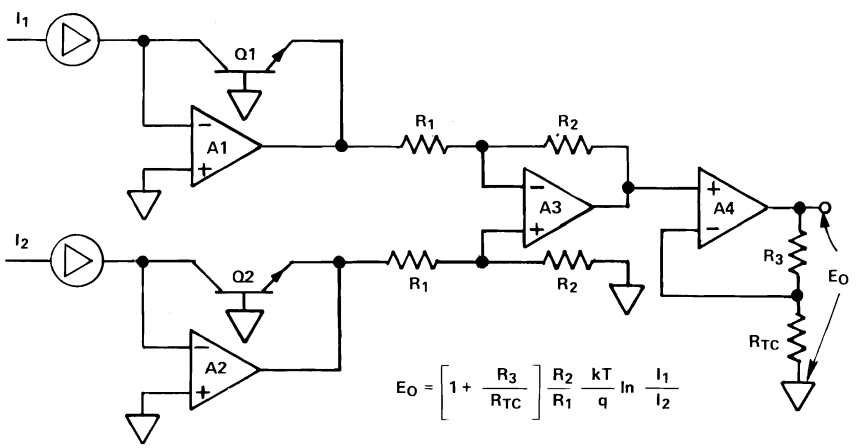
$$\frac{kT}{q} \ln\left(\frac{I_1}{\alpha I_{ES1}}\right) - \frac{kT}{q} \ln\left(\frac{I_2}{\alpha I_{ES2}}\right) = \frac{kT}{q} \ln\left(\frac{I_1}{I_2}\right) + \ln\left(\frac{\alpha I_{ES2}}{\alpha I_{ES1}}\right)$$

The term $\ln\left(\frac{\alpha I_{ES2}}{\alpha I_{ES1}}\right)$ is nearly zero if $\alpha I_{ES_1} \approx \alpha I_{ES_2}$ ($\ln 1 = 0$). A log ratio circuit that performs that cancellation is shown below.



LOG RATIO CIRCUIT WITH TEMPERATURE-COMPENSATED I_{ES}

The last remaining significant error source is the temperature dependence of $\frac{kT}{q}$ which may be cancelled with an equal and opposite temperature as shown below.



LOG RATIO CIRCUIT WITH COMPENSATION FOR BOTH I_{ES} AND kT/q

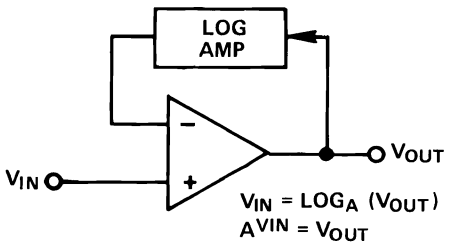
It should be noted that these circuits operate with single-polarity signals.

[1] See "Nonlinear Circuits Handbook", Daniel H. Sheingold, ed, Analog Devices, 1974 for a detailed derivation.

LOG AMPLIFIER APPLICATIONS

- Linear Signal Processing Problems
  - Poor Signal to Noise at Low Levels
  - Saturation at High Levels
- Log Signal Processing
  - Avoid Noise and Saturation
  - Improve Resolution
  - Achieve 10^6 Dynamic Range
- Data Compression & Linearization
  - A to D (11 Bit) & Log Pre-Amp Yields 20 Bit Resolution
  - K_1 Log + K_2 Antilog Yields $I_{IN}^{K1/K2}$
- Absorbance Measurements
  - Blood Analyzers
  - Oxygen Detectors – Pollution Control
  - Colorimetry

The anti-log function is easily implemented with a log amp and a negative feedback amplifier. There are, of course, practical limits on dynamic range with a circuit of this type, but the basic idea of achieving an inverse function by using a functional block as a feedback element is important.



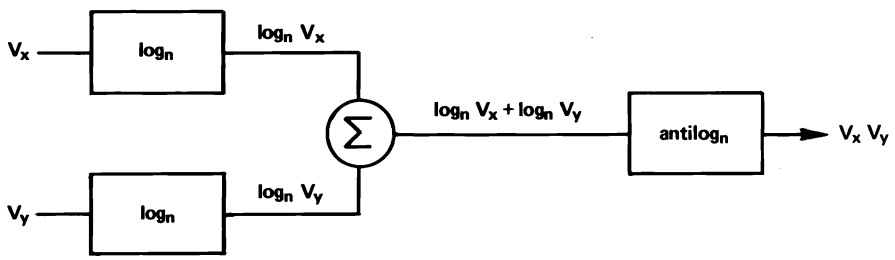
LOG AMP AS FEEDBACK ELEMENT YIELDS ANTI-LOG AMPLIFIER

3. MULTIPLIER/DIVIDERS

The class of devices known as multipliers bears the injustice of a superficially simplified name. These versatile computation elements are indeed capable of performing multiplication of analog inputs, but are in no way restricted to this task alone. By appropriate interconnection, they can be made to divide, root, raise to a power and perform implicit calculations.

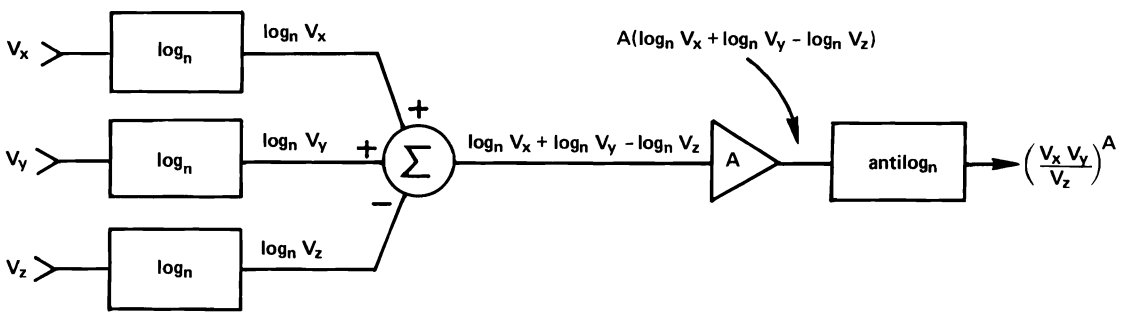
Design Techniques

There are several methods of implementing the multiplication function, the most obvious of which is basically an extension of the log-antilog circuitry discussed previously. If one sums the logs of two quantities and then performs an anti-log operation, the result is the product of the original quantities.



BASIC LOG-ANTILOG MULTIPLIER BLOCK DIAGRAM

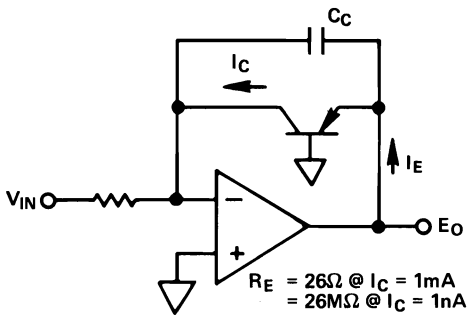
This scheme can be expanded to perform division and raising to a power.



EXPANDED LOG-ANTILOG MULTIPLIER BLOCK DIAGRAM

This technique offers high accuracy, temperature stability, and versatility at the expense of complexity (size and price) and, generally, bandwidth. Errors in the divide mode can be as small as ±0.25% over a 100:1 denominator range.

The bandwidth of a log amplifier is directly related to signal amplitude. This property comes about when one considers the compensation required for a log amp.



LOG AMP COMPENSATION PROBLEM

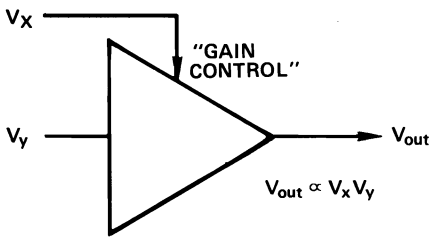
Clearly, a capacitor selected for proper compensation at the high end will yield an extremely low corner frequency at the low end of the range. The problem can be reduced somewhat by adding an external R_E (usually several kΩ) between the amplifier's output and the emitter. This resistance will then be dominant over several decades of signal range and the bandwidth will begin to roll off only at the low end.

Another disadvantage to log-antilog multipliers is the mathematical property that the log of a negative number is undefined. This restricts such multipliers to unipolar signals (one-quadrant operation).

If, however, four-quadrant operation is required, a precision reference and several precision resistors are required. This complicates the circuit to the extent that no complete 4-quadrant log-antilog IC multipliers are presently available.

Variable Transconductance Multipliers

The variable-transconductance technique is the most direct implementation of analog multiplication and is therefore ideally suited to IC technology. One input variable controls the gain (transconductance) of an active device, which amplifies the other input in proportion to the control input.



VARIABLE TRANSCONDUCTANCE (GAIN) MULTIPLIER

Most variable transconductance multipliers use silicon junction transistors as the active elements because of the linear relationship between collector current and transconductance given by the following equation

$$\frac{dI_C}{dV_{be}} = \frac{q}{kT} I_C$$

where

I_C = collector current in amperes

V_{be} = base-emitter voltage, in volts

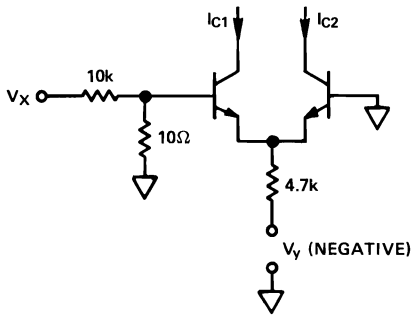
q = unit of electronic charge = 1.60219×10^{-19}

k = Boltzmann's constant = 1.38062×10^{-23}

T = absolute temperature, degrees Kelvin = °C + 273.15°

q/kT = 1/(25.69mV) at 25°C

A simple 1-quadrant variable-transconductance multiplier is shown below:



$$I_{C1} - I_{C2} = \Delta I_C = \frac{q}{kT}\left(\frac{V_y + V_{be}}{4.7 \times 10^3}\right)\left(\frac{10}{10{,}010}\right)V_x$$

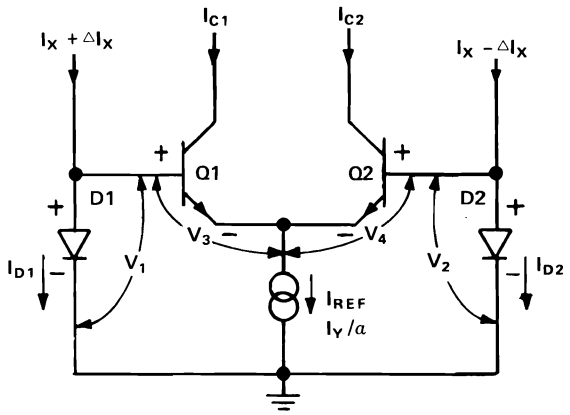
$$= 8.3 \times 10^{-6}\,(V_y + 0.6)\,V_x \;@\; 25°C$$

BASIC TRANSCONDUCTANCE MULTIPLIER CIRCUIT

The practical limitations of this circuit are as follows:

1) The Y input is offset by V_{be} and can only be more negative than V_{be}. Also V_{be} changes nonlinearly with V_y.
2) The scale factor has a temperature coefficient of -0.34%/°C at 25°C.
3) The X input is nonlinear because of the exponential relationship between I_C and V_{be}.

Temperature and linearity errors can be compensated by making use of the logarithmic properties of diodes as in the following circuit:



LINEARIZED 2-QUADRANT MULTIPLIER (PRINCIPLE)

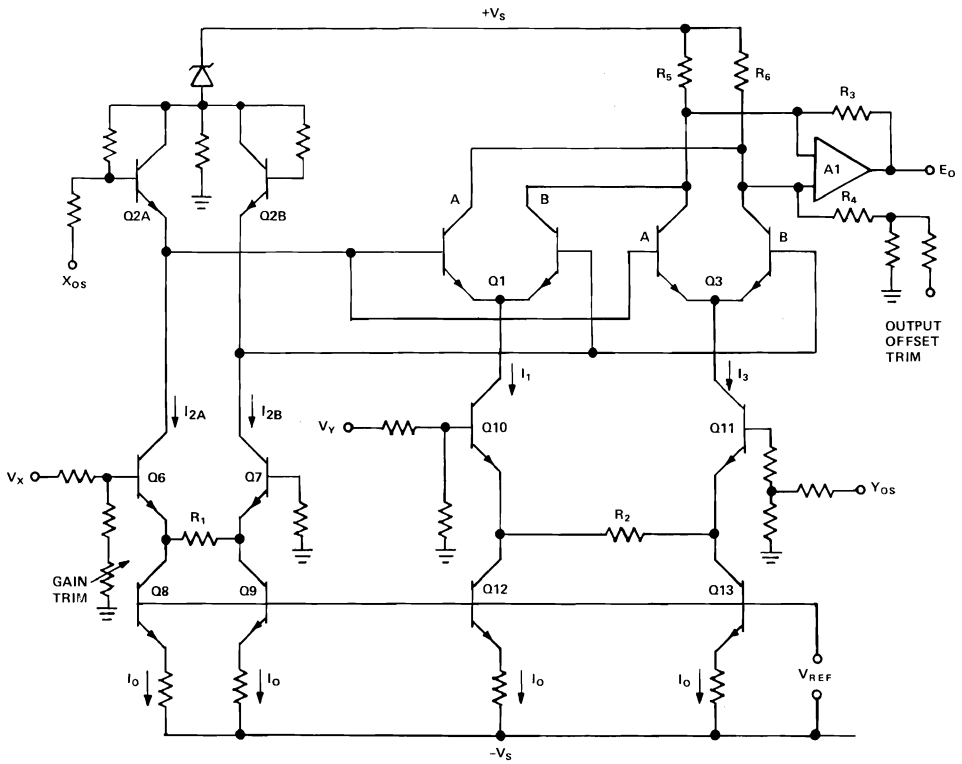
The linear input difference current, ΔI_X, is made into a logarithmically-changing voltage by D1 and D2. This will compensate for exponential relationship of I_C and V_{be}. Furthermore, the $\frac{q}{kT}$ scale factor of the transconductance function will be compensated by the $\frac{kT}{q}$ scale factor of the logarithmic diode response. It can be shown that this results in the transfer function:

$$\Delta I_C = \frac{\Delta I_X \cdot I_y}{2I_X}^{*}$$

This circuit is still incomplete because it requires differential input currents and its output is in the form of a differential current. Furthermore, operation is restricted to two quadrants.

By "cross-coupling" two transconductance cells (Q1 and Q3) and applying differential current sources (Q6, Q7 and Q10, Q11), full 4-quadrant operation is realized.

*For further details see *Nonlinear Circuits Handbook*, Analog Devices, pages 217-221.



4-QUADRANT VARIABLE-TRANSCONDUCTANCE MULTIPLIER

Q2A and Q2B form the linearization "diodes"; A1 converts the differential output current to a single-ended output voltage.

The variable-transconductance multiplier has the following advantages:

ADVANTAGES OF THE VARIABLE-TRANSCONDUCTANCE MULTIPLIER

1) **Good accuracy. Overall errors as small at ±1/4% (AD534L)**
2) **Wide bandwidth. Bandwidths of 10MHz or more can be realized independent of input signal level (unlike log-antilog devices)**
3) **Simplicity (and low cost). This technique may be readily implemented in "discrete" or IC form.**

Practical IC Multiplier/Dividers

Inspection of the above schematic shows that accurate performance requires careful matching of all transistor-pairs. This makes the V-T multiplier ideal for implementation in IC form. However even excellent IC processing tolerances will leave some residual mismatches. In multipliers, the effects of mismatches go beyond dc offsets, in fact, ac inputs may be fed through when an input null is required. DC errors occur due to output amplifier offsets while gain errors may be caused by scaling resistor mismatches.

These errors can appear in log-antilog multipliers as well, since operational amplifiers are used to drive the logging elements.

TRIMMABLE ERRORS IN MULTIPLIERS

X-Input Voltage Offset:	Y Feedthrough
Y-Input Voltage Offset:	X Feedthrough
Z-Input (output amplifier) Voltage Offset:	dc output offset voltage
Resistor Mismatch:	Gain Error

An untrimmed multiplier could exhibit errors as large as ±30%; therefore it is almost always necessary for the user to perform trimming. Due to second-order interactions, some reiteration is often required. An alternative to such a complex trimming procedure is to buy an internally-trimmed multiplier.

Advanced IC technology has made internally-trimmed multipliers available at reasonable cost.

TECHNOLOGY REQUIRED FOR AN INTERNALLY-TRIMMED IC MULTIPLIER

Monolithic Fabrication
Thin-Film SiCr Resistors On-Chip
Laser-Wafer-Trimming
Buried Zener Reference

Applying Variable Transconductance IC Multiplier/Dividers

Although the latest internally-trimmed IC multipliers offer the highest level of performance presently available in IC multipliers, there are situations where other choices may be indicated. The following table compares Analog Devices IC multipliers.

ANALOG DEVICES IC MULTIPLIER/DIVIDERS

AD530	Original Complete IC Multiplier Untrimmed Industry Standard	AD534	Newest Precision IC Multiplier Complete Trimmed Extended Versatility and Performance
AD532	Complete IC Multiplier Trimmed Industry Standard	AD535	Newest IC Divider Complete Trimmed Guaranteed Specs as Divider
AD533	Complete IC Multiplier Untrimmed Very Low Cost		

In order to explore the uses for analog multipliers, we must first become familiar with real devices.

The AD534 is a good example to work with in that it exhibits excellent performance, versatility and trim-free operation. A version trimmed and specified for optimum performance as a divider, the AD535, is also available.

AD534

FEATURES

Pretrimmed to ±0.25% max 4-Quadrant Error
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X100 Gain
Low Noise Design: 90μV rms, 10Hz-10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

APPLICATIONS

High Quality Analog Signal Processing
Differential Ratio and Percentage Computations
Algebraic and Trigonometric Function Synthesis
Wideband, High-Crest rms-to-dc Conversion
Accurate Voltage Controlled Oscillators and Filters

AD535

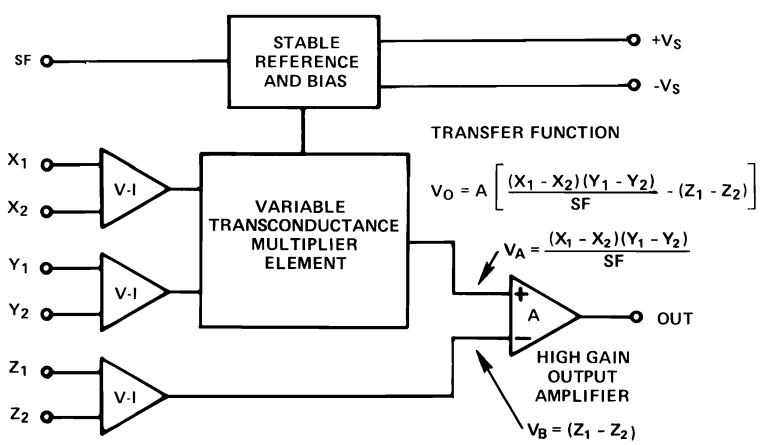
FEATURES

Pretrimmed to ±0.5% max Error, 10:1 Denominato Range
±2.0% max Error, 50:1 Denominator Range
All Inputs (X, Y and Z) Differential
Low Cost, Monolithic Construction

APPLICATIONS

General Analog Signal Processing
Differential Ratio and Percentage Computations
Precision AGC Loops
Square-Rooting

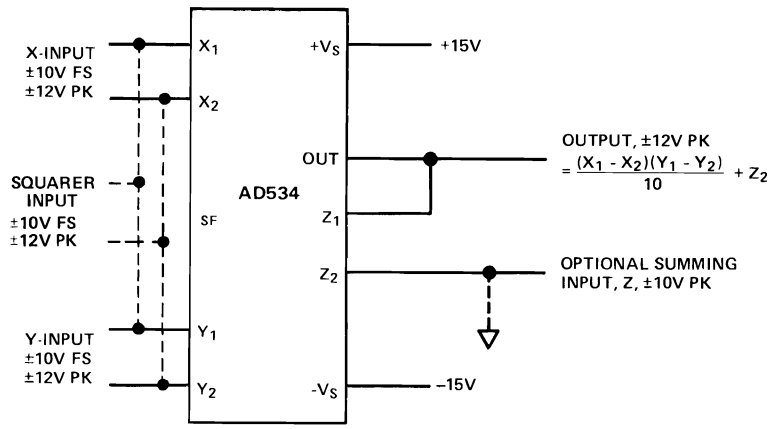
The block diagram for the AD534/5 is shown below:



AD534/5 FUNCTIONAL BLOCK DIAGRAM

This configuration provides differential inputs for the multiplying inputs along with differential access to the output amplifier. The scale factor, while trimmed to 10 during manufacture, can be adjusted for values between 3 and 10. Input offset (feedthrough) and output offset are laser-trimmed at the wafer level thus eliminating a major source of user inconvenience.

The figure below shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.



BASIC MULTIPLIER CONNECTION

Squaring is performed by tying the inputs common. The common input signal is then multiplied by itself. Typically, errors are about half those realized as an $\frac{XY}{10}$ multiplier.

The connection required for division is shown below.

In this configuration, $E_O = Y_2$. Referring to the AD534/5 functional block diagram, it is seen that V_A must equal V_B for the difference voltage at the inputs of the high-gain output amplifier to equal zero, a requirement for proper operation.

$$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} = Z_1 - Z_2$$

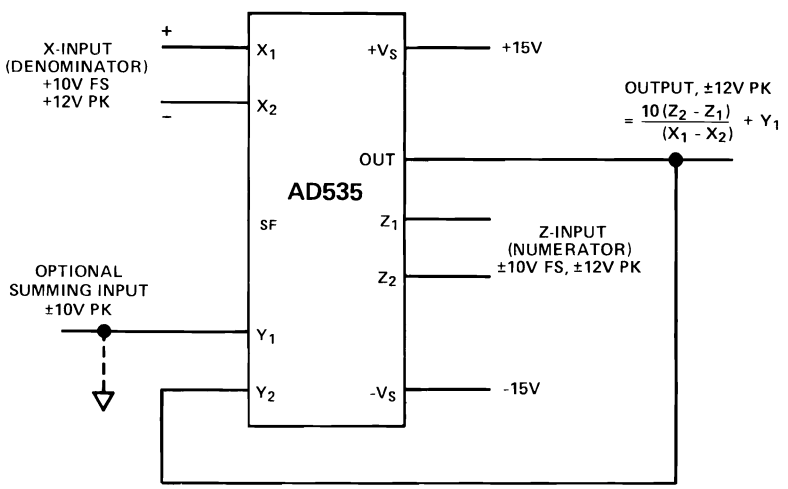
but $Y_2 = E_O$

$$\frac{(X_1 - X_2)(Y_O - E_O)}{10} = Z_1 - Z_2$$

$$Y_1 - E_O = \frac{10(Z_1 - Z_2)}{X_1 - X_2}$$

$$E_O = -10\,\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$$

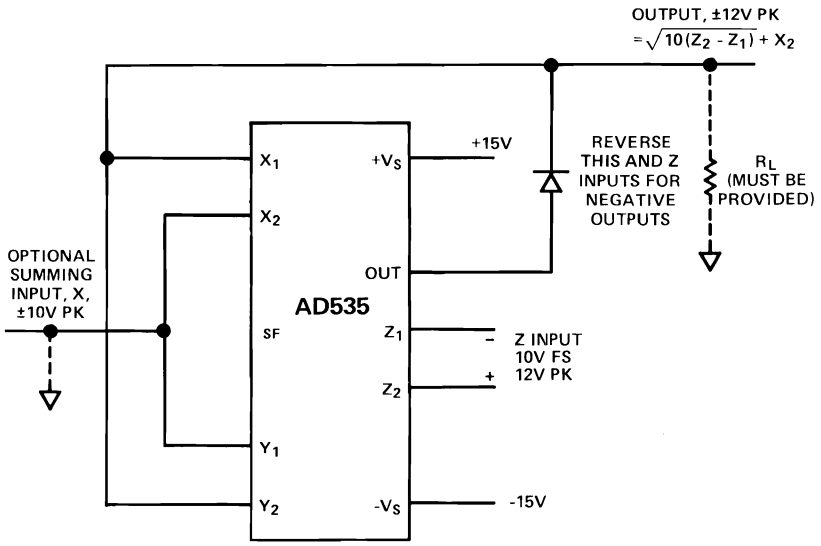
The AD535 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth and accuracy are proportional to denominator magnitude.



BASIC DIVIDER CONNECTION

Without additional trimming, the accuracy of the AD535L is sufficient to maintain a 0.5% error over a 10V to 1V denominator range. This range may be extended to 100:1 by reducing the X-offset with an externally generated trim voltage applied to the unused X-input.

The operation of the AD535 in the square root mode is shown below. The diode prevents a latching condition which could occur if the input momentarily changes polarity. As shown, the output is always positive; it may be changed to a negative output by reversing the diode direction and interchanging the Z inputs. Since the signal input is differential, all combinations of input and output polarities can be realized, but operation is restricted to the one quadrant associated with each combination of inputs.

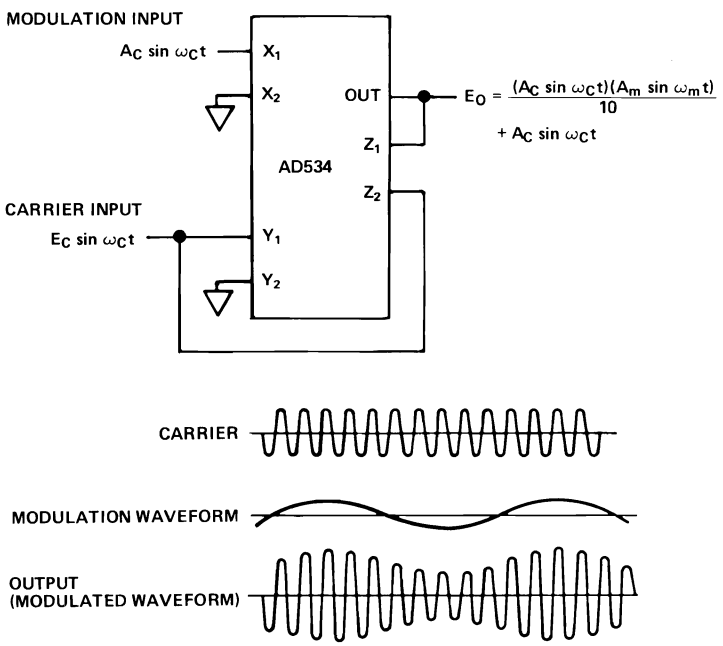


SQUARE-ROOTER CONNECTION

ANALOG MULTIPLIER APPLICATIONS

Perhaps the most obvious application for a multiplier is as an amplitude modulator. In amplitude modulation, the magnitude of a relatively high frequency sine wave (carrier) is controlled by an information or data waveform of lower frequency (modulation waveform).

If the carrier is f_c and the modulation frequency is f_m, the *modulated* waveform is $(A_C \text{ Sin } \omega_c t)(A_m \text{ Sin } \omega_m t) + A_C \text{ Sin } \omega_c t$.

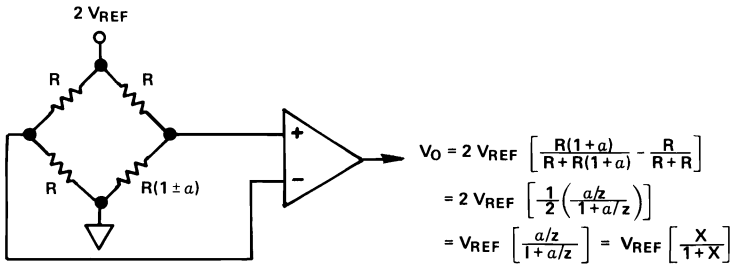


AMPLITUDE MODULATION USING THE AD534

The AD534, as shown, can be used at carrier frequencies up to approximately 1MHz with good linearity.

An analog multiplier can be used to perform implicit calculations, an example of which is linearization of a nonlinear transfer function.

A simple Wheatstone bridge, as shown below, gives an output that is inherently nonlinear.



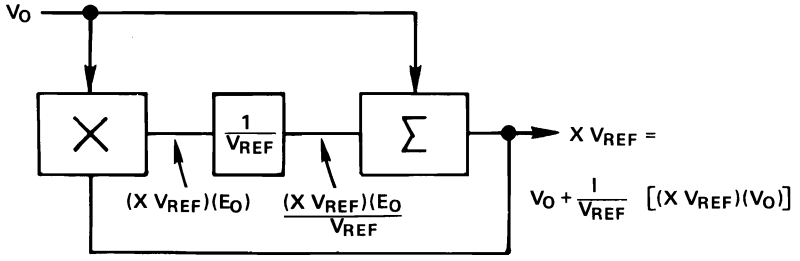
WHEATSTONE BRIDGE

The implicit solution to the above equation is:

$$V_O(1+x) = V_{REF}(x)$$

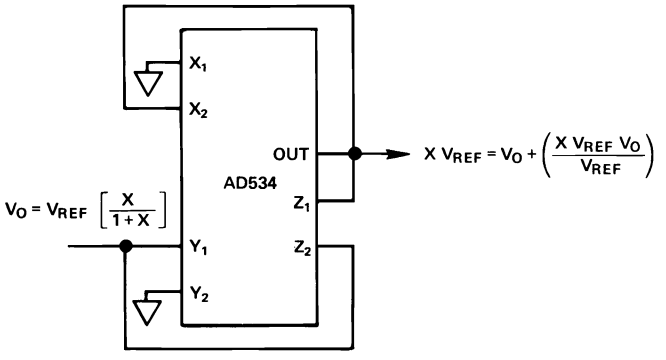
$$\text{or } XV_{REF} = V_O + \frac{I}{V_{REF}} \quad [x(V_{REF})(V_O)]$$

This transfer function can be realized with the following generalized circuit:



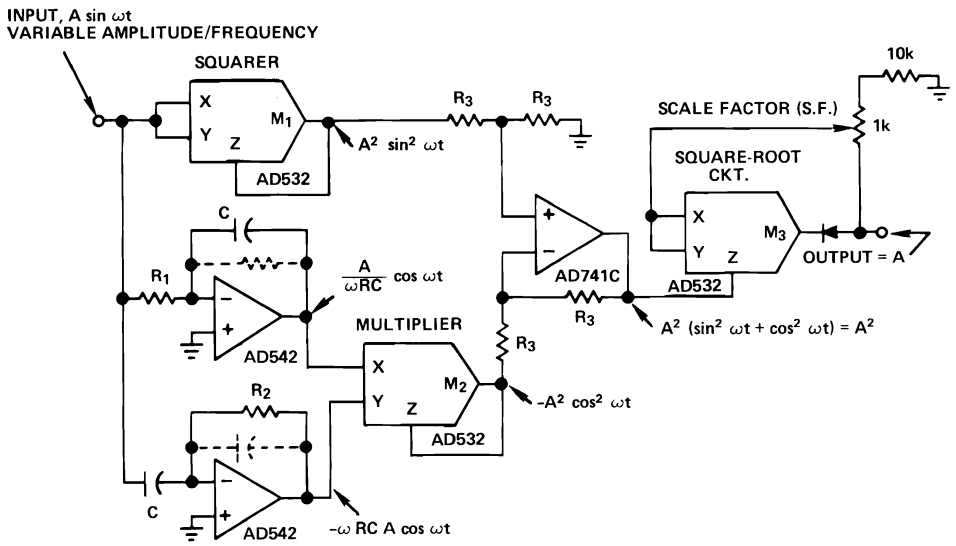
GENERALIZED BRIDGE LINEARIZATION CIRCUIT

The hardware implementation shown below utilizes the summing capability (Z input) of the AD534:

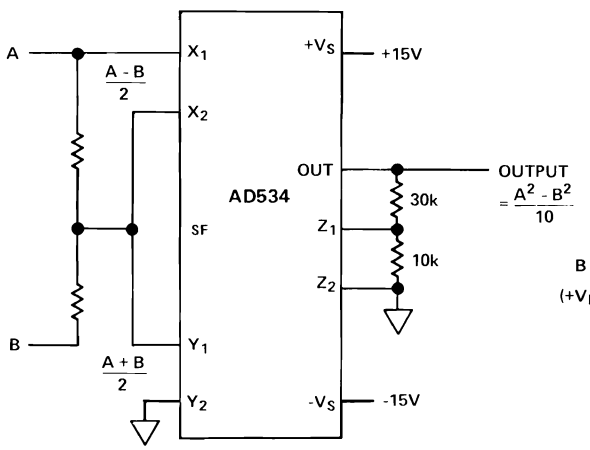


BRIDGE LINEARIZATION CIRCUIT USING THE AD534

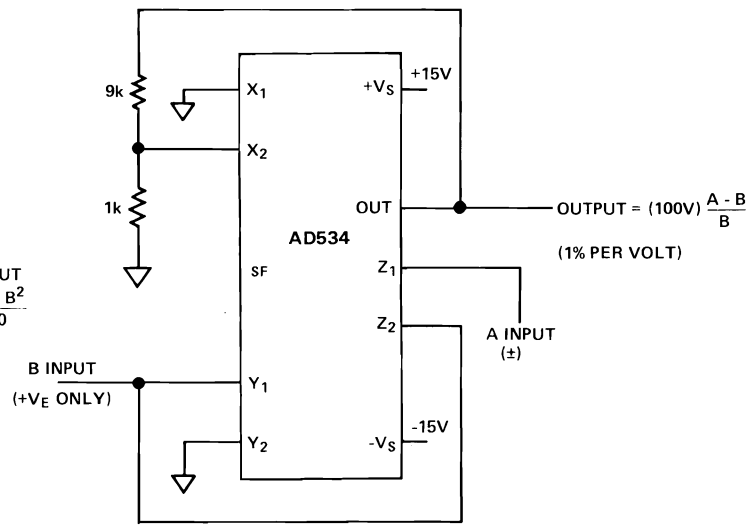
The list of implicit calculations that can be performed by analog multipliers are too lengthy to permit detailed discussion of each. Some of the more interesting examples are illustrated below:



PEAK DETECTOR
FAST RESPONSE AND LOW RIPPLE

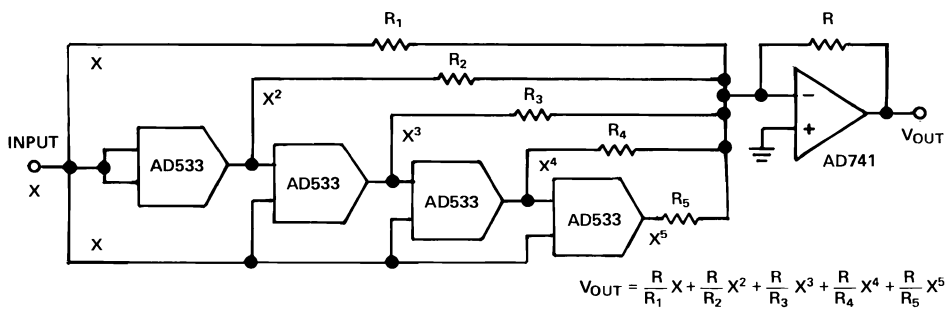


DIFFERENCE-OF-SQUARES



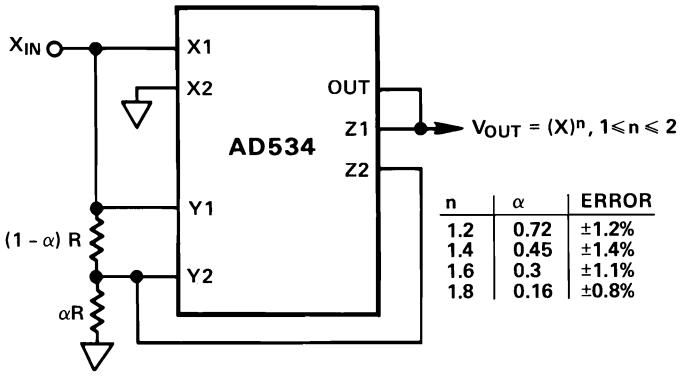
OTHER SCALES, FROM 10% PER VOLT TO 0.1% PER VOLT CAN BE OBTAINED BY ALTERING THE FEEDBACK RATIO.

PERCENTAGE COMPUTER



POWER SERIES SYNTHESIS FROM A TRIANGLE-WAVE INPUT

Integral powers and roots can obviously be implemented with analog multipliers by cascading stages. Nonintegral powers and roots are also possible by making use of some mathematical approximations. For example, the expression $Y = X^n$ can be approximated by $Y = (1 - \alpha) X^2 + \alpha X$, where α varies nonlinearity from 0 to 1 for n = 1 to 2. An error analysis shows that this approximation holds within ±1.5% at all values of n between 1 and 2, with peak error occurring at n = 1.5.

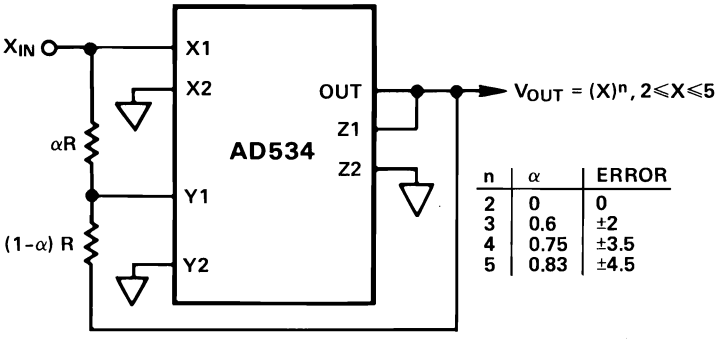


n	α	ERROR
1.2	0.72	±1.2%
1.4	0.45	±1.4%
1.6	0.3	±1.1%
1.8	0.16	±0.8%

NONINTEGRAL POWERS, $1 \leq n \leq 2$

The circuit shown will accept unipolar inputs. Negative values for X_{IN} can be used if X1 and X2 inputs are interchanged.

A similar circuit can be used for exponents between 2 and 5. The approximation used for $Y = X^n$ is $Y = \frac{(1 - \alpha) X^2}{1 - \alpha X}$, where α varies from 0 to about 0.8 for n values from 2 to 5.



n	α	ERROR
2	0	0
3	0.6	±2
4	0.75	±3.5
5	0.83	±4.5

NONINTEGRAL POWERS, $2 \leq n \leq 5$

Circuits to complete fractional powers (nonintegral roots) can also be constructed with similar approximations. The general purpose analog multiplier, then, is a very useful tool for performing otherwise complex computational tasks wholly in the analog domain.

THE LIST CONTINUES:

Voltage-Controlled Filters
Thermocouple Linearization
Time-Constant Measurement
Three Phase Power Measurement
Precision Oscillators

•
•
•
•
•

These applications and many more can be found in the previously listed sources and in:

1) *Nonlinear Circuits Handbook*, Analog Devices, 1976.
2) *Multiplier Applications Guide*, Analog Devices, 1978.

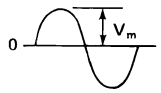
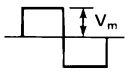
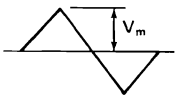
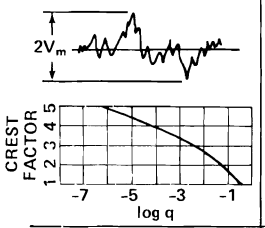
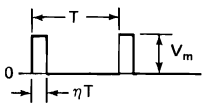
4. DEDICATED COMPUTATIONAL CIRCUITS

Occasionally, a particular analog computation is so often performed that a dedicated circuit to perform that function becomes commercially feasible. In this section, we will examine such a class of circuits.

rms COMPUTATION

The accurate calculation of the root-mean-square of an a-c waveform has long been a stumbling block to designers of a-c measurement and control instrumentation. Historically, this problem has been addressed by various means, each method tailored to the specific application.

The rms of a-c signals is important because it is a measure of the power in that signal. In sine and square waves, the rms is often calculated by measuring mean average value (or statistically, mean average deviation) and scaling accordingly. But in complex waveforms, scaling is rather difficult; examples are given in the following table.

WAVEFORM		RMS	MAD	$\frac{\text{RMS}}{\text{MAD}}$	CREST FACTOR
	SINE WAVE	$\frac{V_m}{\sqrt{2}}$ $0.707\ V_m$	$\frac{2}{\pi} V_m$ $0.637\ V_m$	$\frac{\pi}{2\sqrt{2}} = 1.111$	$\sqrt{2} = 1.414$
	SYMMETRICAL SQUARE WAVE OR DC	V_m	V_m	1	1
	TRIANGULAR WAVE OR SAWTOOTH	$\frac{V_m}{\sqrt{3}}$	$\frac{V_m}{2}$	$\frac{2}{\sqrt{3}} = 1.155$	$\sqrt{3} = 1.732$
	GAUSSIAN NOISE CREST FACTOR IS THEORETICALLY UNLIMITED. q IS THE FRACTION OF TIME DURING WHICH GREATER PEAKS CAN BE EXPECTED TO OCCUR	RMS	$\sqrt{\frac{2}{\pi}}$ RMS $= 0.798$ RMS	$\sqrt{\frac{\pi}{2}}$ 1.253	C.F. / q 1 / 32% 2 / 4.6% 3 / 0.37% 3.3 / 0.1% 3.9 / 0.01% 4 / 63ppm 4.4 / 10ppm 4.9 / 1ppm 6 / 2×10^{-9}
 η: "DUTY CYCLE"	PULSE TRAIN η / MARK/SPACE 1 / ∞ 0.25 / 0.3333 0.0625 / 0.0667 0.0156 / 0.0159 0.01 / 0.0101	$V_m \sqrt{\eta}$ V_m $0.5V_m$ $0.25V_m$ $0.125V_m$ $0.1V_m$	$V_m \eta$ V_m $0.25V_m$ $0.0625V_m$ $0.0156V_m$ $0.01V_m$	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10

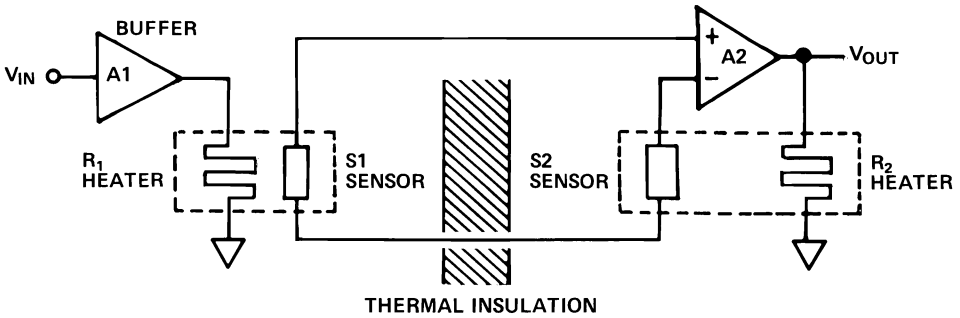
RMS, MAD, AND CREST FACTOR OF SOME COMMON WAVEFORMS

The obvious application for an rms-dc converter is in an a-c voltmeter. But true rms measurement is the *only* technique to accurately measure noise. This is useful in system and grounding design and indispensible for measuring thermal, transistor and switch contact noise. Mechanical response including strain, stress, vibration, shock, expansion and contraction are usually nonperiodic, complex and noisy; analysis and reduction of the effects of these phenomena often require true rms measurement.

Whenever irregular waveforms exist, as in SCR pulse width-height controllers, true rms measurement is ideal.

Design Techniques

The block diagram for a thermal rms-dc converter is shown below:



THERMAL RMS-DC CONVERTER

In this circuit, the waveform, V_{IN}, is applied to a heater, R1. The total energy of V_{IN} is dissipated as heat in R1 and is proportional to the rms of the input waveform. The amplifier, A2, monitors the output of a sensor S1 which puts out a signal that is related to the temperature of R1 (not necessarily a linear relationship). This signal is compared to the output of a second sensor, S2 (matched to S1), which is thermally coupled to heater R2. R2 is driven by the output of A2 which "servos" the loop so that the outputs of S1 and S2 are equal. Therefore, the energy dissipated by R2 equals the energy dissipated by R1. The output voltage of A2 is a dc level equal to the rms of V_{IN}. While very accurate (errors can be less than 0.1%), there are several significant disadvantages to this approach.

1. The heater-sensor assemblies are expensive and must be bulky to provide proper insulation. IC implementation is impractical.
2. Response is slow.
3. Accurate operating range is limited.
4. Limited dynamic range. The "Crest Factor", or ratio of peak input to rms, cannot be high. Accurate measurement of steady-state low-crest-factor waveforms (e.g. sinewaves) require operation in the upper portion of the dynamic range of the heaters. Therefore, little "headroom" remains for peaks.

If the waveshape of the input voltage is known, the peak or average can be detected and the readout can be "scaled" to the rms. For example, a sinewave rms meter can detect and display the peak of the input by scaling the meter face by a factor of 1.11.

However, if nonsinusoidal waves are measured with such a voltmeter, significant errors arise.

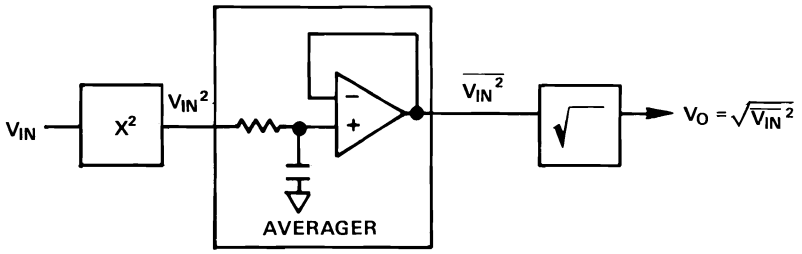
COMPARISON OF TRUE RMS TO "AVERAGE" READING METER

SIGNAL	TRUE RMS VALUE	READING ON SINE-CALIBRATED "AVERAGE" METER	ERROR
Sinewave	0.707	0.707	0%
Full-Wave Rectified Sine	0.707	0.298	-57%
Half-Wave Rectified Sine	0.500	0.382	-23%
Square Wave	1.000	1.110	+11%
Triangle Wave	0.577	0.545	-5.5%

NOTE: All Signals 1 Volt Peak

While accurate for known waveforms, this technique of rms measurement is not sufficiently versatile for use in anything but the most basic instruments such as VOM's. In this day of SCR'd sinewaves, even this application calls for a more accurate method of rms conversion.

The rms of a waveform can also be computed directly as shown below:



DIRECT COMPUTATION OF THE ROOT-MEAN-SQUARE

This technique, while serviceable, is unsatisfactory because it requires two multipliers and an op amp. It is further limited to low crest factor signals since the first block, the squarer, uses up a lot of dynamic range; its output amplitude will vary 10,000 to 1 for a 100 to 1 input amplitude range.

Perhaps the best approach to computing the rms value of a signal is simple but not direct. It involves the use of a circuit that implements an implicit solution to the rms equation

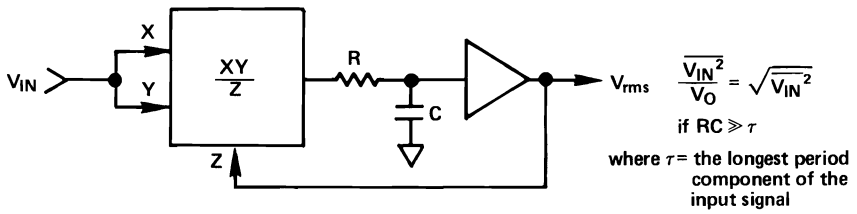
$$V_{rms} = \sqrt{\overline{V_{IN}}^2}$$

or

$$V_{rms}^2 = \overline{V_{IN}}^2$$

$$V_{rms} = \frac{\overline{V_{IN}}^2}{V_{rms}}$$

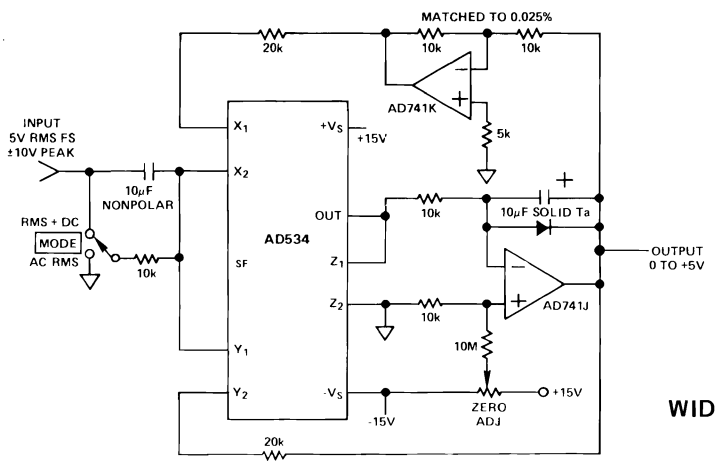
This can be easily performed thus:



IMPLICIT COMPUTATION OF THE ROOT-MEAN-SQUARE

Analog multipliers such as the AD534 can be used to accurately compute rms, but at least one additional active device will be required. Furthermore, it is ultimately the responsibility of the designer to provide the exact configuration that will optimize performance.

A dedicated rms-dc converter is a better choice in most applications. Analog Devices offers two such devices, the AD536A and the AD636, optimized for different signal ranges. These devices, unlike circuits using general-purpose components to accomplish rms computation, are specified for use in rms computation with guaranteed maximum errors. This simplified the design task for the user and assures performance to a specified level. The figures below compare a typical rms circuit using an AD534 multiplier with the equivalent circuit based on an AD536A rms-dc converter.



CALIBRATION PROCEDURE:

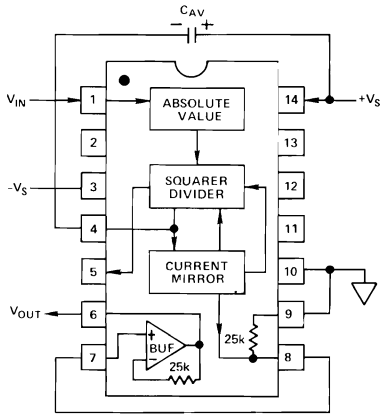
WITH 'MODE' SWITCH IN 'RMS + DC' POSITION, APPLY AN INPUT OF +1.00VDC. ADJUST ZERO UNTIL OUTPUT READS SAME AS INPUT. CHECK FOR INPUTS OF ±10V; OUTPUT SHOULD BE WITHIN ±0.05% (5mV).

ACCURACY IS MAINTAINED UP TO 100kHz, AND IS TYPICALLY HIGH BY 0.5% AT 1MHz FOR V_{IN} = 4V RMS (SINE, SQUARE OR TRIANGULAR WAVE).

PROVIDED THAT THE PEAK INPUT IS NOT EXCEEDED, CREST-FACTORS UP TO AT LEAST TEN HAVE NO APPRECIABLE EFFECT ON ACCURACY.

INPUT IMPEDANCE IS ABOUT 10kΩ; FOR HIGH (10MΩ) IMPEDANCE, REMOVE MODE SWITCH AND INPUT COUPLING COMPONENTS.

WIDEBAND, HIGH-CREST, RMS-TO-DC CONVERTER USING AN AD534 MULTIPLIER



AD536A/AD636
STANDARD RMS CONNECTION

AD536A and AD636 Principle of Operation

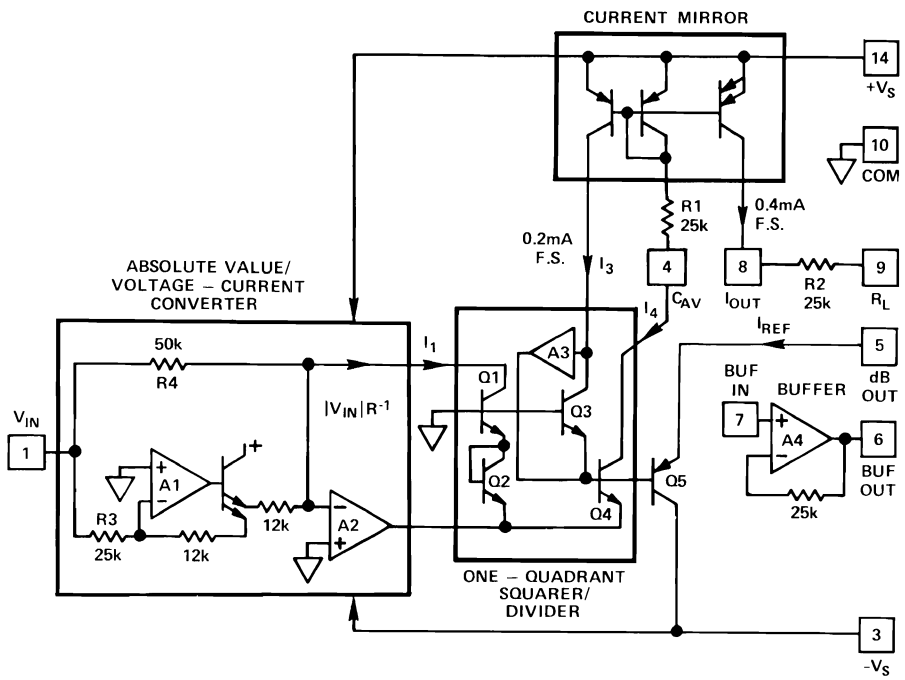
The AD536A and AD636 embody an implicit solution of the rms equation. The actual computation performed by both devices follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

COMPARISON OF MONOLITHIC RMS TO DC CONVERTER PERFORMANCE

SPECIFICATION	GENERAL PURPOSE AD536AK	LOW LEVEL AD636K
Nominal input range	0 to 2.0V rms 0 to ±10V peak	0 to 200mV rms 0 to ±2.8V peak
Total error, no external trims dc or 1kHz sinewave input	±2mV ±0.2% RDG. max	±0.2mV ±0.5% RDG. max
Error vs. crest factor		
CF = 3	-0.1%	-0.2%
CF = 7	-1.0%	-0.5%
Bandwidth, -3dB, 1V rms in	2MHz	2MHz
0.1V rms in	300kHz	800kHz
Nominal supply voltage	±15V	+3V, -5V
supply current	1.2mA typ, 2.0mA max	700μA typ, 1.0mA max
Supply voltage range	±3.0V to ±18V	±2.5V to ±15V

The simplified schematic shown below may be used to illustrate the operation of the AD536A.



AD536A SIMPLIFIED SCHEMATIC

The circuitry is divided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2/I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the $(R_1),(C_{AV})$ time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$ back to the squarer/divider to complete the implicit rms computation. Thus:

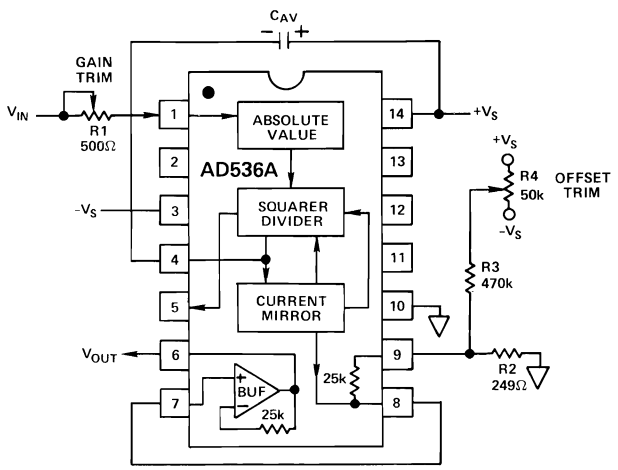
$$I_4 = \text{Avg. } [I_1^2/I_4] = I_1 \text{ rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD536A thus results:

$$V_{OUT} = 2R_2\ I_{rms} = V_{IN\ rms}$$

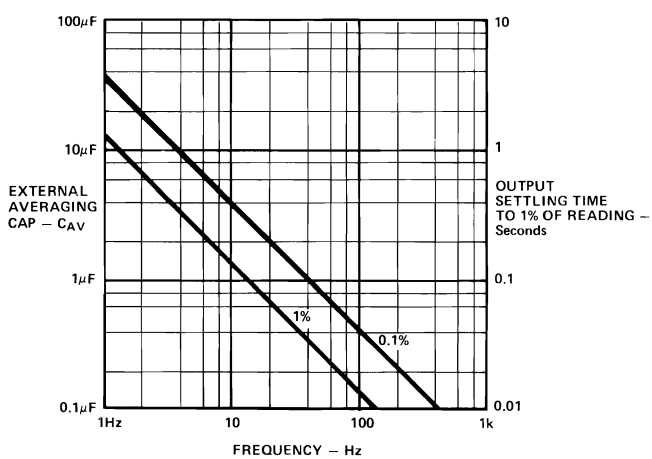
The dB output is derived from the emitter of Q_3, since the voltage at this point is proportioned to $-\log V_{IN}$. Emitter follower Q_5 buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied Q_5 emitter current (I_{REF}) approximates I_3.

The figure below shows the AD536A connection diagram for rms measurement. The trim resistors R1 and R4 are useful for optimizing device performance for a reduced signal range; the AD536A is internally trimmed for a 7V rms full scale range, while the AD636 is trimmed for a 200mV rms range.



AD536A RMS CONNECTION, SHOWING OPTIONAL EXTERNAL GAIN AND OUTPUT OFFSET TRIMS

In this configuration, the AD536A will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown.

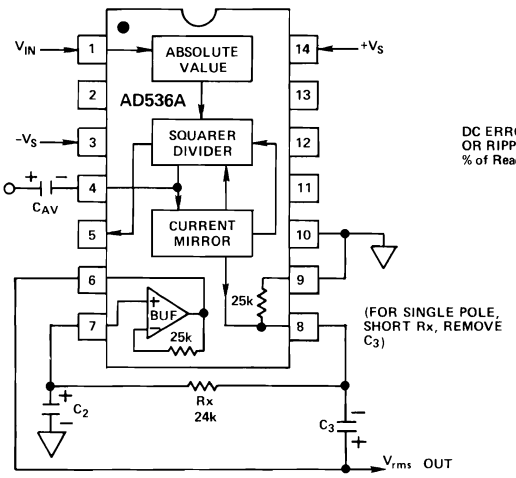


LOWER FREQUENCY FOR STATED % OF READING ERROR AND SETTLING TIME FOR STANDARD RMS CIRCUIT

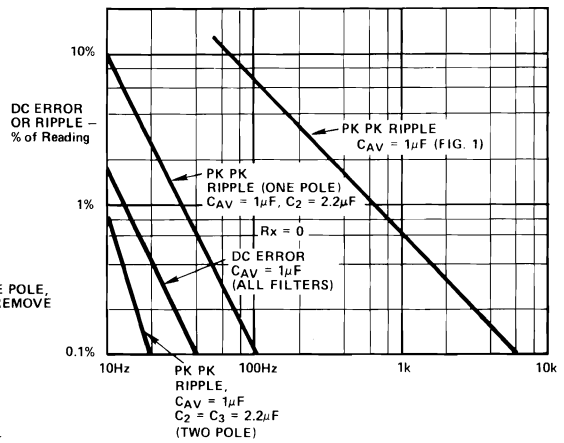
Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy above these points will be according to specification. If it is desired to reject the dc level, a capacitor is added in series with the input; that capacitor must be non-polar.

The AD536A can also be used in an unbuffered voltage output mode by disconnecting pins 7 and 8; the output then appears unbuffered at pin 8. The buffer amplifier can then be used for other purposes. The AD536A can also be used in a current output mode by disconnecting pin 9 from ground. The output current is available at pin 8 with a nominal full scale of 400μA, positive out.

Ripple can be reduced by applying a "post-filter". This can partially relieve C_{AV} of this task allowing a reduction in the size of C_{AV} which, in turn, improves settling time. Such a filter circuit is shown below along with a graph that aids in the selection of filter components.



2 POLE "POST" FILTER



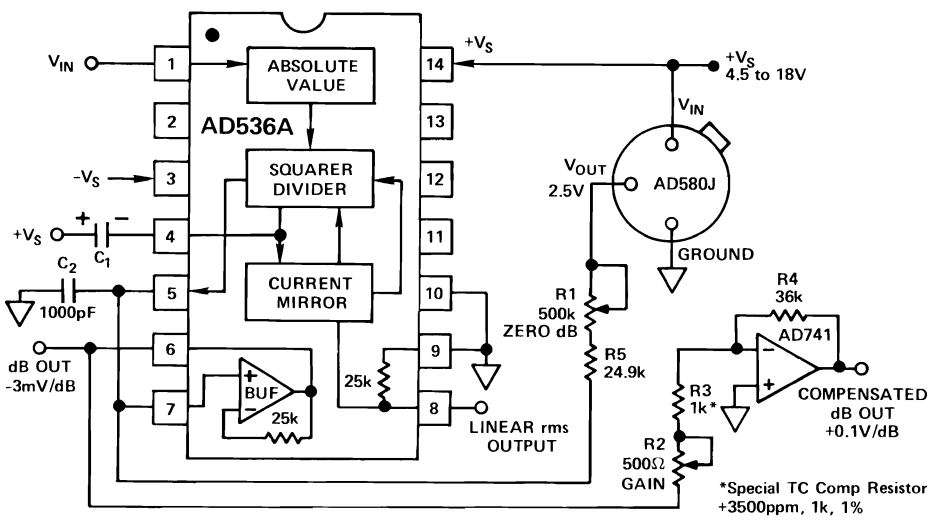
PERFORMANCE FEATURES OF VARIOUS FILTER TYPES

A feature added to both the AD536A and AD636 which is not available in other computing rms circuits, is the logarithmic or decibel output. The internal circuit which computes dB is very accurate and works well over a 60dB range. The connection for dB measurements is shown below. The user selects the 0dB by setting R_1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer/divider at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the 0.3%/°C temperature drift of the dB circuit. The special T.C. resistor, R_3, is available from Tel Labs, type number Q-81. The linear rms output is available at pin 8 with an output impedance of 25kΩ; thus many applications may require an additional buffer amplifier if this output is desired.

dB Calibration:

1. Set V_{IN} = 1.00V dc
2. Adjust R_1 for dB out = 0.00V
3. Set V_{IN} = +0.1V dc
4. Adjust R_2 for dB out = 2.00V

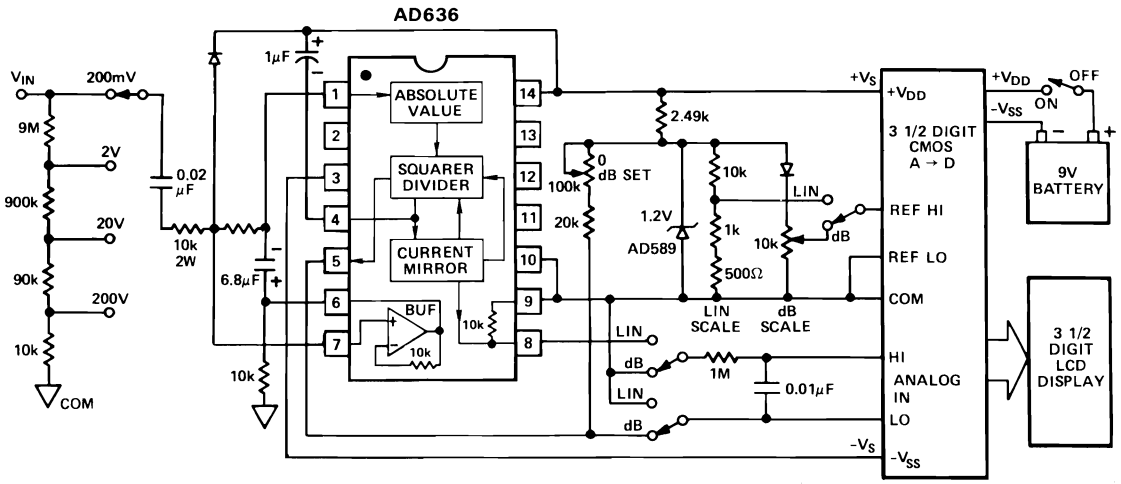
Any other desired 0dB reference level can be used by setting V_{IN} and adjusting R_1 accordingly. Note that adjusting R_2 for the proper gain automatically gives the correct temperature compensation.



dB CONNECTION

In many instrument applications, a lower input voltage range is encountered; 0 to 200mV is popular with manufacturers of digital voltmeters. And, since many DVMs are of the battery-powered, (portable) variety, there exists a requirement for lower supply voltage and current operation.

The AD636 has been developed to satisfy that requirement. The circuit is substantially the same as the AD536A, but with different resistor values.



BATTERY POWERED RMS DIGITAL VOLTMETER

The circuit above is a schematic of a battery powered 3 1/2 digit true rms voltmeter that features both linear and dB scales. The entire circuit draws about 2.5mA from the 9V battery, permitting 100 hours of continuous operation. The overall midband error of this meter can be as small as ±3 digits.

In this voltmeter application, the AD636's on-chip unity gain amplifier is connected to buffer the input range attenuator from the low input resistance of the converters absolute value section. The meter's input signal is ac coupled into the buffer input through the 0.02μF capacitor and the 10kΩ input protect resistor. In turn the buffer's output is ac coupled into the converter to minimize errors due to the buffer's dc offset voltage. The 1MΩ resistor provides a return path for the buffer's dc input current, and also "bootstraps" the buffer's input impedance to over 100MΩ at midband.

In the linear rms mode, the A to D reads, converts and displays the rms converters output voltage on a one-to-one basis.

The signal processing in the dB mode is not quite so straightforward. The voltage at the AD636 dB output pin is:

$$V_{dB} = -kT/q \ln (V_{rms}/V_{REF})$$

$$V_{REF} = 0dB \text{ set level}$$

At room temperature this amounts to a -3mV change in output voltage for a +1dB change in input. To be useful, this dB voltage must be inverted, scaled to a more convenient value, and corrected for the approximately 0.3%/°C scale factor drift introduced by the "T" in the equation.

The inversion is easily accomplished by interchanging the AD converters HI and LO inputs in the dB mode. The required scaling, in this case to 1mV per dB, and temperature compensation are effected by increasing the converter's reference voltage from 100mV to 300mV, and making this voltage increase proportional to absolute temperature. The series connection of a silicon diode and dB gain set pot across the 1.2V "bandgap" reference zener automatically generates the required TC.

Section IV

Analog Switches and Multiplexers

Analog Switches and Multiplexers

1. Types of Analog Switches
2. Specifications and Their Meanings
3. Applying the CMOS Switch

ANALOG SWITCHES

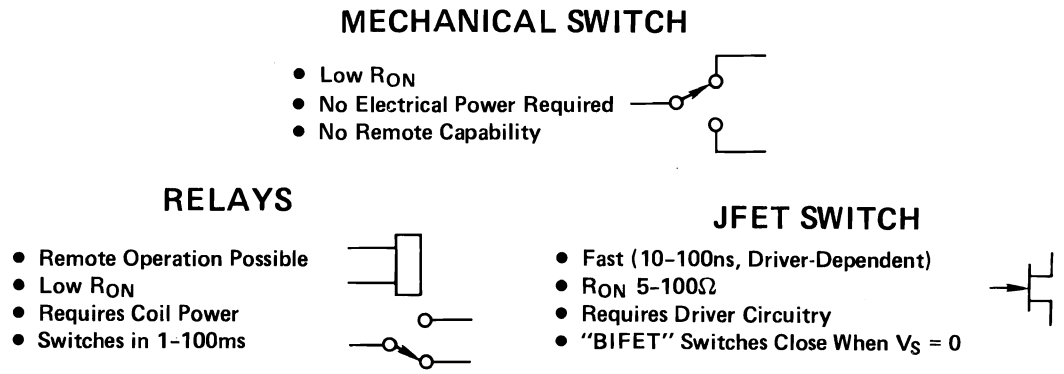
While the preceding three chapters have dealt exclusively with analog circuitry, this section represents a limited foray into the digital domain.

Analog switches provide a means for external manipulation of analog data or signals. Like their mechcal counterparts, these manipulations are performed by external influences, be they a human finger or a bit from a computer. The integrated circuit analog switch is thus a highly useful component in analog circuitry.

In order to properly select the correct switch for a particular application, a thorough understanding of device specifications and their contributions to total circuit accuracy as well as an idea of the limitations of such switches is necessary.

TYPES OF ANALOG SWITCHES

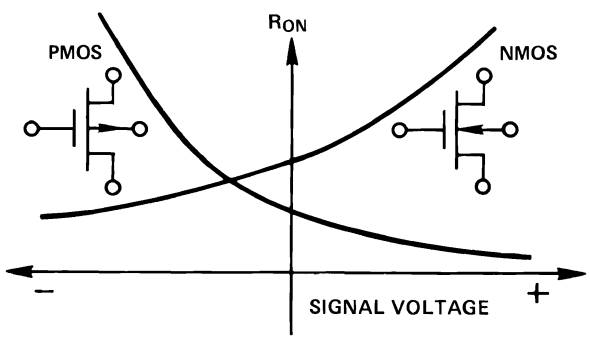
Over the years, devices for switching analog signals have taken many forms. The simple manually-operated mechanical switch is still used extensively. Such switches are available in a nearly infinite number of configurations. The mechanical switch has the advantages of low on resistance and zero power requirements but the disadvantages of large size and no remote control capability.



The problem of remote operation is solved by the relay—a mechanical switch opened and closed by a remotely activated magnetic field. The relay does, however, require some power to the coil.

The junction transistor is sometimes used as a switch. However, a base-emitter voltage drop is inserted in the signal path and this can be awkward to compensate. Furthermore, junction transistors are undirectional and will only conduct current in one direction.

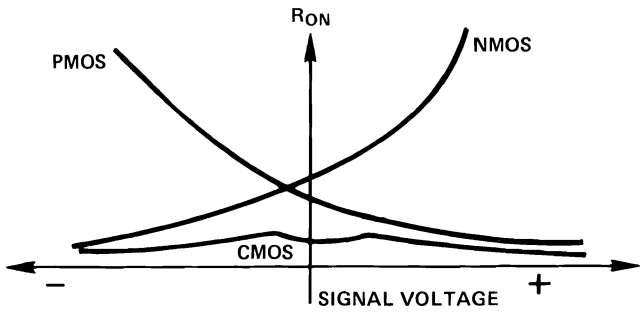
Junction FETs are somewhat better suited to switching signals bidirectionally. Discrete JFETs require level-shifters to provide a suitable drive signal, and this can be awkward to implement.



R_{ON} VS. SIGNAL VOLTAGE

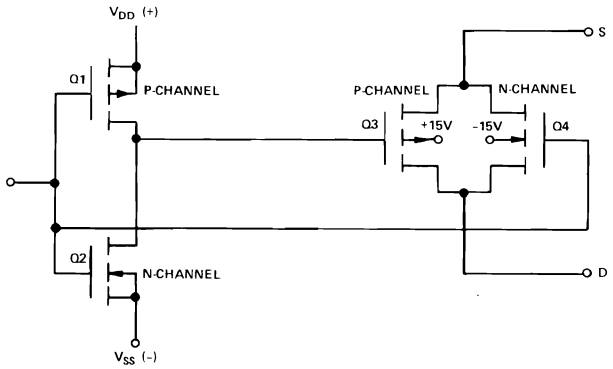
MOSFETs are well-suited to analog switching applications. They are easily integrated along with the required drive circuitry on one chip. The disadvantage of either PMOS or NMOS switches is the sensitivity of on resistance to signal voltage level.

This problem can be eliminated almost completely with a CMOS switch. A CMOS switch consists of two switches in parallel, a p-channel MOSFET and an n-channel MOSFET. The parallel combination yields a relatively flat R_{ON} vs. analog voltage curve.



CMOS SWITCH R_{ON} CHARACTERISTIC

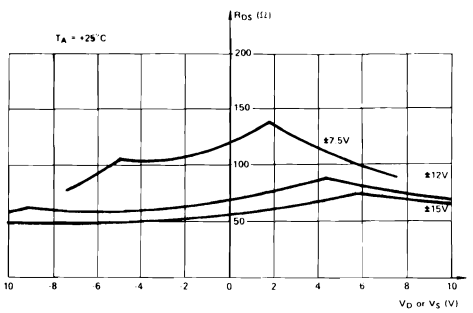
This figure shows the basic CMOS switch design used in our analog switch and multiplexer products. The design employs both p-channel and n-channel switches, so that analog signals over the entire range from -10 volts to +10 volts can be processed. The inverter in front of the switch is required because n-channel and p-channel devices require opposite drive-polarities.



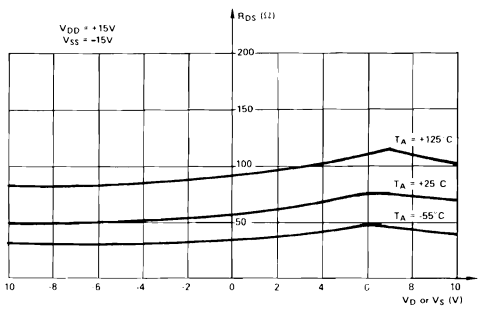
BASIC CMOS SWITCH

Such a switch has the advantages of low power consumption as well as low on resistance—generally 100 ohms or less over a wide range of signal and supply voltages and ambient temperatures.

R_{DS} AS A FUNCTION OF SWITCH VOLTAGE V_D (V_S)



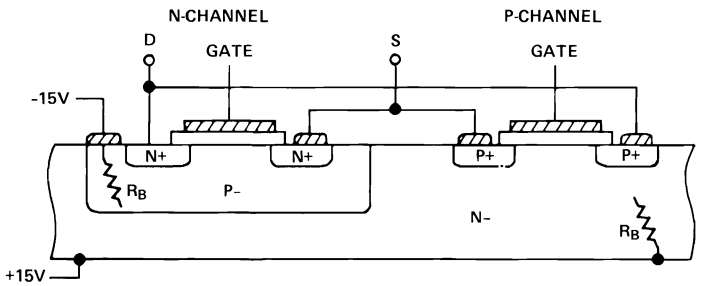
AT DIFFERENT POWER SUPPLIES



AT DIFFERENT TEMPERATURES

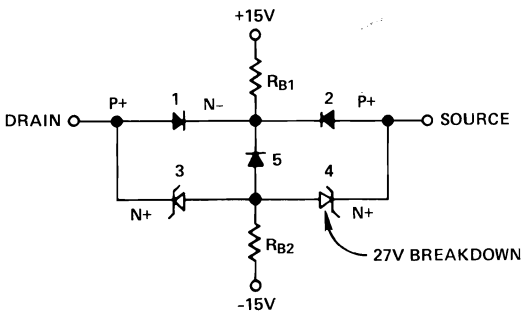
The conventional junction-isolated CMOS switch suffers from only one major drawback—it is prone to latch-up if a signal exceeds the supply or voltage or if two signals applied to different switches in a single package are greatly separated.

The drawing below shows a cross section of a junction-isolated CMOS switch.



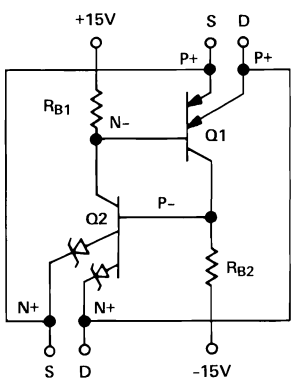
CROSS SECTION OF JUNCTION-ISOLATED CMOS SWITCH

Note that the sources of both the N- and P-channel devices, as well as the drains of both devices, are tied together. The substrate of the P-channel device (N-region) is tied to V+ while the substrate of the N-channel device (P- pocket or P-well) is tied to V-. The resistances R_B are the bulk resistance from substrate to the supply voltages. An equivalent circuit can now be drawn, as shown below.



DIODE EQUIVALENT CIRCUIT OF CMOS SWITCHING ELEMENT

If the analog input voltage at either the S or D terminals exceed the power supply voltages, the parasitic transistors formed by the various diode junctions shown above are placed into a forward bias mode. These parasitic NPN and PNP transistors appear to form the SCR circuit shown below.

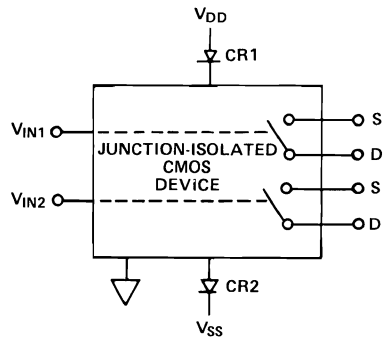


PARASITIC TRANSISTOR ACTION IN CMOS SWITCH

For example, consider the case of a positive overvoltage applied to the drain terminal of a CMOS switch. Since the base of Q1 is normally at V_{DD}, it will conduct when its emitter voltage exceeds V_{DD} by a V_{BE} drop. The collector current of Q1 will increase to a level limited only by the V_{SS} and V_D current limitations. Since the metal interconnect to the power supply terminal is normally designed to handle small currents, the current densities involved can cause device failure.

The preceding analysis is also valid for any S and D terminal between any two or more switches.

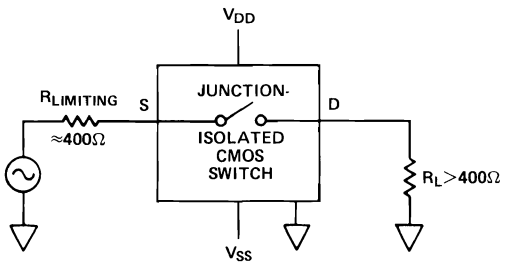
Normally, the outputs of operational amplifiers are used as the voltage sources feeding the S or D terminals so the currents cannot exceed the op amp's dc output current limitations. The op amps may even be powered from the same supply as the CMOS device, but it still is possible for transient induced currents to destroy the CMOS device, therefore one or more of the following protection schemes should be employed.



DIODE PROTECTION

The above drawing illustrates a method of preventing the initial turn-on of the parasitic transistors. The diodes CR1 and CR2 are placed in series with the supply lines. If the S or D terminal exceeds either supply voltage, CR1 and/or CR2 are reverse biased, therefore no base drive is available to cause transistor turn-on. When this method is employed, it is advised that each CMOS package have its own protection diodes. If, for example, two or more CMOS switches utilize common protection diodes, it is possible for the power supply current of one switch to furnish the required base current for parasitic transistor action on another device, even though the protection diode is reverse biased. The diodes used can be any general purpose device, such as a 1N914.

Even the diode protection scheme is not infallible. The internal diodes 3 and 4 in the equivalent circuit have a 27-30V reverse breakdown while diodes 1 and 2 have a 40-50V breakdown. This means that if one of the terminals, say "S", has a potential above +12V (assuming V_{SS}=−15V), an avalanche current will run through the diode and RB2 to the −15V supply. Therefore, the potential of the base of Q2 can be raised above the −15V line, turning on Q2 if the other terminal (emitter) is sufficiently negative. If +15V is applied to terminal "S" (instead of +12V), then the potential on the base of Q2 will be −12V (because of the 27V zener), limiting potential on the other terminal to approximately −12.5V before Q2 turns on. The only way to protect against this condition is to have a 300 or 400 ohm resistor in series with both terminals "S" and "D", as shown below. This will prevent burn-out.



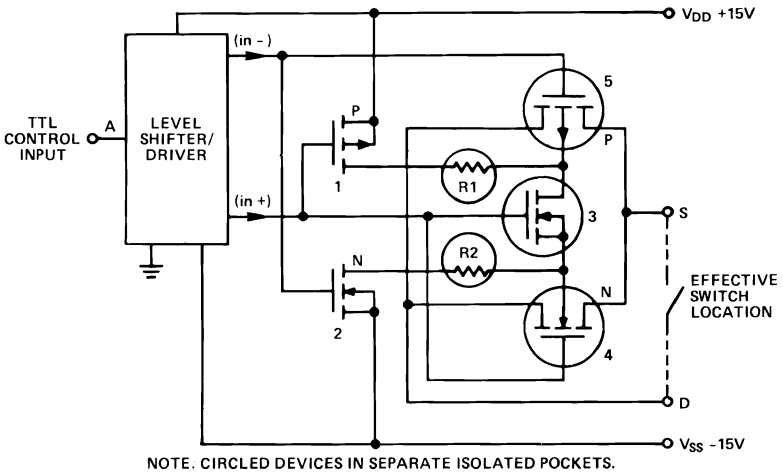
CURRENT LIMITING PROTECTION

Unfortunately, the addition of this resistor increases the effective on resistance of the switch by a factor of five.

DIELECTRIC ISOLATION

- **The Process of Choice for Switches**
- **Low Power**
- **Low R_{ON}**
- **Bulletproof**

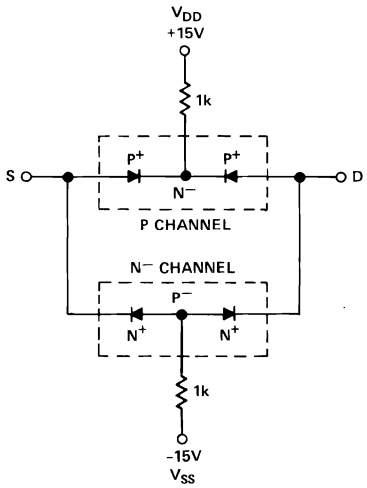
The dielectric-isolated (or DI) CMOS switch eliminates the problems of latch-up. Internally protected against overvoltages, they retain all the features of junction-isolated CMOS switches.



NOTE. CIRCLED DEVICES IN SEPARATE ISOLATED POCKETS.

SCHEMATIC OF DI CMOS SWITCH

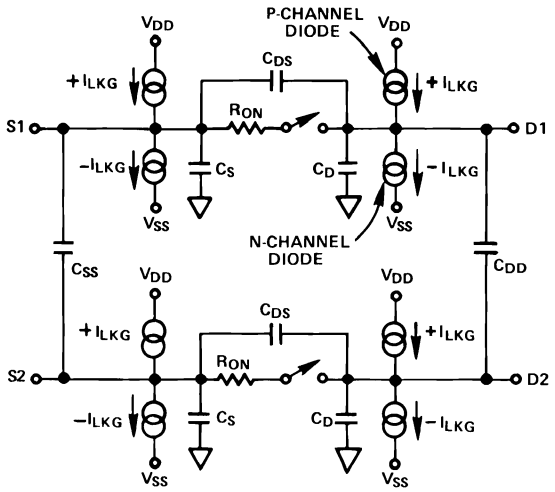
Note from the above schematic that the signal-carrying FETs are located in isolated pockets, eliminating parasitic junctions. Also, the protection resistors (R1 and R2) are *not* in series with the signal path. This novel protection arrangement provides protection for signals to ±25V past the supply rails with no increase in on resistance.



AD7590DI SERIES DIODE-EQUIVALENT CIRCUIT

SWITCH SPECIFICATIONS

So far in this chapter we have only discussed one specification of switches—the on resistance. Another low-frequency error must also be considered—the leakage currents. High-frequency errors include the effects of parasitic capacitances as shown in the model below:



EQUIVALENT CIRCUIT OF TWO ADJACENT SWITCHES

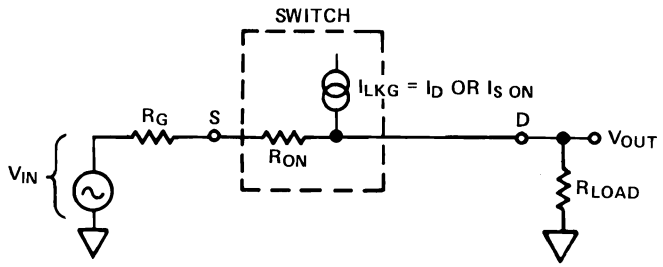
Typical values for some of these specs are as follows:

TYPICAL SWITCH SPECIFICATIONS (AD7590DI)

R_{ON}:	60Ω typ, 90Ω max
I_{LKG}:	0.5nA typ, 5nA max
C_{DS}:	1pF typ
C_D, C_S:	10pF typ (Off)
	30pF typ (On)
C_{DD}, C_{SS}:	0.5pF typ
t_{ON}, t_{OFF}:	170ns, 340ns

The on resistance and leakage current specs determine low frequency signal transmission accuracy. Their effects can only be properly analyzed if the external source and load impedances are known.

A low frequency model of a switch in the "ON" condition is shown below. It is obviously desirable to have a very high value of R_{LOAD} to minimize voltage divider effects with R_{ON}. Further, low values of R_G are desirable, since switch leakage current will flow through this resistance, causing another error.



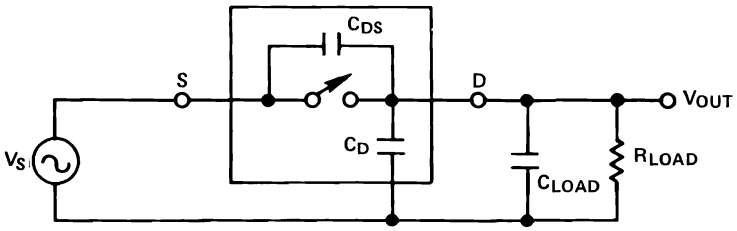
$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_G + R_{ON} + R_{LOAD}}\right] + I_{LKG}\left[\frac{R_{LOAD}(R_{ON} + R_G)}{R_G + R_{ON} + R_{LOAD}}\right]$$

If $R_G \rightarrow 0$,

$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_{LOAD} + R_{ON}}\right] + I_{LKG}\left[\frac{R_{LOAD}\,R_{ON}}{R_{LOAD} + R_{ON}}\right]$$

MODEL OF SWITCH IN "ON" CONDITION

The primary concerns in using analog switches in ac applications are bandwidth and off isolation. These specifications are not often specified on switch data sheets, and with good reason. It is impossible for a manufacturer to test a switch for ac parameters without first knowing the load resistance and capacitance of the planned application circuit. As shown in the circuit below, the load resistance and capacitance directly impact off isolation.



CIRCUIT MODEL FOR OFF ISOLATION

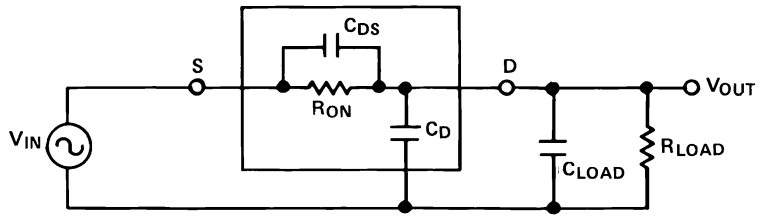
To illustrate the sensitivity to load impedances, try computing the off isolation with various load impedances. As an example, consider a switch with C_{DS} of 0.5pF, $C_{D(OFF)}$ of 10pF, an operating frequency of 1MHz, and two combinations of load resistance and capacitance.

LOAD AFFECTS OFF ISOLATION

At 1MHz, C_{DS} = 1.0pF, C_D = 10pF:

If R_L = 1kΩ	If R_L = 10kΩ
C_L = 100pF	C_L = 10pF
Off Isolation is -48dB	Off Isolation is -31dB

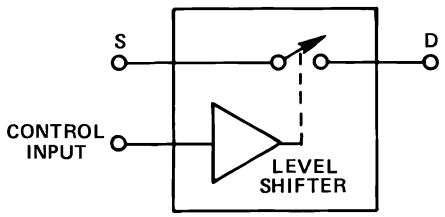
A similar analysis can be performed for the circuit model below, in order to compute the available bandwidth for a particular set of load conditions.



CIRCUIT MODEL FOR BANDWIDTH ANALYSIS

Another set of specifications important in analog switch applications is the turn-on and turn-off time characteristics.

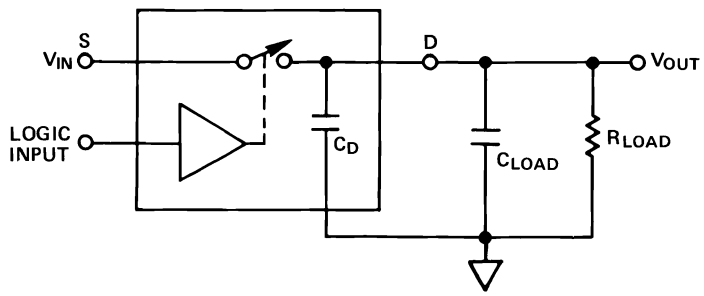
When a switch is commanded to switch on or off, there is a propagation delay in the level shifter/driver circuits. These t_{ON} and t_{OFF} specs can be used to determine when a switch begins to operate, and to determine whether multiple switches connected as a multiplexer will have make-before-break or break-before-make operation.



PROPAGATION DELAY IN ANALOG SWITCH

Propagation delay should not be confused with settling time. Settling time of a switch, like off isolation and bandwidth, is directly affected by load capacitance and resistance.

For a switch turning from OFF to ON or ON to OFF, the settling time to a given error band can be computed by examining the model shown below.



$$\text{OFF-TO-ON: } t_{SETT} = t_{ON} + \frac{R_{ON}\,R_{LOAD}}{R_{ON}+R_{LOAD}}\,(C_{LOAD}+C_D)\,\text{-ln}\,\frac{\%\ \text{ERROR}}{100}$$

$$\text{ON-TO-OFF: } t_{SETT} = t_{OFF} + (R_{LOAD})\,(C_{LOAD}+C_D)\,\text{-ln}\,\frac{\%\ \text{ERROR}}{100}$$

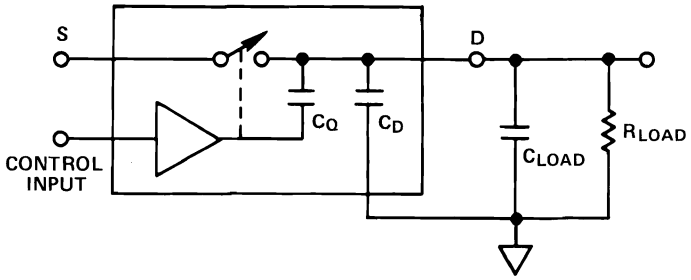
SETTLING TIME MODEL

The $\ln\left(\frac{\%\ \text{ERROR}}{100}\right)$ term can be recognized as the number of time constants required (with a single-pole response) to reach a particular error band.

One additional specification related to transitions in analog switches is charge injection. Charge injection comes about due to capacitive coupling through the gates of the FET switches. Its effect is to create a voltage step on any output capacitance according to the formula:

$$\Delta V = \frac{Q_{INJ}}{C_{OUT}}$$

This is particularly annoying in sample-hold amplifier applications since it introduces an error between the sample and hold modes.

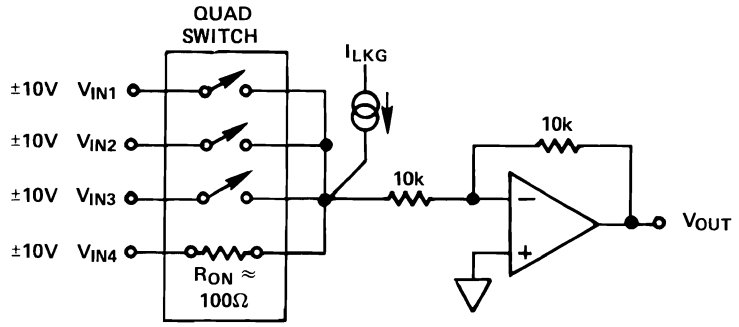


CHARGE INJECTION MODEL

The voltage pedestal error can be reduced by increasing the load capacitance, at the expense of settling time. The AD7590DI series switches feature typical charge injection of 40pC which translates to a peak transient of 40mV with a 1000pF load capacitor, or 4 millivolts with a 10,000pF capacitor. The length of the pulse depends on the load resistance.

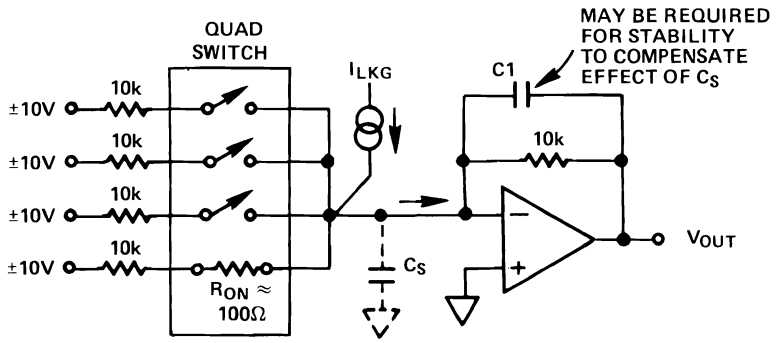
APPLYING ANALOG SWITCHES

The obvious application for an analog switch is to select one of several signals to be amplified. In the inverting amplifier shown below, the on resistance of the switch introduces a gain error.



UNITY-GAIN INVERTER WITH SWITCHED INPUT

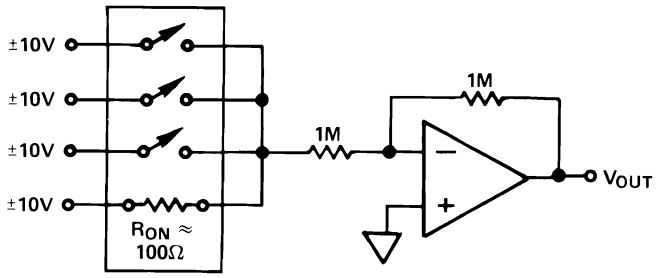
Recalling that CMOS switches have some small variations with signal voltage as well as environmental conditions, it is clear that this circuit will produce significant and nonlinear errors. The circuit can be improved by placing the switch at the summing junction end of the input resistor. This reduces the signal voltage variations seen at the switch, thereby maintaining a more constant on resistance.



CONNECTING SWITCH AT THE SUMMING POINT

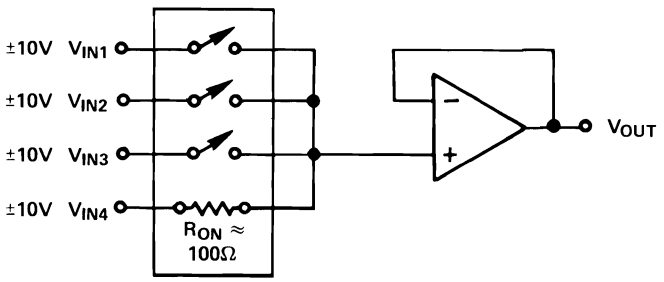
One disadvantage of this circuit is that the switch capacitance appearing at the summing junction may de-stabilize the amplifier. If this happens, a feedback capacitor may be necessary to compensate for the excess summing-junction capacitance, and this will limit overall circuit bandwidth. Additionally, four input resistors are required, as opposed to one in the original circuit.

The variations in R_{ON} with signal and temperature can be compensated by connecting a closed switch. Of course, raising the impedances in the circuit will reduce the effect of switch resistance variations. The trade-off here is increased noise, and dc offsets due to switch leakage currents and amplifier bias currents flowing through such large resistances.



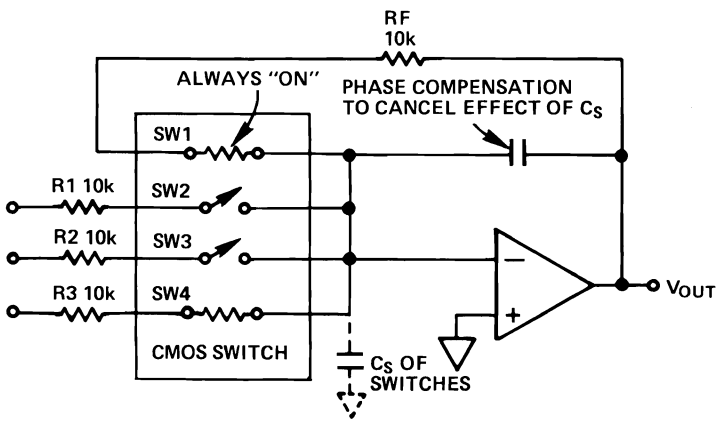
USING LARGER VALUES OF RESISTANCE

A better solution is to follow the switch with a noninverting amplifier, which carries the impedance-raising technique to an extreme. In the event that an inverting function is actually required, the follower can be followed by an inverter.



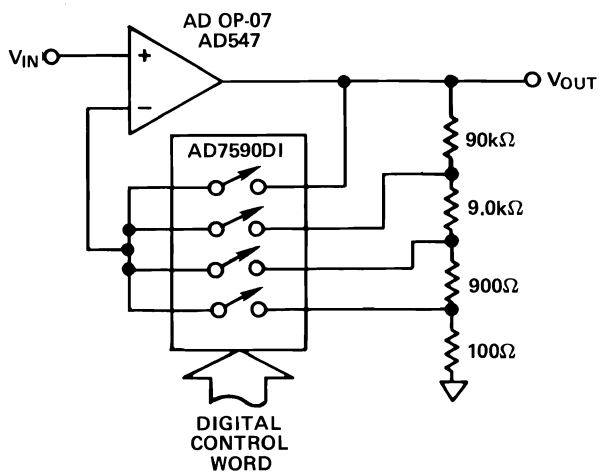
NONINVERTING SOLUTION

It is worth noting that if, for some reason, signals are applied with the switch power off, all signal sources are disconnected if a CMOS switch is used. With a JFET (this includes "BIFET" switches), all switches revert to an ON state with power removed. This can cause problems for both the switch and the signal sources in series with the feedback resistance as shown below. This, of course, restricts the circuit to three inputs. The previously–mentioned difficulties of excessive summing–point capacitance also still exist.



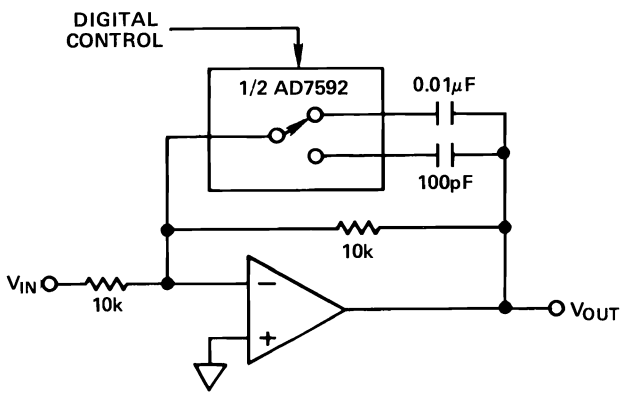
SWITCH IN SERIES WITH FEEDBACK RESISTOR COMPENSATES GAIN

A switched-gain amplifier can be implemented by using a CMOS switch to select taps on a resistive output attenuator. This circuit is capable of high accuracy and linearity if good quality resistors and a precision op amp are used. Switch on resistance is a very minor error contributor since only amplifier bias current flows through it. The AD7590 is chosen because it provides a make-before-break operation, necessary to prevent the amplifier from running open-loop during gain switching.



SWITCH-GAIN AMPLIFIER

Filter time constants can also be digitally controlled by using analog switches. In the circuit shown below, the low-pass cutoff frequency can be changed by selecting one of two capacitors. This circuit is useful in applications where a coarse reading is to be taken, and high-frequency noise can be tolerated, and a finer reading will also be required, demanding much less noise. Of course, this technique is not limited to low pass filters. Any filter function can be adapted to this basic idea of switching capacitors to alter filter frequency response.



DIGITALLY CONTROLLED LOW-PASS FILTER

Appendix A

STANDARD VALUE DECADE FOR 1% DECADE FOR 1% FILM RESISTORS

Ohms*

10.0	14.7	21.5	31.6	46.4	68.1
10.2	15.0	22.1	32.4	47.5	69.8
10.5	15.4	22.6	33.2	48.7	71.5
10.7	15.8	23.2	34.0	49.9	73.2
11.0	16.2	23.7	34.8	51.1	75.0
11.3	16.5	24.3	35.7	52.3	76.8
11.5	16.9	24.9	36.5	53.6	78.7
11.8	17.4	25.5	37.4	54.9	80.6
12.1	17.8	26.1	38.3	56.2	82.5
12.4	18.2	26.7	39.2	57.6	84.5
12.7	18.7	27.4	40.2	59.0	86.6
13.0	19.1	28.0	41.2	60.4	88.7
13.3	19.6	28.7	42.2	61.9	90.9
13.7	20.0	29.4	43.2	63.4	93.1
14.0	20.5	30.1	44.2	64.9	95.3
14.3	21.0	30.9	45.2	66.5	97.6

*Standard resistance values are obtained from the decade by multiplying by powers of 10. Ex.: 13.3 can be 13.3, 133, 1.33K, 13.3K, 133K, or 1.33MΩ.

Appendix B

CHARACTERISTICS OF VARIOUS CAPACITOR TYPES

Type		Capacitance Range	Voltage Range	Tempco ppm/°C	D.A. %	Leakage Ohm – μF
Ceramic –	COG	1pF - 0.1μF	50-600	0 ±30	0.2	$5X10^8$
	COH	1pF - 0.01μF	50-600	0 ±60	0.2	$5X10^8$
	COJ	1pF - 0.01μF	50-600	0 ±120	0.2	$5X10^8$
	COK	1pF - 0.01μF	50-600	0 ±250	0.2	$5X10^8$
	U2J	1pF - 0.01μF	50-600	-750 ±120	0.2	$5X10^8$
	P3K	100pF - 0.01μF	50-600	-1500 ±250	0.2	$5X10^8$
	X7R	10pF - 2.7μF	50-100	+1000 ±3000	0.2	$10^8 - 10^9$
	Y5F	0.01 - 2.2μF	3-50	±2500	0.2	$10^5 - 10^8$
	Y5R	0.01 - 2.2μF	3-50	±3000	0.2	$10^5 - 10^8$
	Y5T	0.01 - 2.2μF	3-50	+1000 ±4000	0.2	$10^5 - 10^8$
	Y5V	470pF -4.7μF	50-100	±20,000	0.2	10^9
	S2L	3-200pF	1k-6k	-330 ±500	0.2	$8X10^7$
	S3N	3-200pF	1k-6k	-3300 ±2500	0.2	$8X10^7$
	X5F	100pF - 0.01μF	50-600	-500 ±2500	0.2	$5X10^4 - 10^{10}$
	X5U	100pF - 0.01μF	50-600	±7500	0.2	$5X10^4 - 10^{10}$
	Z5F	100pF - 0.01μF	50-6k	±2000	0.2	$5X10^4 - 10^{10}$
	Z5P	0.001 - 0.01μF	50-6k	+2500 ±2500	0.2	$5X10^4 - 10^{10}$
	Z5R	0.005 - 0.1μF	50-6k	+2500 ±2500	0.2	$5X10^4 - 10^{10}$
	Z5U	0.001 - 4.7μF	50-6k	±10,000	0.2	$5X10^4 - 10^{10}$
	Z5V	0.001 - 0.1μF	50-600	±10,000	0.2	$5X10^4 - 10^{10}$
Silver Mica		1pF - 0.1μF	100-2k	±500 to ±10	1.0	$10^9 - 10^{11}$
Polyester (mylar)		0.001 - 10μF	50-1600	+400 ±200	0.5	$5X10^9 - 10^{11}$
Polystyrene		20pF - 30μF	30-600	-120 ±30	0.02	$10^{11} - 10^{12}$
Polycarbonate		0.001 - 25μF	50-400	0 ±100	0.2	$10^{10} - 10^{11}$
Polypropylene		100pF - 0.15μF	200-1600	-450 ±300	0.02	$10^{10} - 10^{12}$
Parylene		0.001 - 1μF	30-100	0 ±50, -200	0.05	$10^{10} - 10^{12}$
Teflon		0.001 - 1μF	50-600	-200	0.02	$10^{11} - 10^{12}$
Paper Impregnated		0.0005 - 100μF	200-15k	0 ±500	2.0	$10^9 - 5X10^{10}$
Glass		0.5pF - 0.01μF	300-1k	+140 ±25	2.0	10^9
High K Glass		10pF - 0.01μF	50-100	±4500	5.0	10^9
Aluminum Foil		0.5μF - 1F	3-500	+10,000	10	0.01 - 10μA/μF
Solid Tantalum		0.001 - 1000μF	3-125	+1000	2	0.01 - 1μA/μF
Tantalum Foil		0.1 - 10,000μF	3-500	+2500		0.01 - 1μA/μF

All values shown are representative figures.

Appendix C

INTEGRATOR REFERENCE POINTS FOR ANALOG DEVICES ICS

	Internal Integrator Referred to:	Comments
AD380	V+	
AD381	V-	
AD382	V-	
AD3554	V+	
AD503	V-	
AD504	V+	External Cap
AD506	V-	
AD507	—	External Cap to Signal Common or V+
AD509	—	External Cap to Signal Common or V+
AD510	V+	
AD515	V-	
AD517	V+	
AD518	V+, V-	Internal Feedforward Cap V+ to V- and Integrator to Output
AD521	V-	Output Amplifier Integrator Refers to V-
AD522	V+, V-	Input Amplifier Refers to V+ Output Amplifier Refers to V-
AD523	V-	
AD524, AD624	V-	
AD528	V+, V-	Internal Feedforward Cap V+ to V- and Integrator to Output
AD530	V+	Multiplier Output Amplifier Integrator Refers to V+
AD532	V+	Multiplier Output Amplifier Integrator Refers to V+
AD533	V+	Multiplier Output Amplifier Integrator Refers to V+
AD534	V-	Output Amplifier
AD535	V-	Output Amplifier
AD536A, AD636	V-, V+, Common	External Integrator to V+, Internal Feedforward V- to Common
AD537	V-	Internal Buffer Amp
AD540	V-	
AD542, AD642	V-	
AD544, AD644	V-	

	Internal Integrator Referred To:	Comments
AD545	V-	
AD547, AD647	V-	
AD559	V-, Common	DAC Control Loop Integrator Referred Between V- and Common
AD561	V-, Common	DAC Control Loop Integrator and Ref. Amp Refer to Common Ref. Bias Amp Refers to V-
AD562	V-	DAC Control Loop Integrator Referred to V-. Reference Input Common to Control Loop Isolated from DAC Output Common
AD563	V-	DAC Control Loop Integrator Referred to V-. Reference Input Common to Control Loop Isolated from DAC Output Common
AD565	V-	DAC Control Loop Integrator Referred to V-. Reference Input Common to Control Loop Isolated from DAC Output Common
AD566	V-	DAC Control Loop Integrator Referred to V-, Reference Input Common to Control Loop Isolated from DAC Output Common
AD567	V-	DAC Control Loop Integrator Referred to V-, Reference Input Common to Control Loop Isolated from DAC Output Common
AD580	V-	
AD581	V-	
AD582	V-	
AD584	V-	
AD101A	V-	External Cap (Includes AD201A, AD301A, etc.)
AD108	V+	External Cap (Includes AD208, AD308, etc.)
AD741	V-	Internal Cap (Includes 741J, K, L, etc.)
HOS-050	V+	
ADLH-0032	V+	