elektronik-
mekanikerbranchen

kredsløbsopgaver

Maj 1984

Metalindustriens Svendeprøvekommissioner

97284

Metalindustriens Svendeprøvekommissioner

KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN

A 1. Diff.-forstærker
A 2. Diff.-forstærker med strømgen.
A 3. Emitterfølger og jordet emitter.
A 4. Swich mode powersupply.
A 5. Operationsforstærker.
A 6. RC-faseskift osc.
A 7. Transformatorløs udgangstrin.
A 8. Wien-bro osc.
A 9. Effekt forstærker.
A 10. Transformatorkoblet LF-forstærker.
A 11. SCR-regulering.
A 12. Stabiliseret spændingsforsyning.
A 13. Inverterende forstærker.
A 14. Ikke inverterende forstærker.
B 15. Komperator med hysterese.
B 16. Multivibrator med IC.
B 17. D/A-converter.
B 18. Monostabil MV.
B 19. 4 bits skifteregister.
B 20. Miller integrator.
B 21. Differentiering/delay.
B 22. Schmitt-trigger.
B 23. R-S flip flop.
B 24. Bistabil MV.
B 25. Intergreret tæller.
B 26. DC/AC/DC-converter.
B 27. Intergration.
B 28. Astabil MV.
B 29. Multiplexet display.
B 30. Acyncron decadetæller.
B 31. Syncron decadetæller.
B 32. Koblingsmåder for NE 555.
C 33. Blandertrin.
C 34. Krystalstyret osc. med ALC-regulering.
C 35. MF-forstærker.
C 36. HF-forstærker og blander.
C 37. Jordet basis + additiv blandertrin.
C 38. HF-forstærker og blander.
C 39. PA-trin.
C 40. Usymmetrisk foster seeley detektor.
C 41. Bredbåndsblander.
C 42. AGC-reguleret forstærker.
C 43. VCO-osc.
C 44. MF-forstærker.
C 45. Bottler osc.
C 46. Fasemodulator.
C 47. Diode begrænser.
C 48. HF-forstærker.
C 49. X-tal osc.
C 50. Bal. blander.
C 51. Forholdsdetektor.
C 52. AGC-forstærker.

Virkemåder af ovennævnte kredsløb skal forklares af eksaminanden.
Det skal bemærkes, at på de diagramudsnit hvor der er fortaget "indstipling", skal hovedvægten af overhøringen lægges på den del af diagramudsnittet der er indstiplet.

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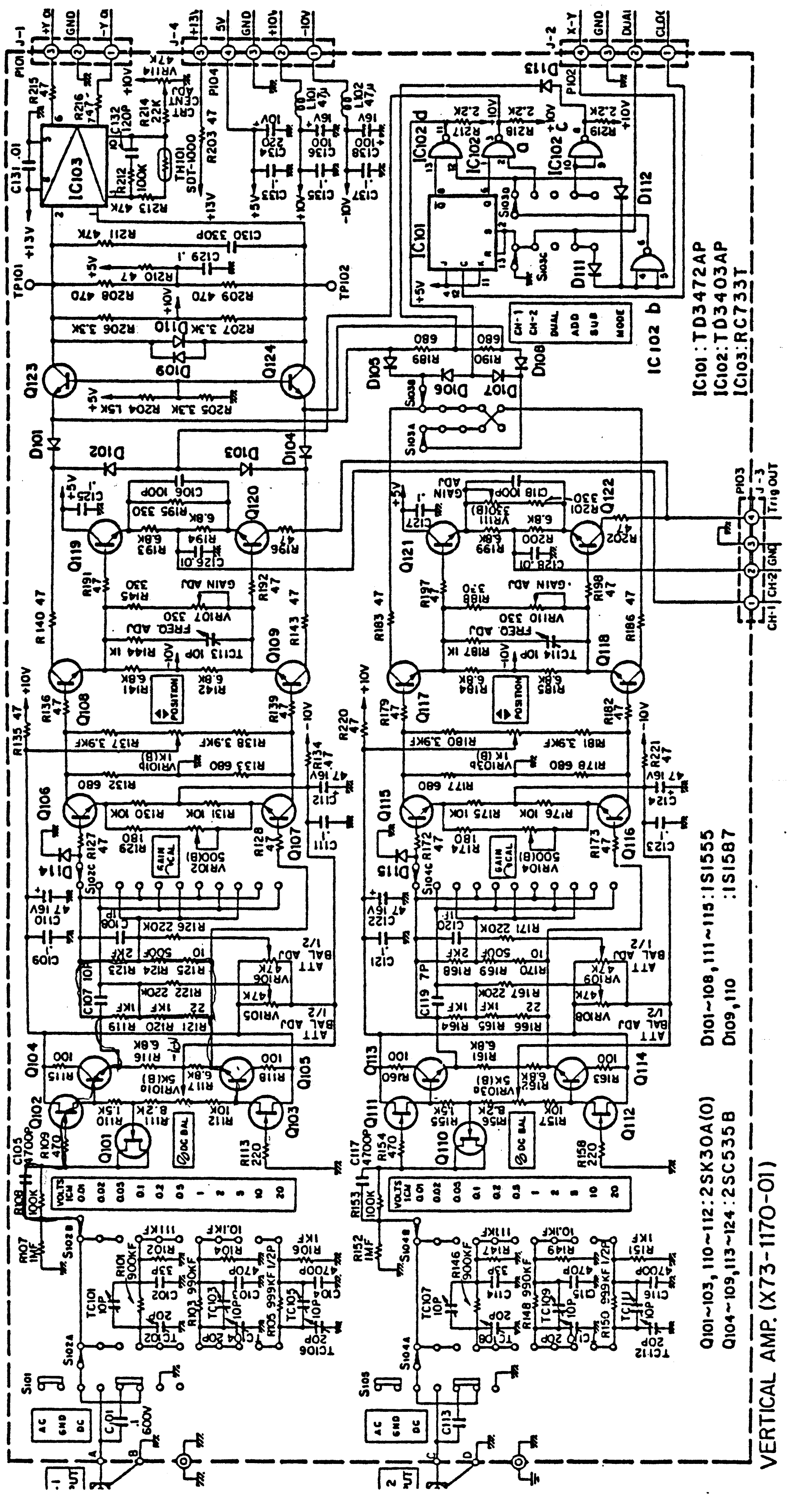
A 1

KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN



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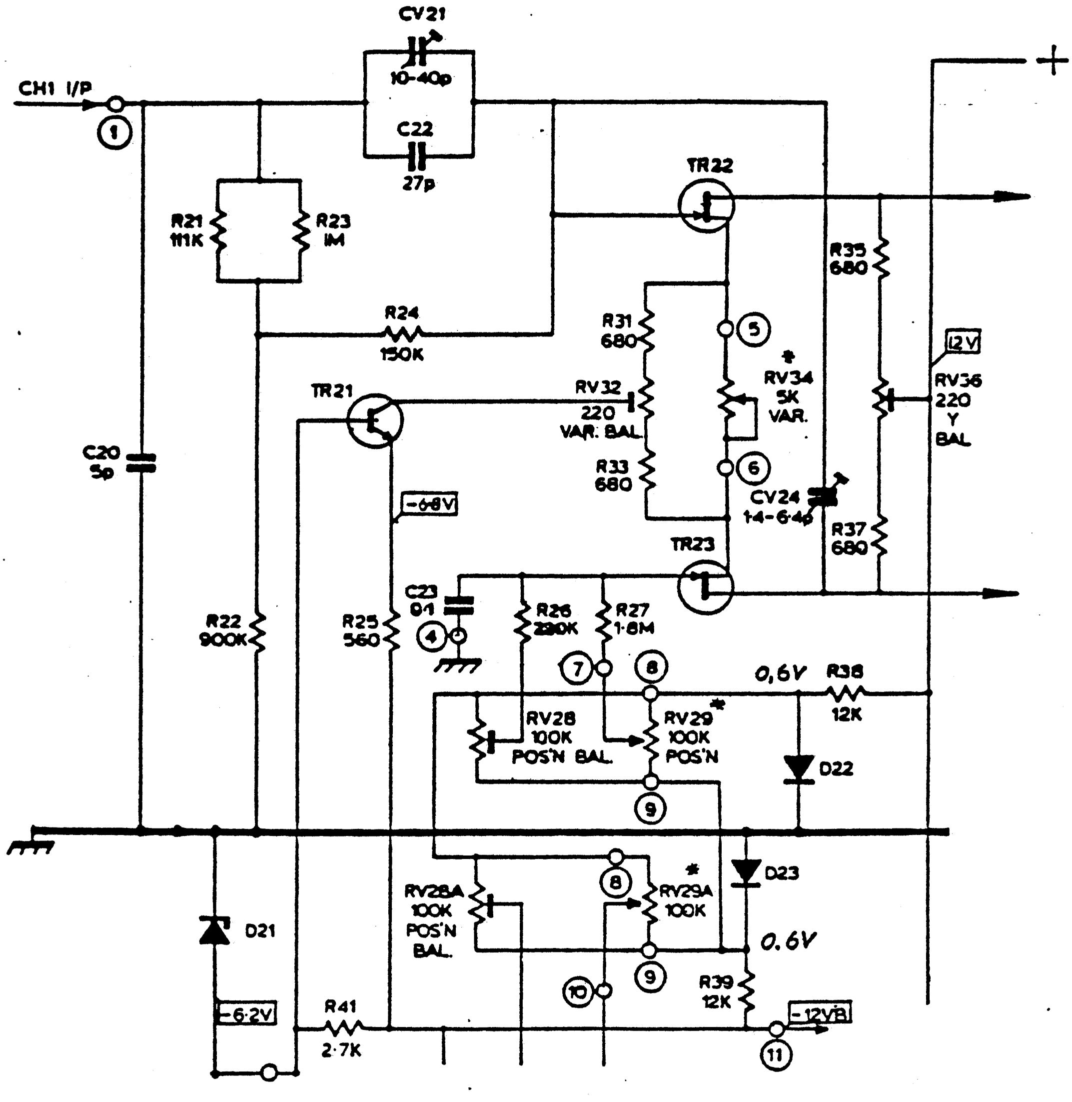
A 2

KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN



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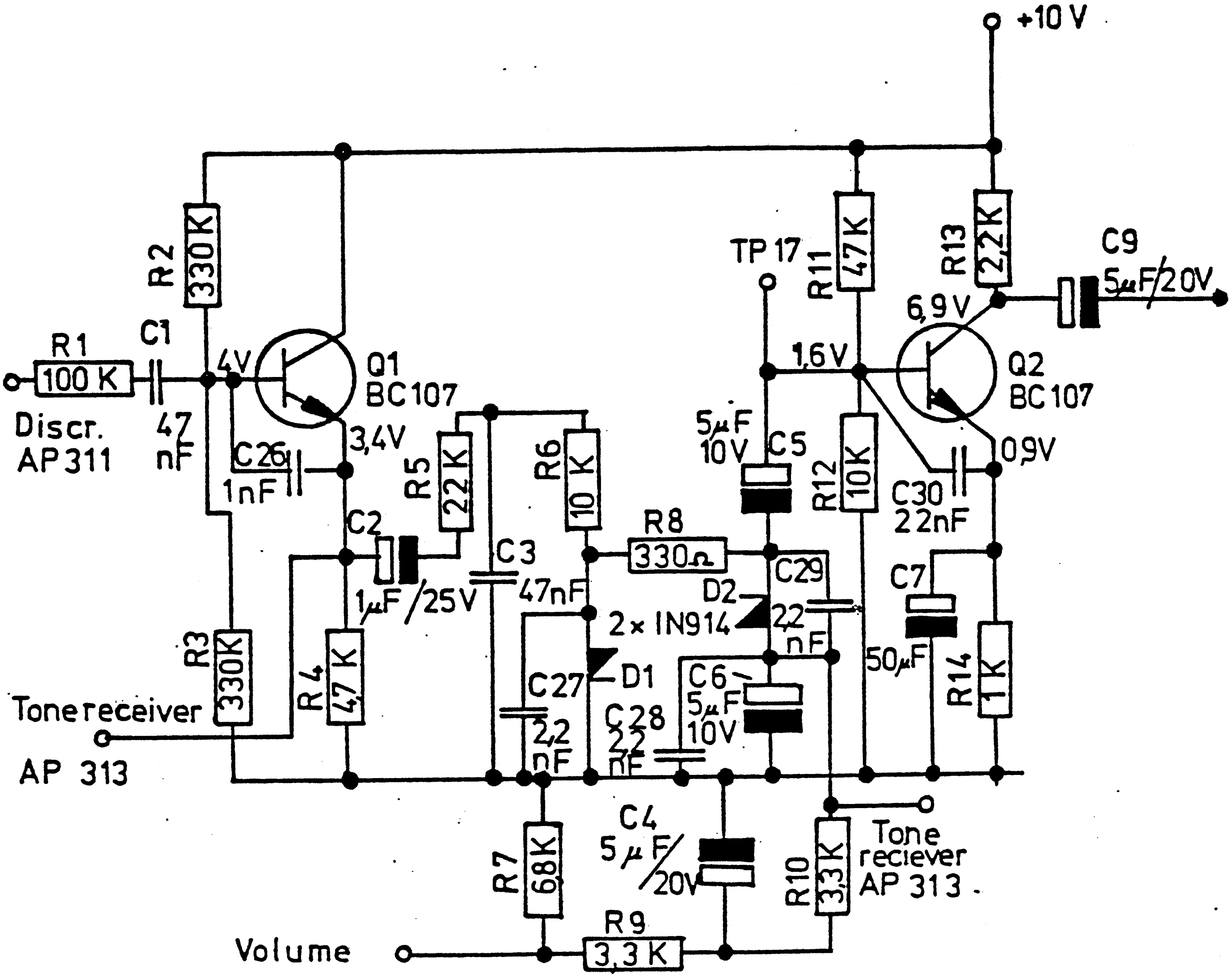

+10 V
R2
330K
R1
100 K
C1
47
nF
4V
Q1
BC107
Discr.
AP311
3,4V
C26
1nF
R5
22 K
R6
10 K
C2
1μF/25V
C3
47nF
R8
330Ω
TP 17
R11
47K
R13
2,2K
C9
5μF/20V
6,9V
1,6V
Q2
BC107
5μF
10V
C5
R12
10K
C30
22nF
0,9V
C7
50μF
R14
1K
C29
22
nF
D2
2× IN914
D1
C27
2,2
nF
C28
22
nF
C6
5μF
10V
R3
330K
R4
4,7 K
Tonereceiver
AP 313
C4
5μF
20V
R7
68K
R10
3,3K
Tone
reciever
AP 313
R9
3,3 K
Volume

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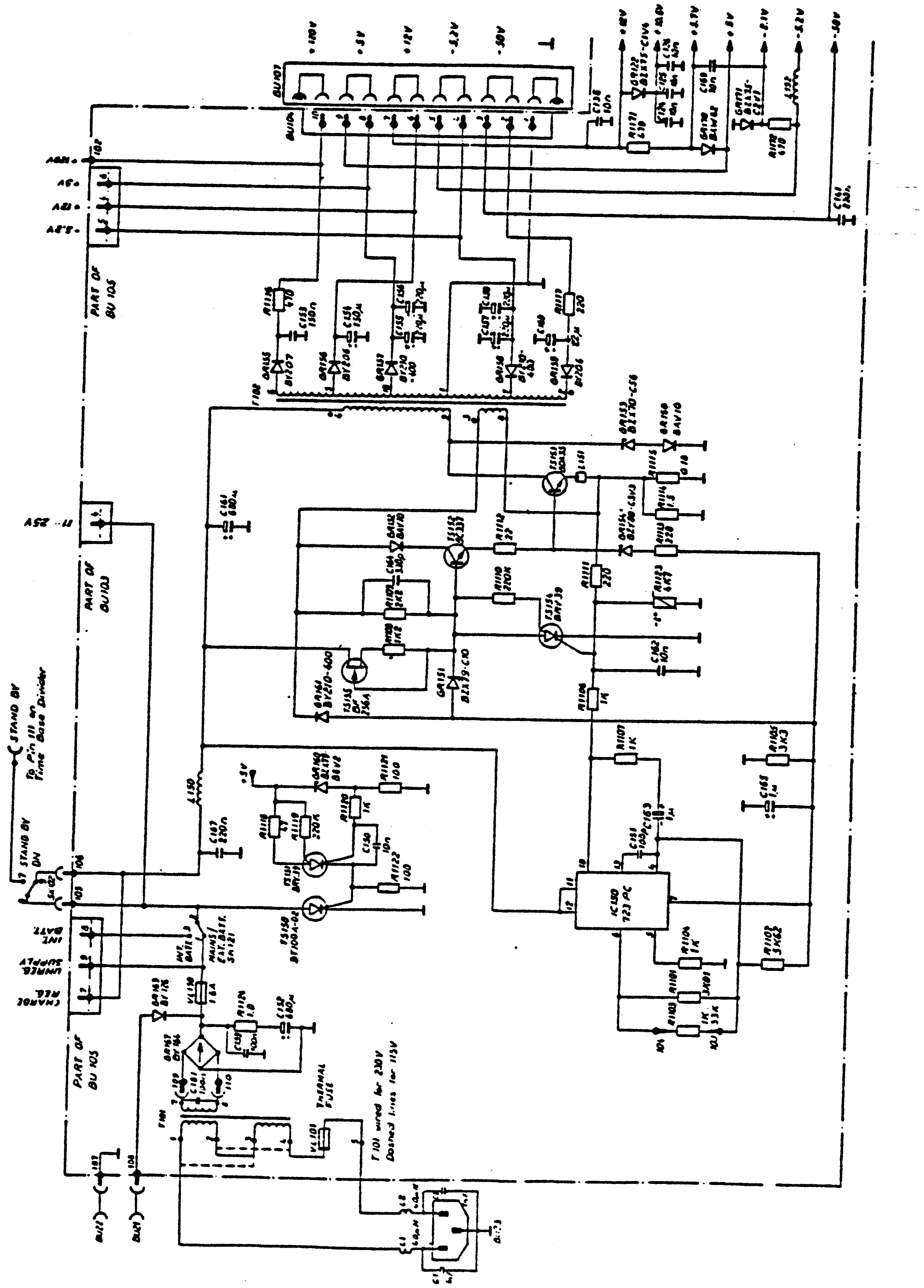

PM 66 12

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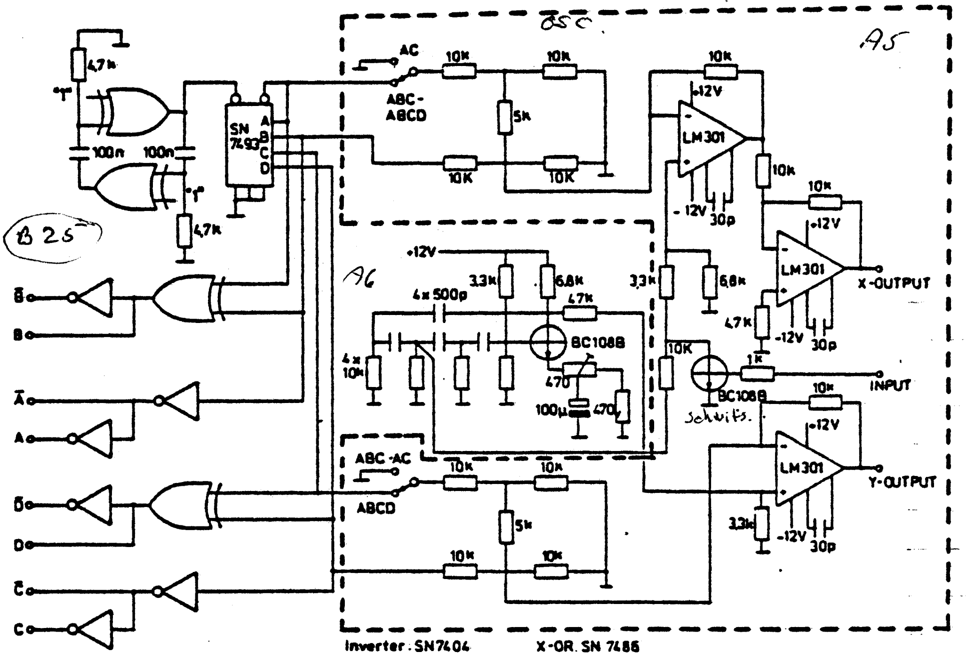
Karnov generator.

Rød læremiddel 16-tæller

RC faseskift



'93A, 'L93, 'LS93 . . . 4-BIT BINARY COUNTERS

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'L90	20 mW
'LS90	45 mW
'92A, '93A	130 mW
'LS92, 'LS93	45 mW
'L93	16 mW

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, 'L90, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, 'L93, and 'LS93.

All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

'93A, 'L93, 'LS93
COUNT SEQUENCE
(See Note C)

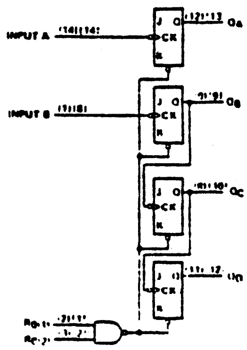
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

'92A, 'LS92, '93A, 'L93, 'LS93
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

'93A, 'L93, 'LS93

('93A), L93)



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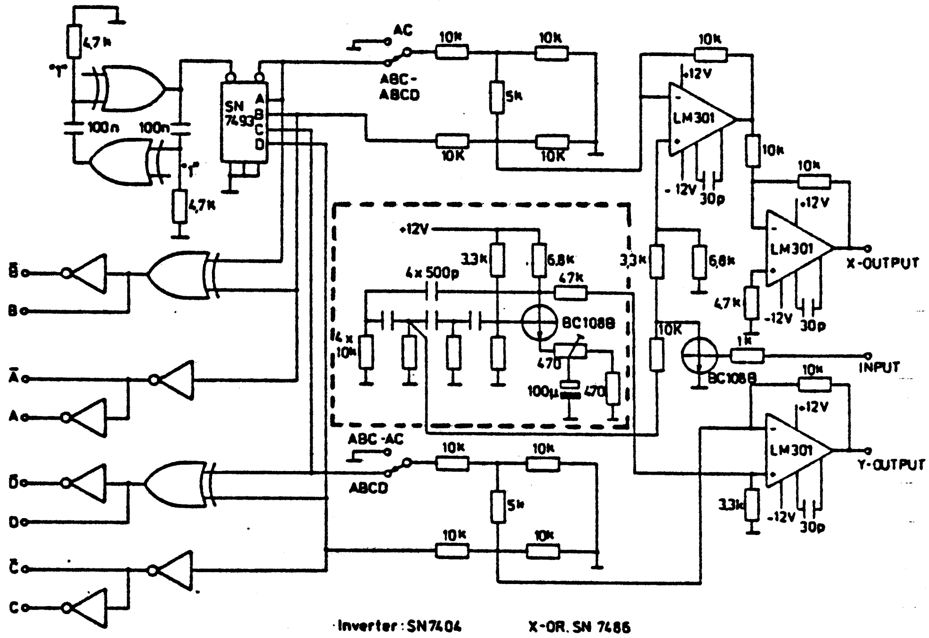

Inverter: SN7404 X-OR. SN 7486

'93A, 'L93, 'LS93 . . . 4-BIT BINARY COUNTERS

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'L90	20 mW
'LS90	45 mW
'92A, '93A	130 mW
'LS92, 'LS93	45 mW
'L93	16 mW

description

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All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

'93A, 'L93, 'LS93
COUNT SEQUENCE
(See Note C)

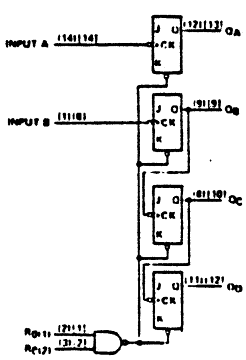
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

'92A, 'LS92, '93A, 'L93, 'LS93
RESET/COUNT FUNCTION TABLE

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	OUTPUT Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

'93A, 'L93, 'LS93

('93A) ('L93)



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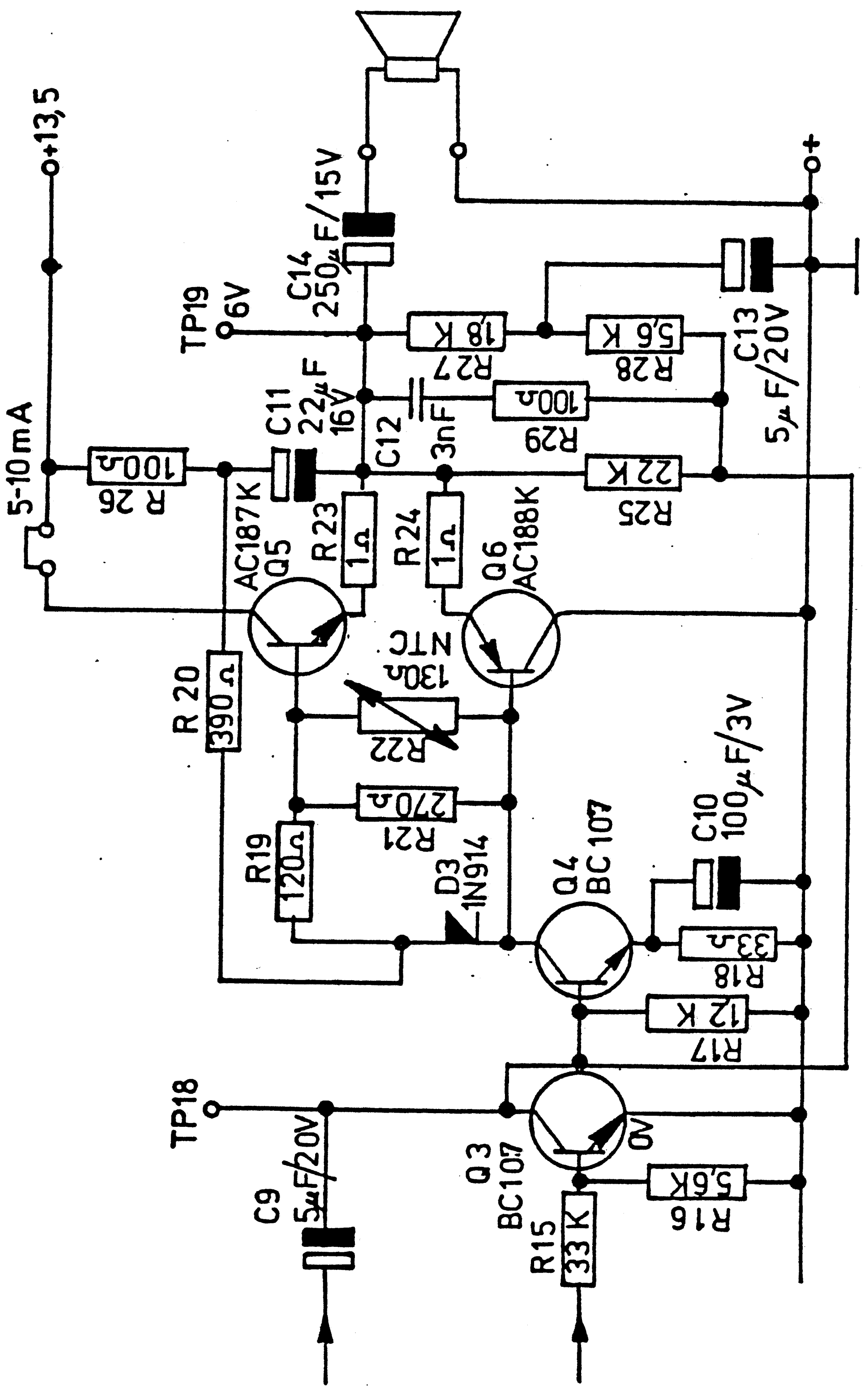
KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN



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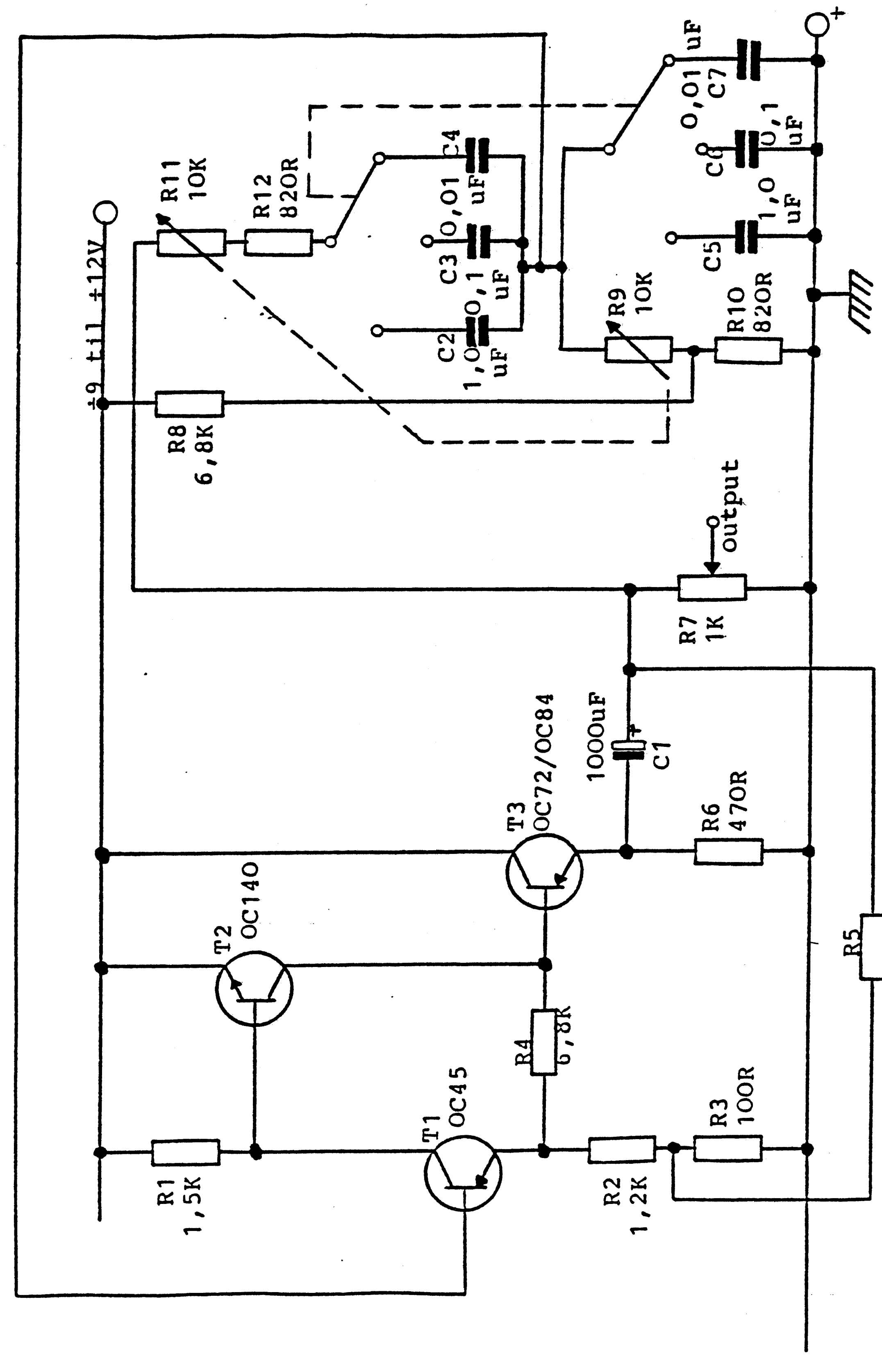
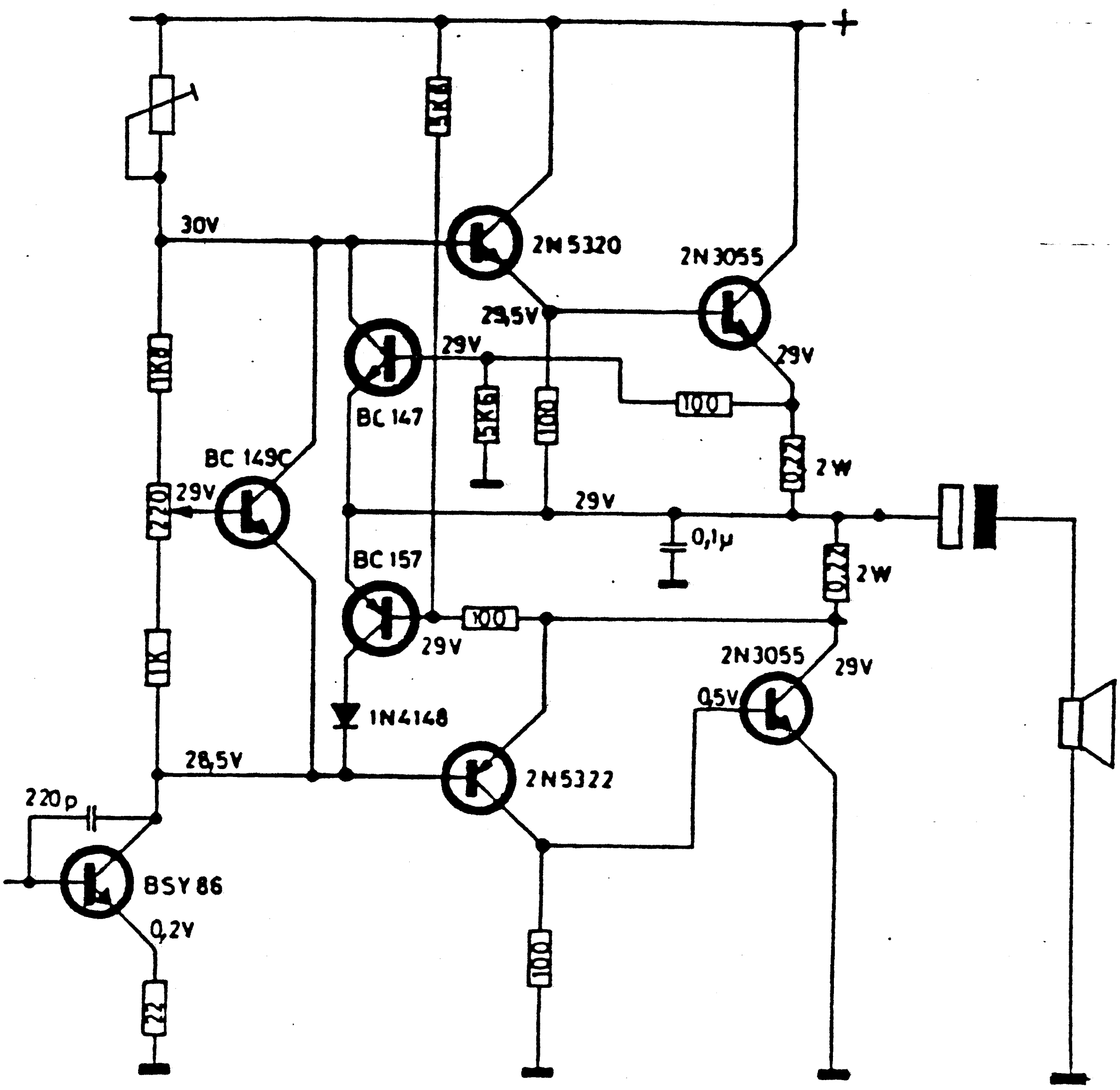
KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN



37354


+
30V
2N5320
2N3055
29,5V
29V
BC 147
5K6
100
BC 149C
29V
2W
0,1µ
BC 157
1K
1N4148
28,5V
2N5322
0,5V
220p
BSY 86
0,2V
22

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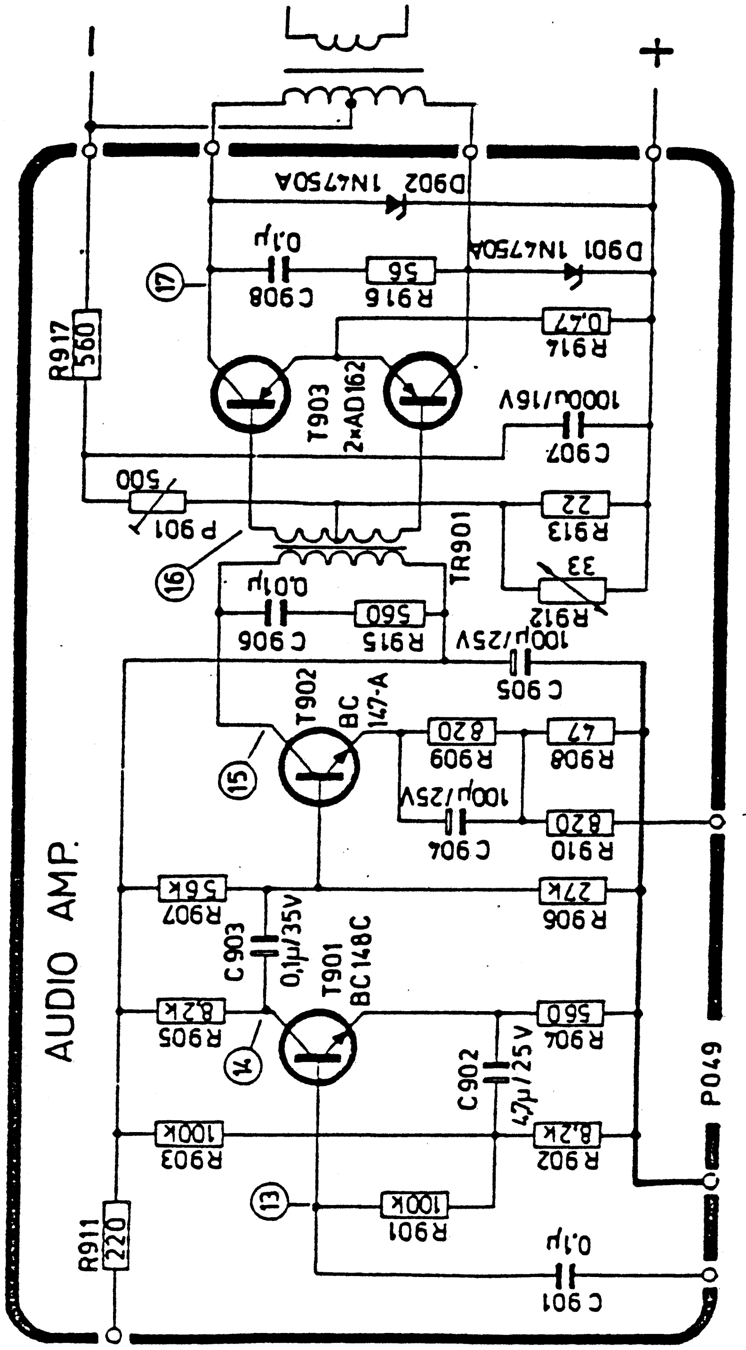
KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN



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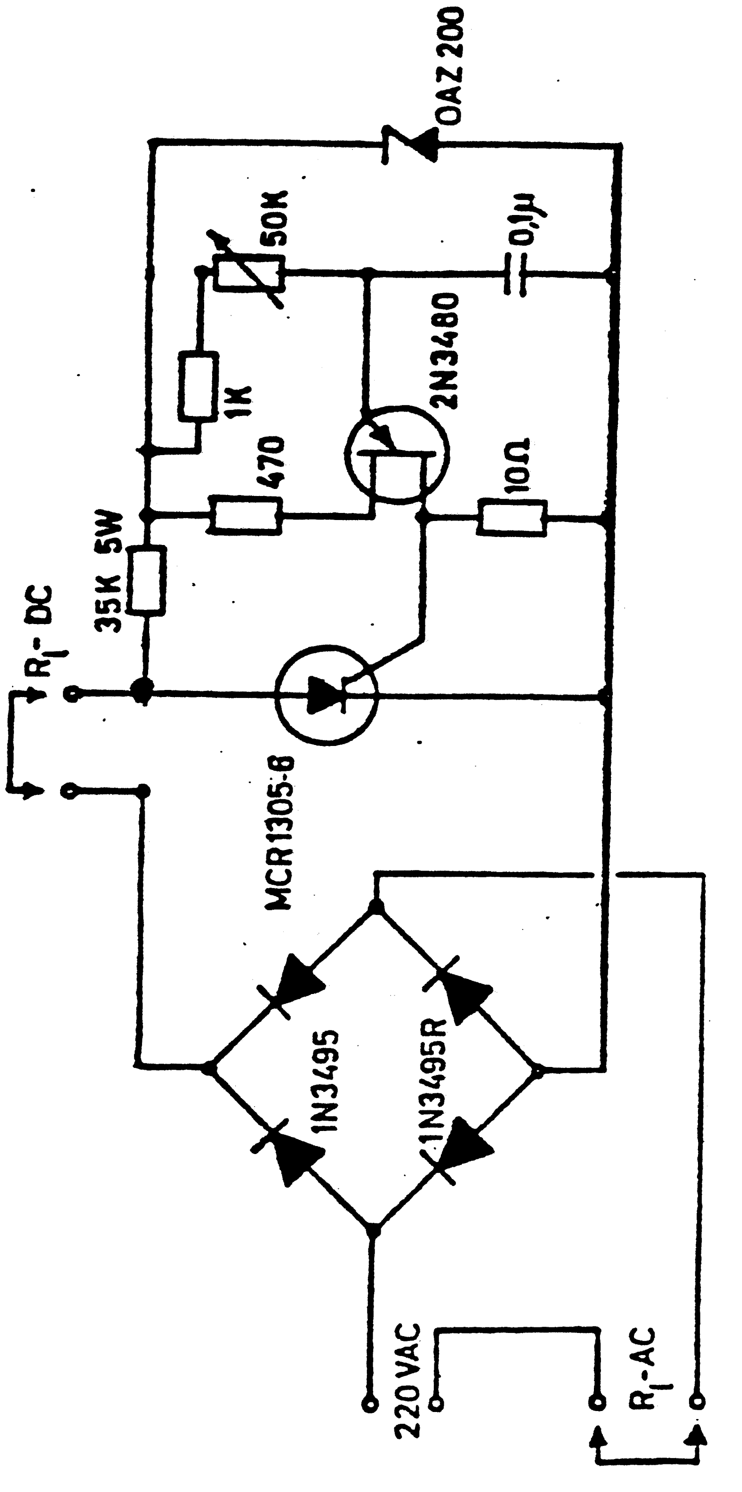

OAZ 200
50K
0,1μ
1K
2N3480
470
10Ω
35K 5W
R1- DC
MCR1305-6
1N3495
1N3495R
220 VAC
R1-AC

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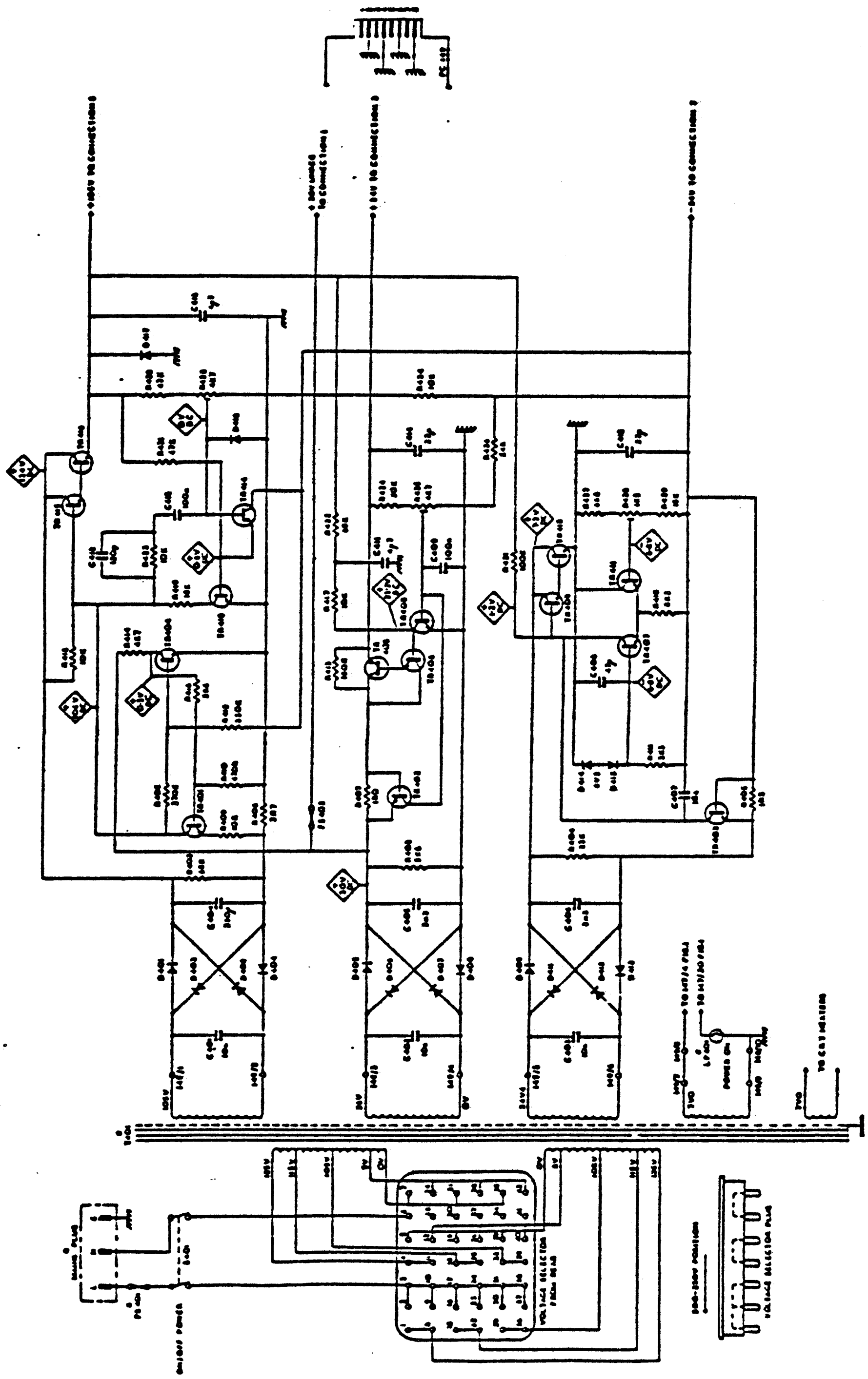

Telego. D75

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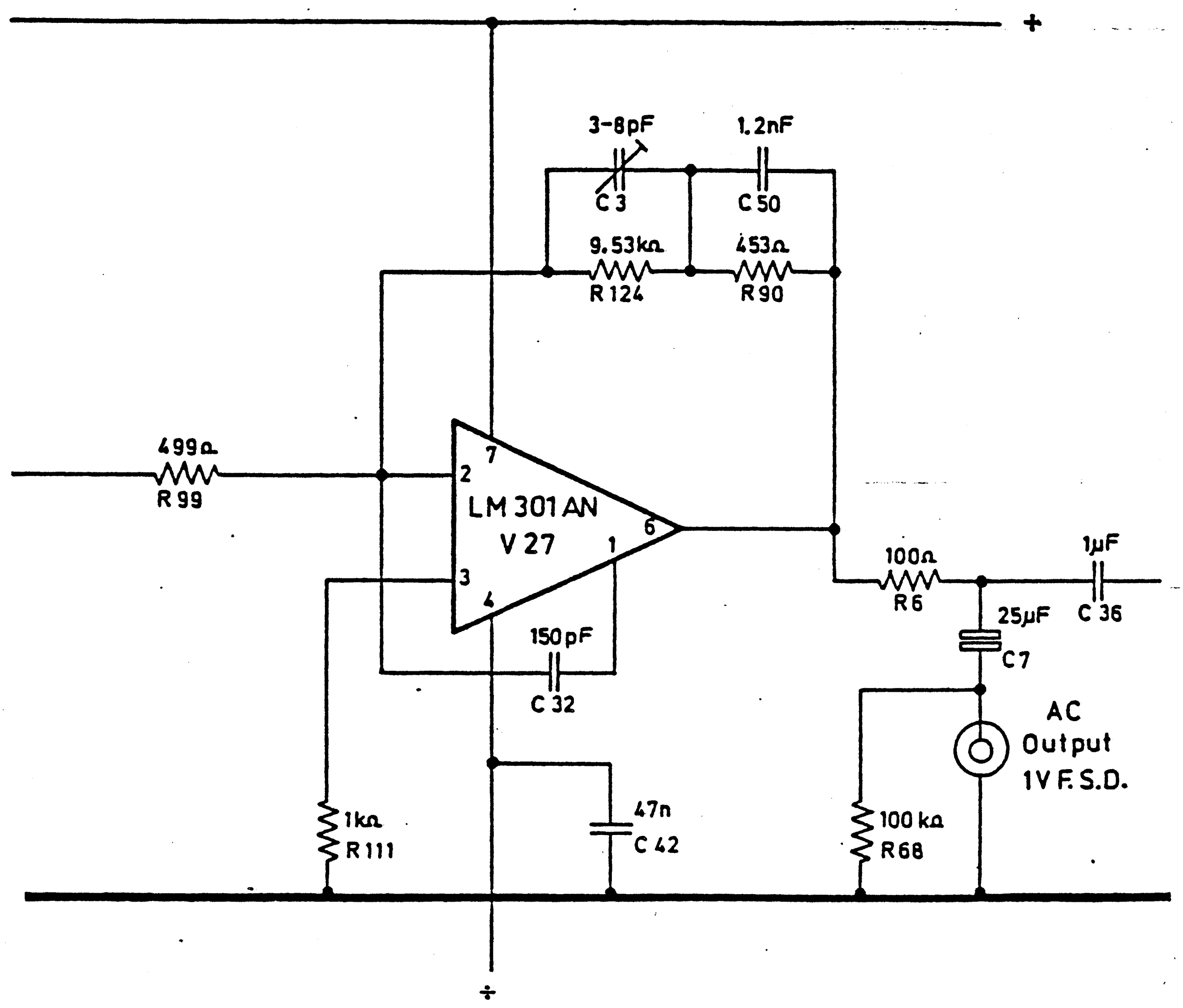
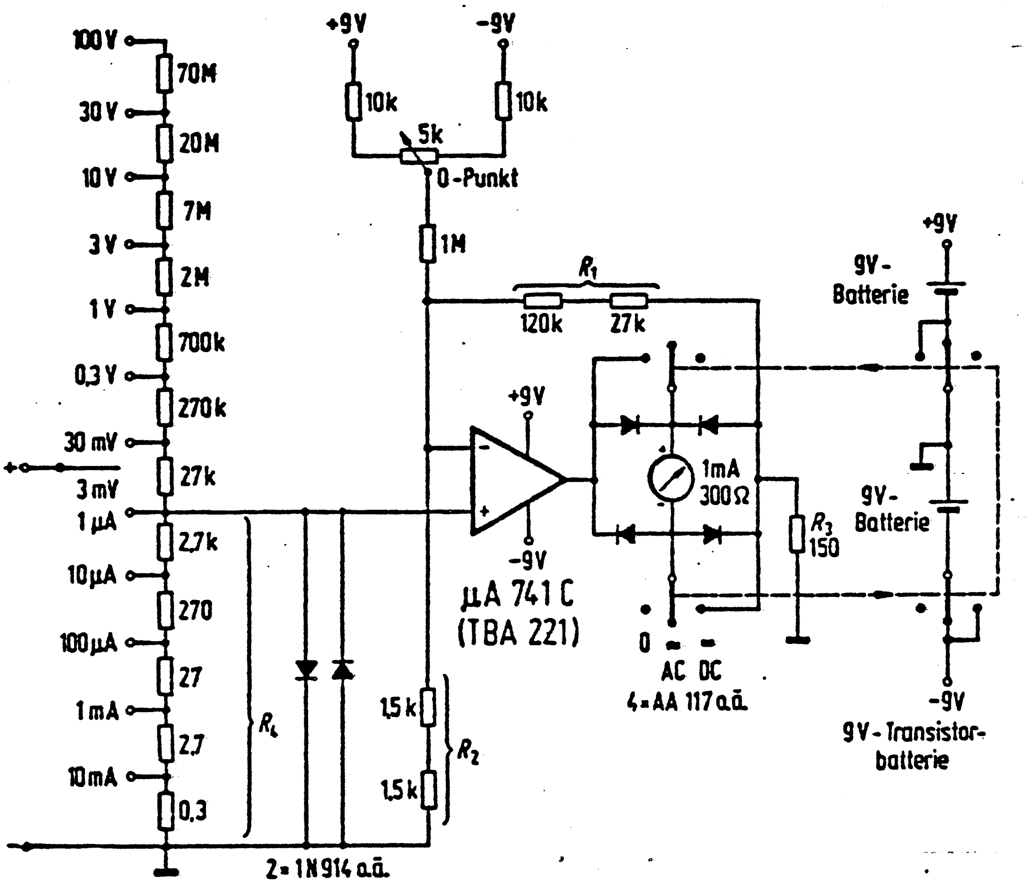
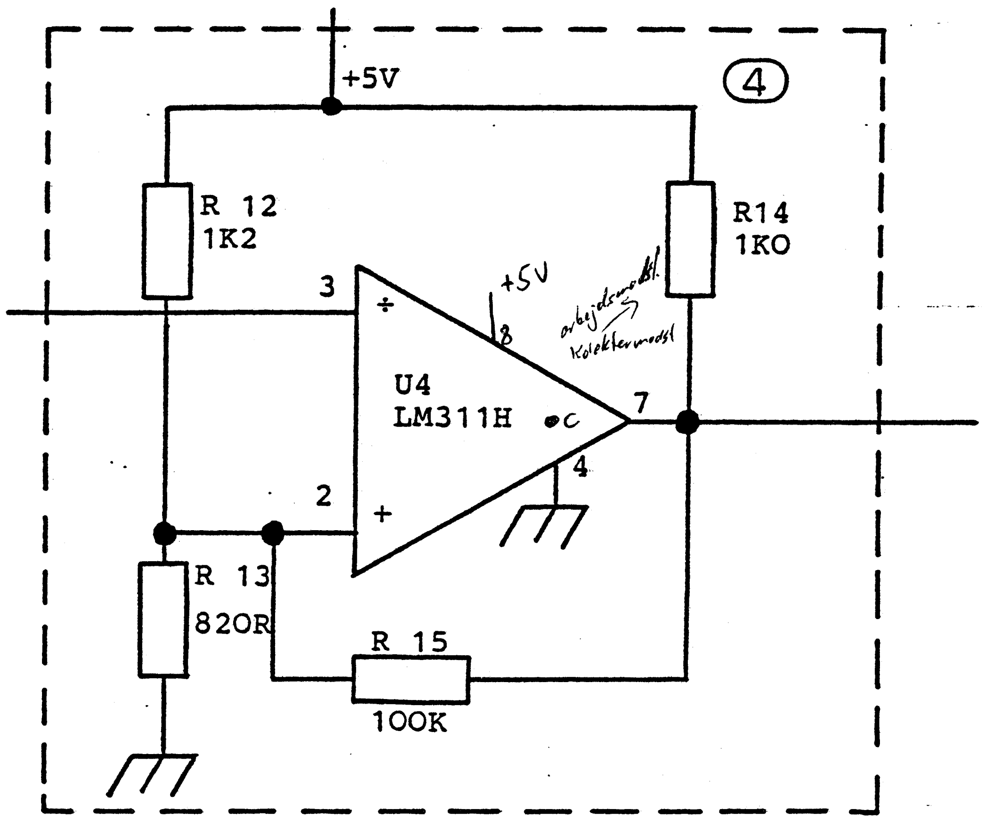
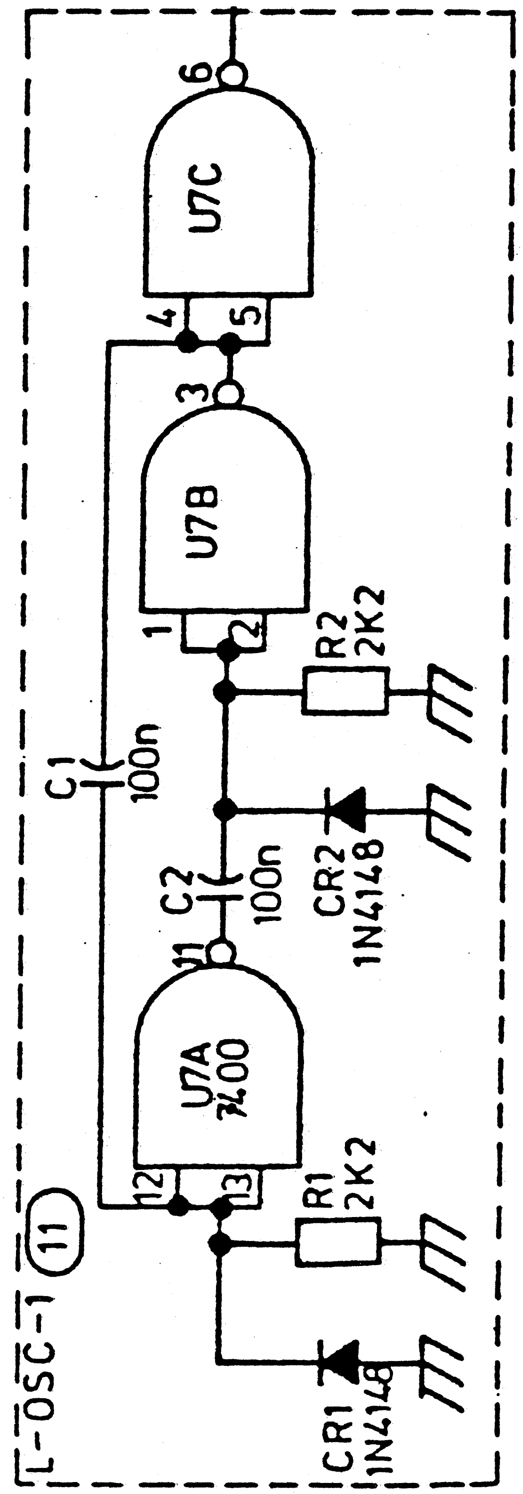

+
3-8pF
C 3
1.2nF
C 50
9.53kΩ
R 124
453Ω
R 90
499Ω
R 99
7
2
LM 301 AN
V 27
6
1
3
4
150pF
C 32
100Ω
R 6
1µF
C 36
25µF
C 7
AC
Output
1V F.S.D.
1kΩ
R 111
47n
C 42
100 kΩ
R 68
÷


100 V
70M
30 V
20M
10 V
7M
3 V
2M
1 V
700k
0,3 V
270k
30 mV
27k
3 mV
1 µA
2,7k
10 µA
270
100 µA
27
1 mA
2,7
10 mA
0,3
R_L
2 = 1N914 o.ä.
+9V
-9V
10k
10k
5k
0-Punkt
1M
R_1
120k
27k
+9V
-9V
µA 741 C
(TBA 221)
1,5 k
1,5 k
R_2
1mA
300Ω
R_3
150
0
AC
DC
4 = AA 117 o.ä.
9V-
Batterie
9V-
Batterie
9V - Transistor-
batterie

Comperator





kan anvendes til øvelse i A-trin

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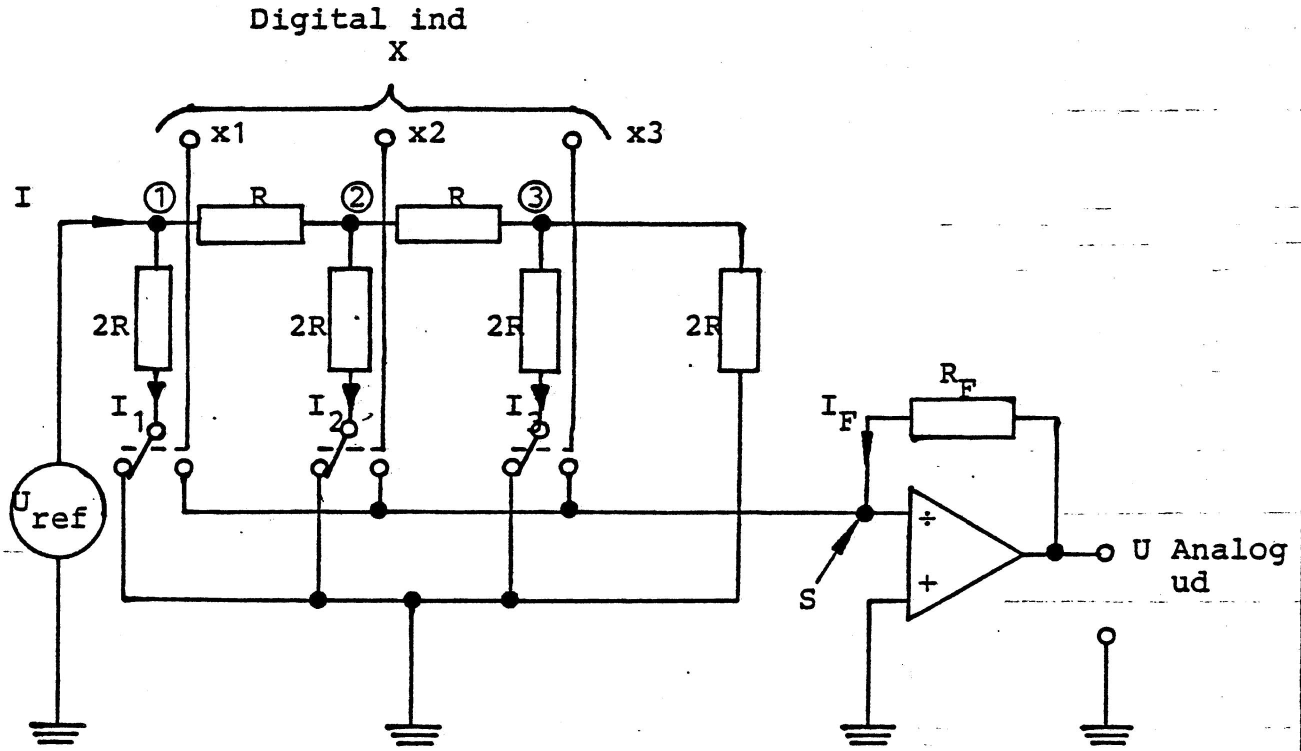
Digital ind
X
x1
x2
x3
I
①
②
③
R
R
2R
2R
2R
2R
I1
I2
I3
Uref
RF
IF
÷
+
S
U Analog
ud

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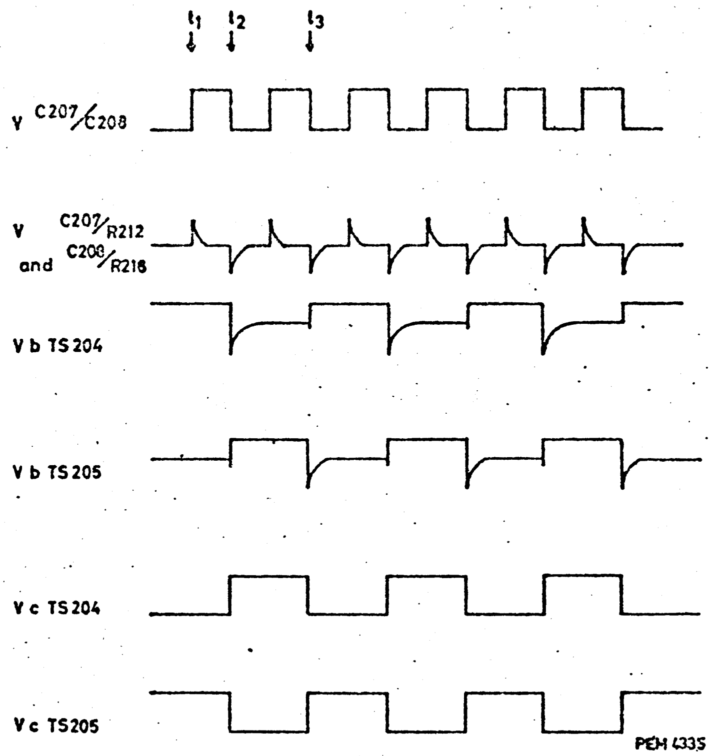


Fig. II-3. Working principle line information generator

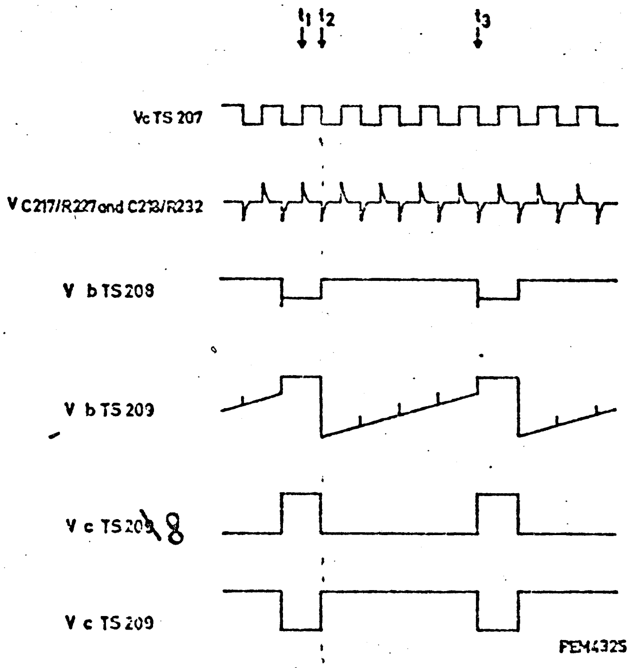


Fig. II-4. Working principle line blanking generator

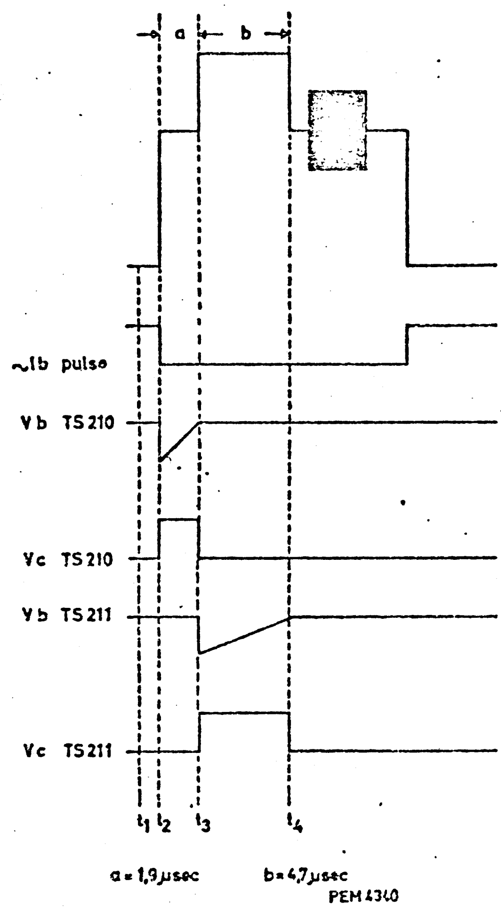


Fig. II-5. Working principle line sync. generator

Line blanking generator – Unit 2a (see Fig. II-2)

The generator for line blanking pulses is a 5 : 1 divider consisting of TS208 and TS209.
The drive pulses for the generator are differentiated by C217/R227 and C218/R232 successively.
Diodes GR206 and GR207 only pass on the negative part of the differentiated pulse to the base of TS208 and TS209.
The working principle of the generator is shown in Fig. II-4.
At moment t_1 e.g. TS208 is cut off and consequently TS209 is saturated.
At moment t_2 a negative-going drive pulse drives TS209 into cut-off via GR207.
The positive-going pulse on the collector of TS209 will drive TS208 into saturation via R230/C216.
The negative step on the collector of TS208 will charge C215 via GR205 so that a high negative voltage appears on the base of TS209.
TS209 is cut off until C215 is so far discharged via R229 that the positive pulses applied via GR206, TS208 and GR205 can drive TS209 into saturation again (moment t_3).
GR205 and C216 ensure that the line blanking pulses have the correct rise time.

Line sync. generator – Unit 2a (see Fig. II-2)

This generator consists of the two pulse delay circuits C219, R234, TS210 and C220, R236, TS211.
RC circuit C219, R234 provides a delay time "a" (1.9 μs) (see Fig. II-5) which corresponds to the front porch.
C220, R236 determines the width of the line sync. pulse ("b" = 4.7 μs).
The working principle is shown in Fig. II-5.
With no signal on their bases TS210 and TS211 are in saturation (moment t_1). This is due to the + 6 V via R234 and R236.
At moment t_2 the (negative-going) leading edge of the "~ lb" pulse will cut off TS210 and charge C219 to a negative value (current towards the base).
The positive-going pulse in the collector of TS210 will have a width determined by the discharge time of C219 via R234 (internal $t_2 \ldots t_3$).
At moment t_3 the negative-going trailing edge of the pulse from the collector of TS210 will cut off TS211.
The cut-off time and thus the width of the line sync. pulse ("ls") at the collector of TS211 depends on the discharge of C220 via R236 (time t_4).

Colour bar generator – Unit 2b (see Fig. II-6)

The colour bar generator consists of a divider formed by three identical series-coupled flip-flops (TS212 . . . TS217).
Each of these circuits divides the applied "~a" signal by two.
Diodes GR222, GR223 and GR224 form an AND gate which, via TS219, will short circuit the applied "~a" signal when the output voltages of the three flip-flops to the diodes all are + 6 V.
The working principle of the colour bar generator is shown in Fig. II-7.
At moment t_1 the three flip-flops are set by means of differentiated line blanking pulses (applied via GR216).
As a result the voltages to the three diodes of the AND gate will become 0 V, and TS219 is driven into cut-off.
The "~a" pulses can affect circuit TS212-TS213 during interval t_1-t_3. The dividing process starts at moment t_2 and goes on, as indicated, till moment t_3 when all diode voltages are + 6 V.
The "~a" signal is short circuited via TS 219, and counting stops.
At the trailing edge of the next line blanking pulse, time t_1 is reached again, and the process is repeated.
During the frame blanking period the generator is stopped. This is achieved by means of the "fb" pulses which, via GR 217 and GR220, will drive TS218 into saturation during the blanking period. The setting pulses ("lb") are consequently short circuited, and the generator is stopped.
In test pattern "PHASE" the signals from the colour bar generator are only used every second line in the lower part of the pattern (from line 169 to line 288).
The drive signal to the generator is in this test pattern obtained by means of signals "312 l" and "2 l" which are applied to AND gate GR218/GR219.
The signal from the gate drives TS218 into saturation every second line in the lower part of the test pattern.
As a result the setting pulses ("lb") are short circuited, and the generator is stopped for these periods.

II. CIRCUIT DESCRIPTION

A. POWER SUPPLY – UNIT 1 (see Fig. II-1)

The power supply delivers stabilized voltages of + 6 V and — 6 V.
The stabilizing circuit for + 6 V consists of transistors TS101 and TS1, and Zener diode GR102.
The circuit for — 6 V is similar to that for + 6 V. It consists of TS102, TS2, and Zener diode GR103.
Stabilization is obtained as follows:
The emitter voltages of TS101 and TS102 are kept constant with respect to + 6 V and — 6 V. This is effected by means of Zener diodes GR 102 and GR103.
The base voltages of TS101 and TS102 are kept at 0 V.
If, for example, + 6V increases, the voltage on the base of TS101 will decrease with respect to the emitter voltage. Then the current in TS101 decreases. The base voltage, and the current in TS1 depend on the voltage division effected by R102 and TS101.
In this case the current in TS101 is reduced, and thus the base voltage of TS1 will become more positive (via R102) with respect to the emitter voltage.
The current in TS1 decreases, and the + 6 V voltage is restored to its nominal value.
The working of the — 6 V stabilization is similar to that of the + 6 V stabilization.
The power supply is also protected against short circuit. For instance, a short circuit between terminals 1 and 2 would cause the voltage on emitter TS102 to become 0 V. TS102, and consequently TS2 will be cut off, and the voltage at terminal 3 will be 0.
0 V at terminal 3 would, via R104, likewise drive TS101, and consequently TS1, into cut-off.
Both TS1 and TS2 are driven into cut-off, and the power supply is disconnected. The short circuit protection applies in the same way to short circuit between terminals 2 and 3.
An overload of one voltage will cause interruption of both voltages.

B. LINE INFORMATION – UNIT 2

Master oscillator – Unit 2a (see Fig. II-2)

TS201 and TS202 form an emitter-coupled LC oscillator. This oscillator operates as a master oscillator controlling the generators for sync. signals, line information, picture information, and the PAL switching pulses.
The oscillator frequency is 312.5 kHz.
The frequency is determined by L201, C203.

Pulse shaper – Unit 2a (see Fig. II-2)

The signal from the master oscillator is a sinewave. The following divider should be controlled by a squarewave signal to obtain stable triggering. Therefore it is necessary to convert the sinewave into a squarewave signal. This is effected in shaper TS203.
This transistor is cut off when no signal is applied to the base.
The applied signal has such a high amplitude that the positive half period will drive TS203 into saturation very fast.
The pulse obtained on the collector of TS203 is practically a squarewave.

Line information generator – Unit 2a (see Fig. II-2)

This generator supplies pulses "a′", "~a" and "~a′" giving the horizontal picture information ("a′" and "~a′") for the crosshatch and dot patterns, while pulse "~a") is used for controlling the colour bar generator.
The circuit, consisting of transistors TS204 and TS205, is a bistable multivibrator which divides the applied squarewave by two.
The control pulses from pulse shaper TS203 applied to the divider are differentiated in C207/R212 and C208/216 successively.
Diodes GR201 and GR202 ensure that only the negative part of the pulse can reach the base of TS204 and TS205.
The working principle of the generator is shown in Fig. II-3.
At moment t_1, before the first negative-going drive pulse arrives, e.g. TS204 is saturated so that its collector voltage will be low.
At the same time TS205 will be cut off, and its collector voltage will be high.
At moment t_2 a negative-going drive pulse is applied to the base of TS204 (GR202 not conducting) so that this transistor is cut off.
The positive pulse at the collector of TS204 drives TS205 into saturation.
At moment t_3 the process is repeated, only this time TS205 is driven into cut-off and, consequently, TS204 into saturation.
Capacitors C205 and C206 ensure that the generated pulses have the proper rise time.

2 : 1 Divider – Unit 2a (see Fig. II-2)

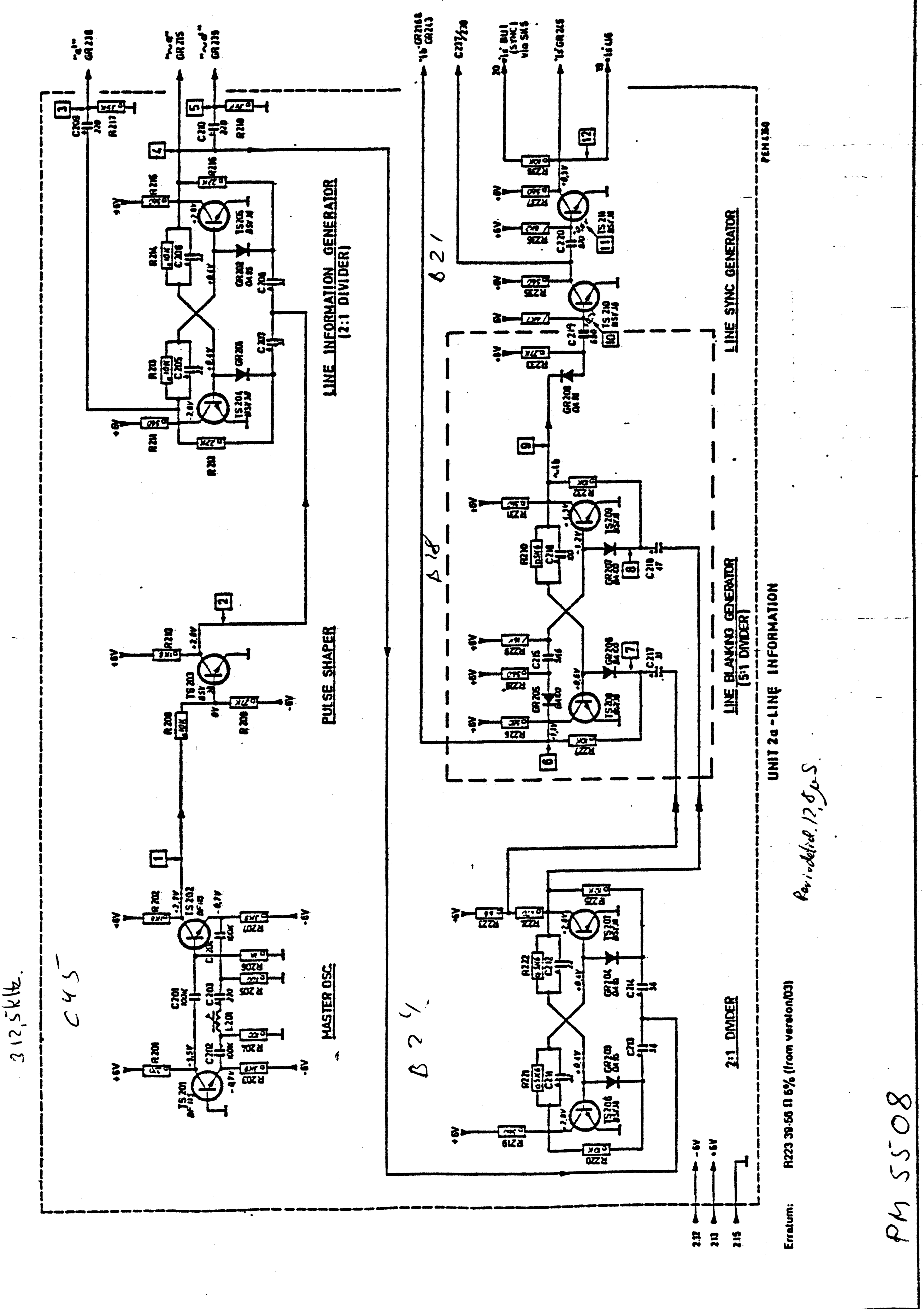
This generator consists of TS206 and TS207 which produces drive pulses for the "Line blanking generator". The divider is an astable multivibrator, and its working principle is the same as that of the "Line information generator".
The generated pulses have a frequency of:

$$\frac{156.25}{2}\,\text{kHz} = 78.125\ \text{kHz}.$$

Metalindustriens Svendeprøvekommissioner

B 18

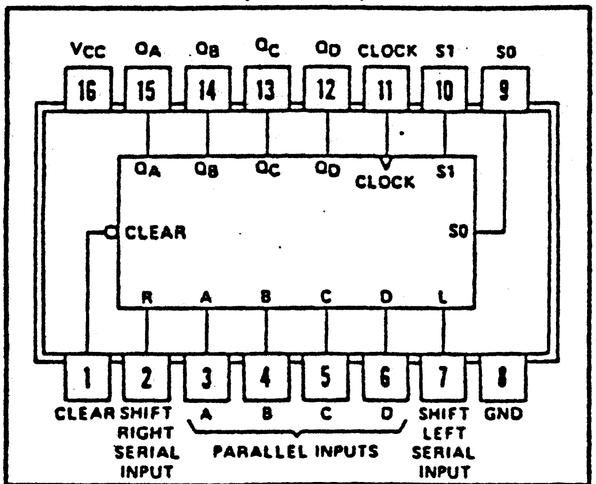
KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

BULLETIN NO. DL-S 7611866, MARCH 1974–REVISED OCTOBER 1976

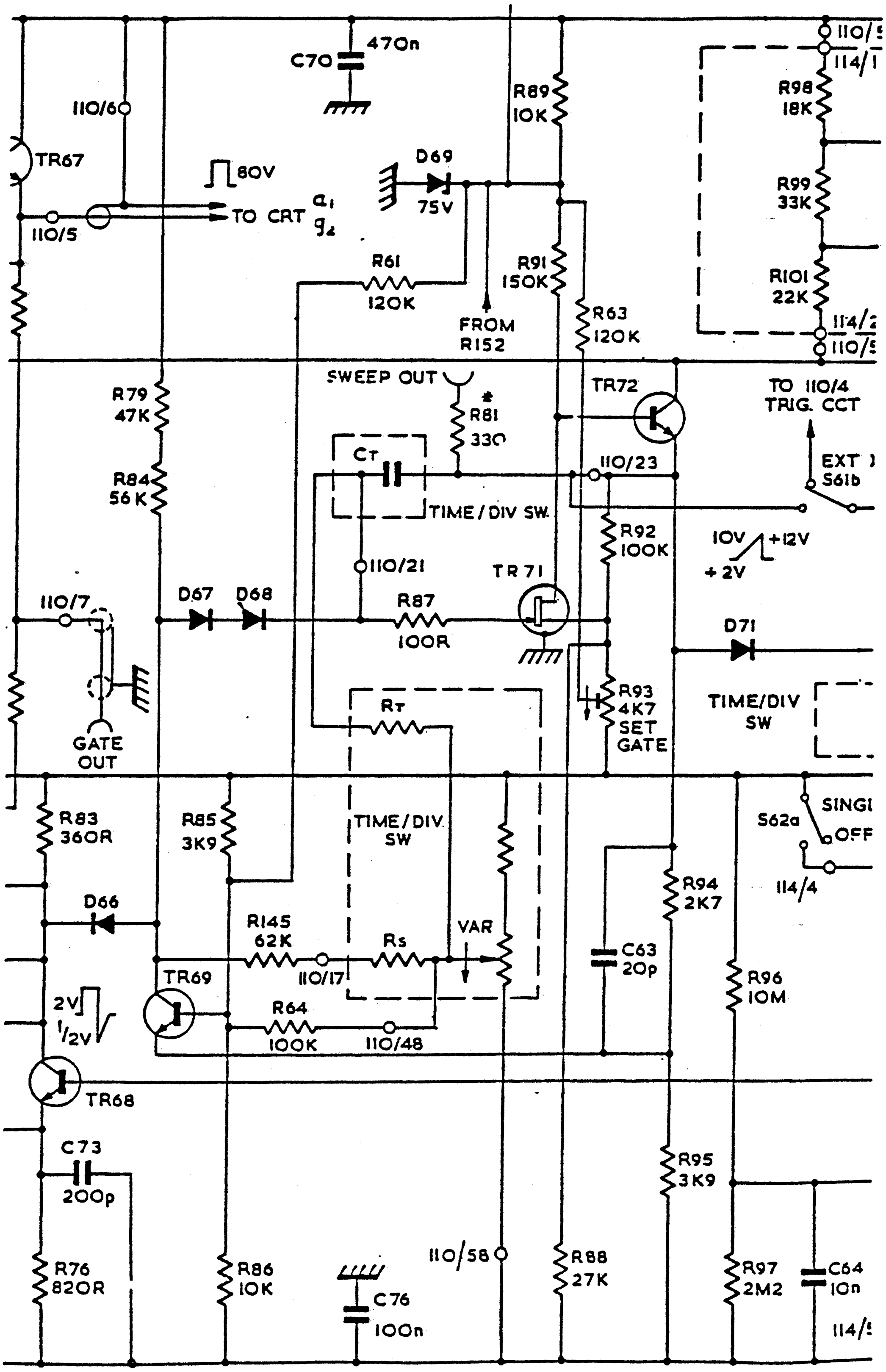
SN54194, SN54LS194A, SN54S194 . . . J OR W PACKAGE
SN74194, SN74LS194A, SN74S194 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

FUNCTION TABLE

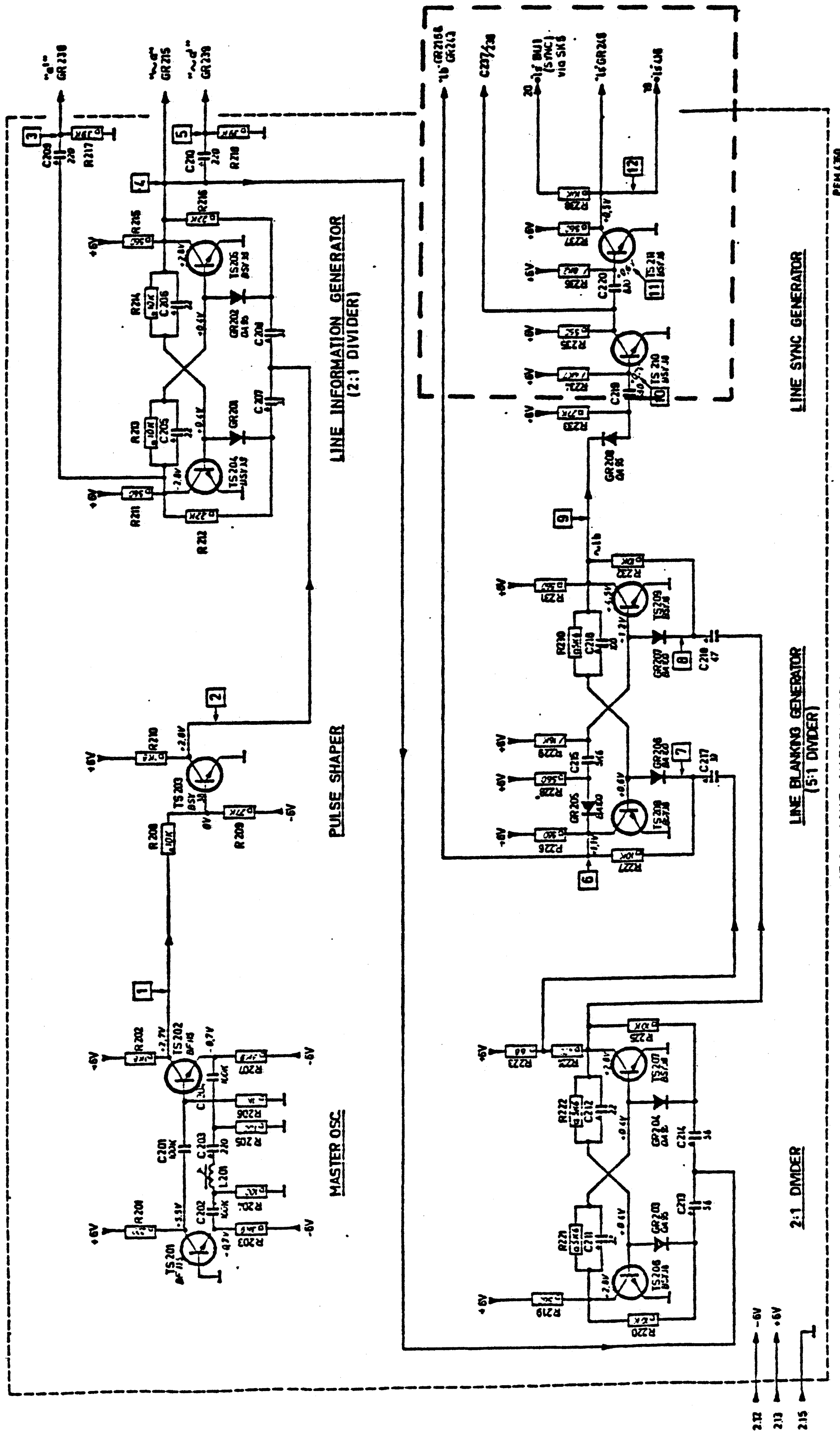
INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}



TIMEBASE X-AMP

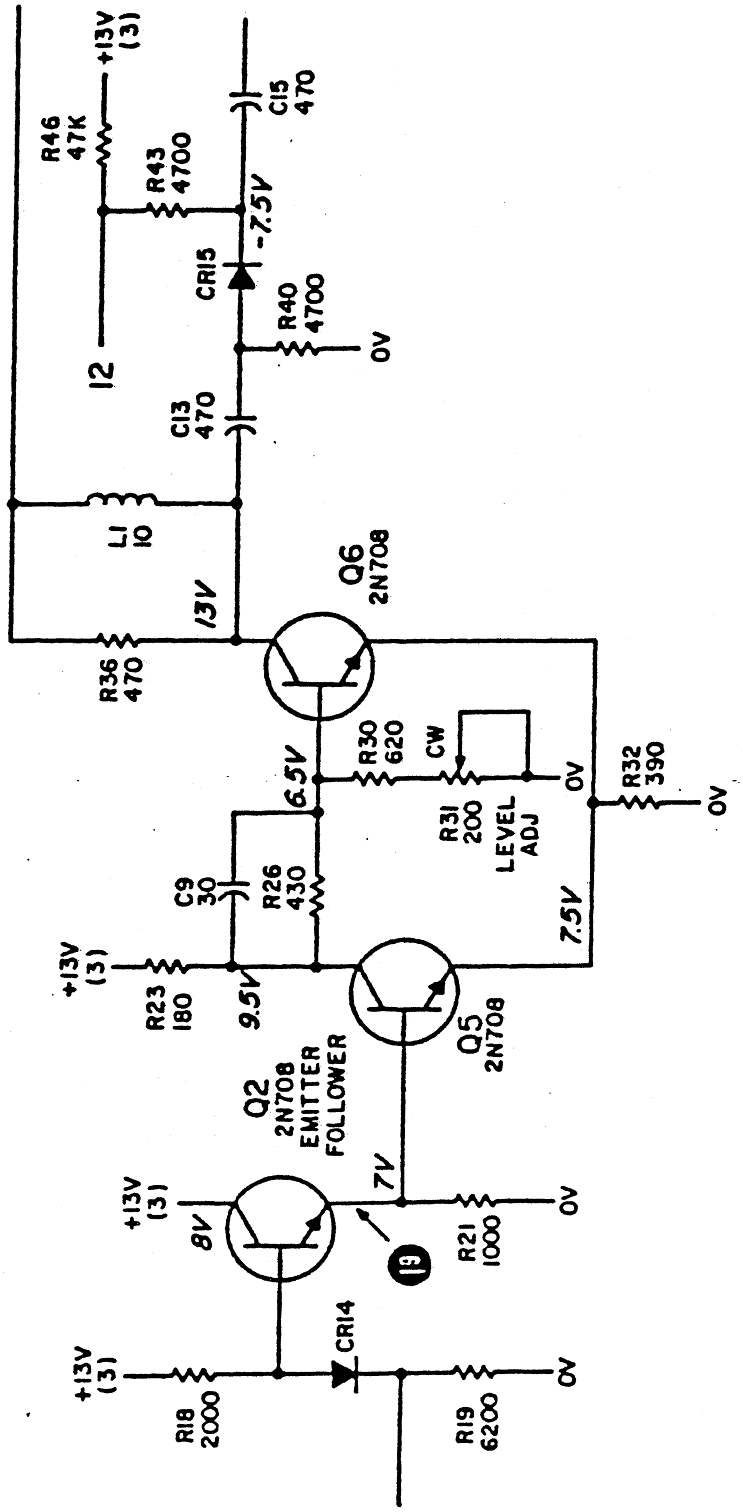
D65 ✓

37354



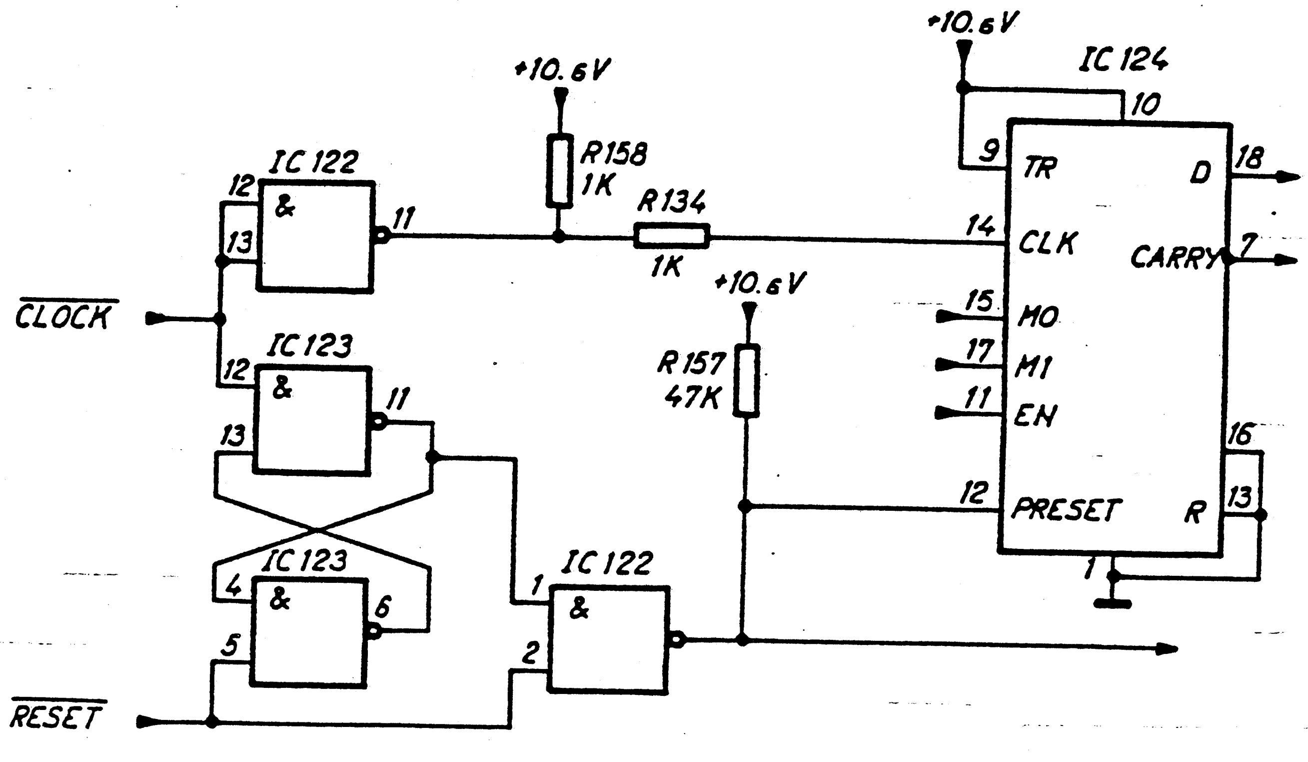
Erratum: R223 39-56 Ω 5% (from version 03)
R229 10-12 kΩ 5%
C215 8.2 nF 5%

37354

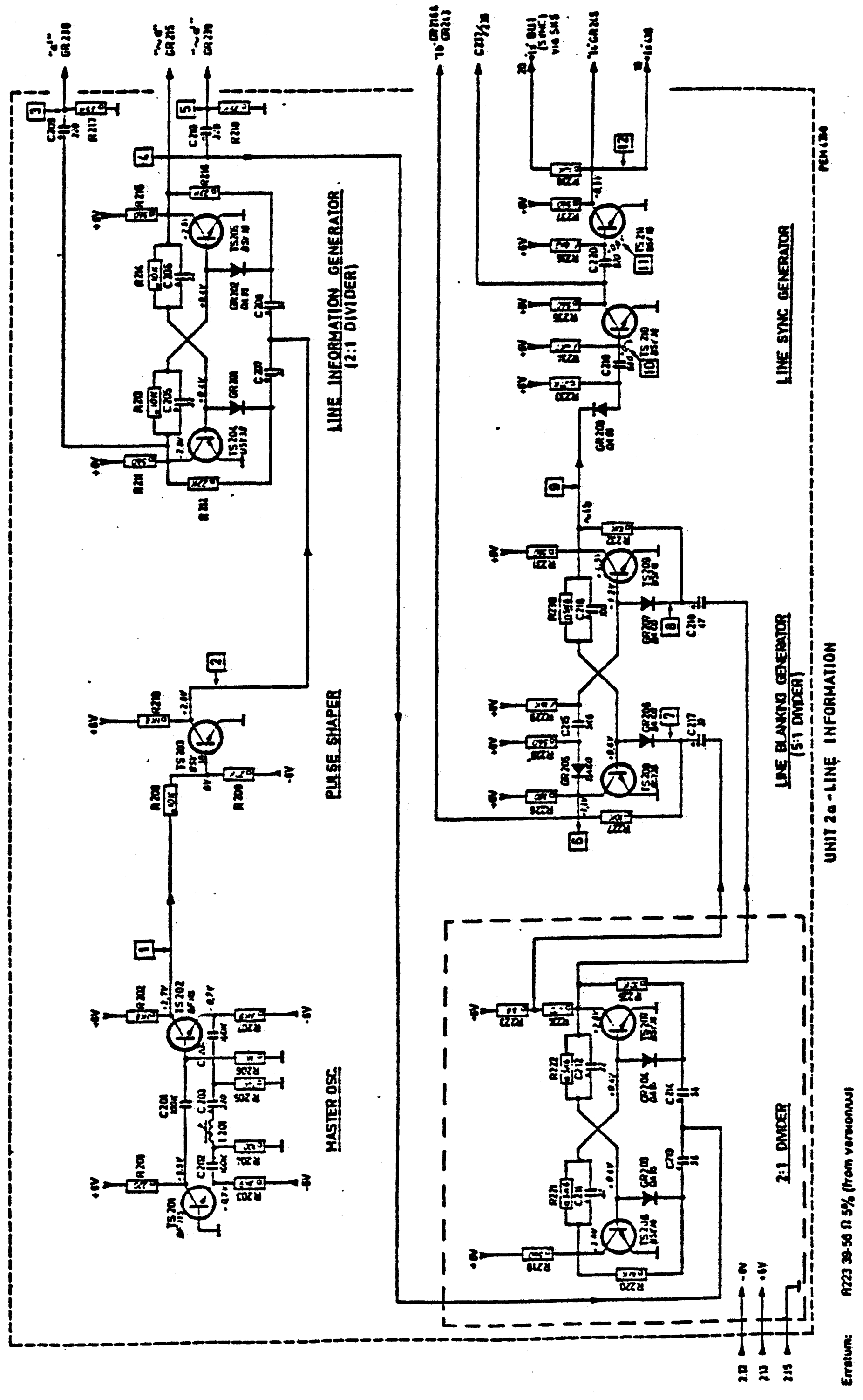


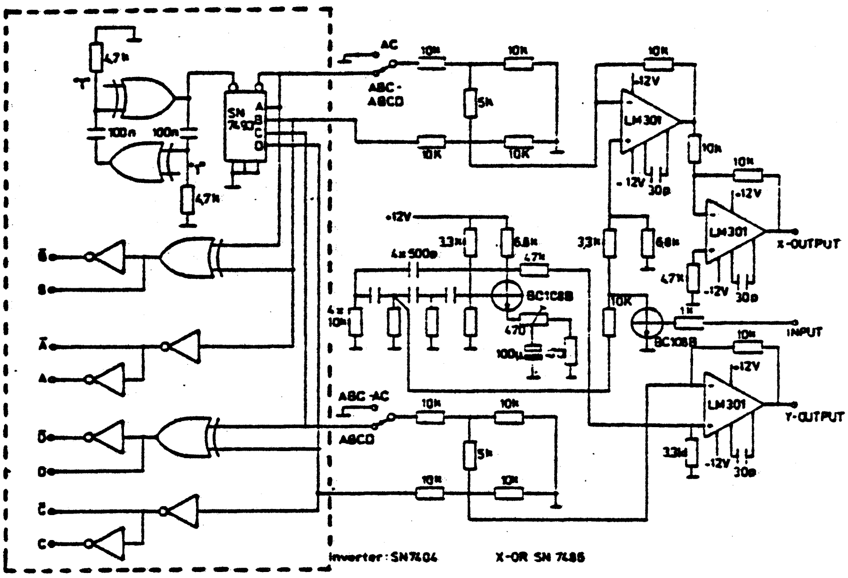
+13V (3)
R46 47K
R43 4700
C15 470
-7.5V
CR15
R40 4700
0V
12
C13 470
L1 10
13V
Q6 2N708
R36 470
R30 620
CW
6.5V
R31 200
LEVEL ADJ
0V
R32 390
0V
C9 30
R26 430
7.5V
+13V (3)
R23 180
9.5V
Q5 2N708
Q2 2N708 EMITTER FOLLOWER
7V
+13V (3)
8V
19
R21 1000
0V
CR14
+13V (3)
R18 2000
R19 6200
0V

(Kan ikke tåle at få reset hvis clock er lav.)



PM 6612.


LINE INFORMATION GENERATOR
(2:1 DIVIDER)
PULSE SHAPER
MASTER OSC
LINE SYNC GENERATOR
LINE BLANKING GENERATOR
(5:1 DIVIDER)
2:1 DIVIDER
UNIT 2a - LINE INFORMATION
Erratum:
R223 39-56 Ω 5%



'93A, 'L93, 'LS93 . . . 4-BIT BINARY COUNTERS

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'L90	20 mW
'LS90	45 mW
'92A, '93A	130 mW
'LS92, 'LS93	45 mW
'L93	16 mW

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, 'L90, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, 'L93, and 'LS93.

All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

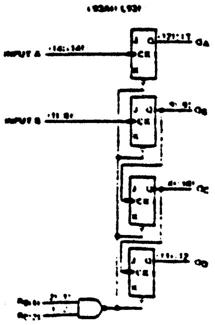
'93A, 'L93, 'LS93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

'92A, 'LS92, '93A, 'L93, 'LS93
RESET/COUNT FUNCTION TABLE

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	OUTPUT Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

'93A, 'L93, 'LS93



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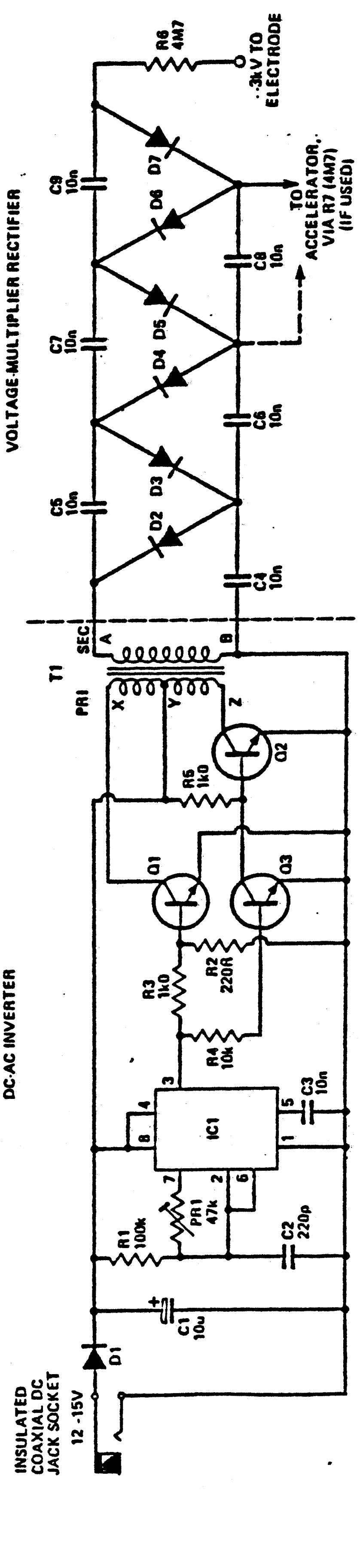


NOTE
IC1 IS 555
Q1,2 ARE TIP 31C
Q3 IS BC107
D1,8 ARE 1N4001
D2–7 ARE 1N4007

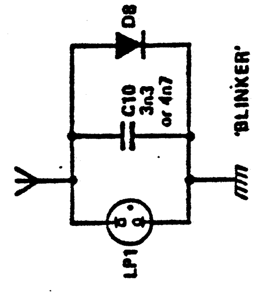
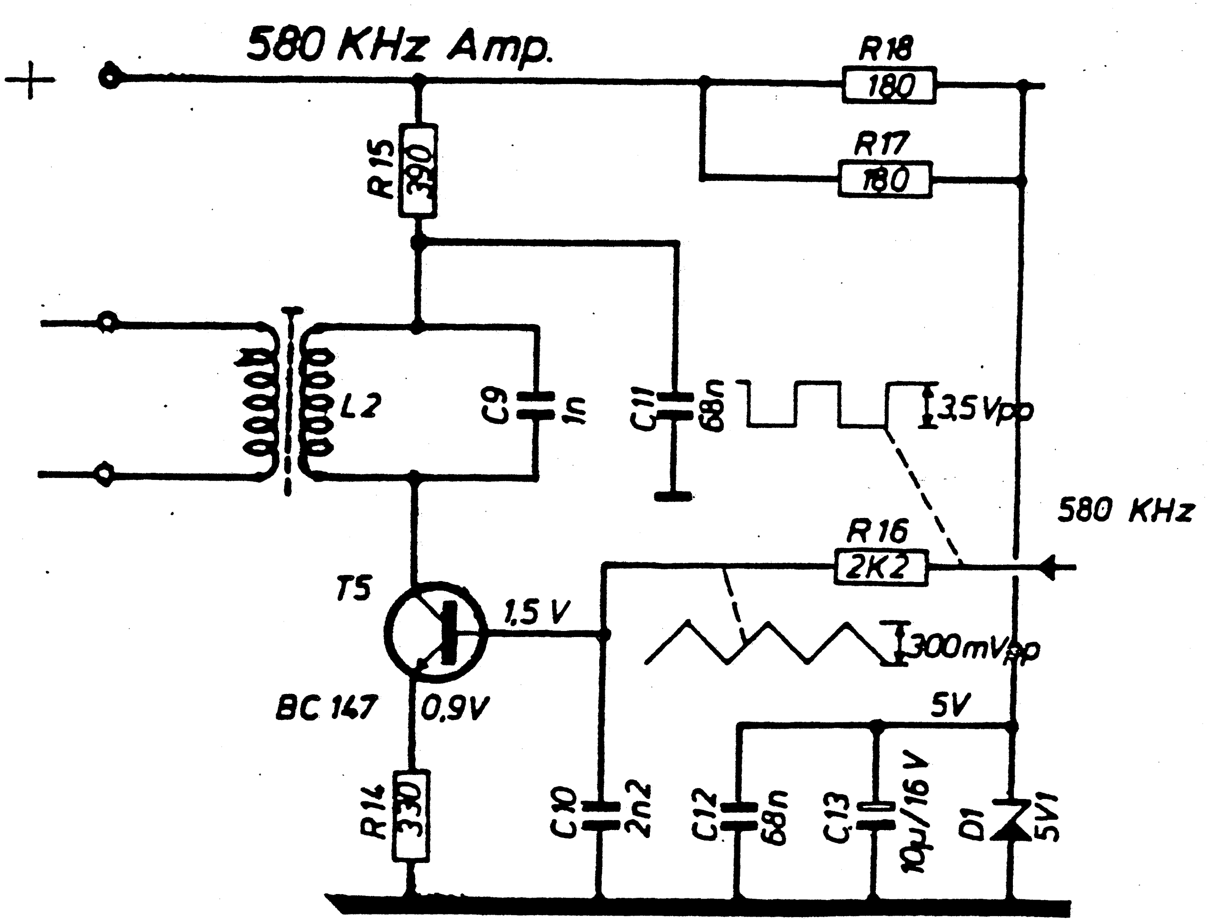
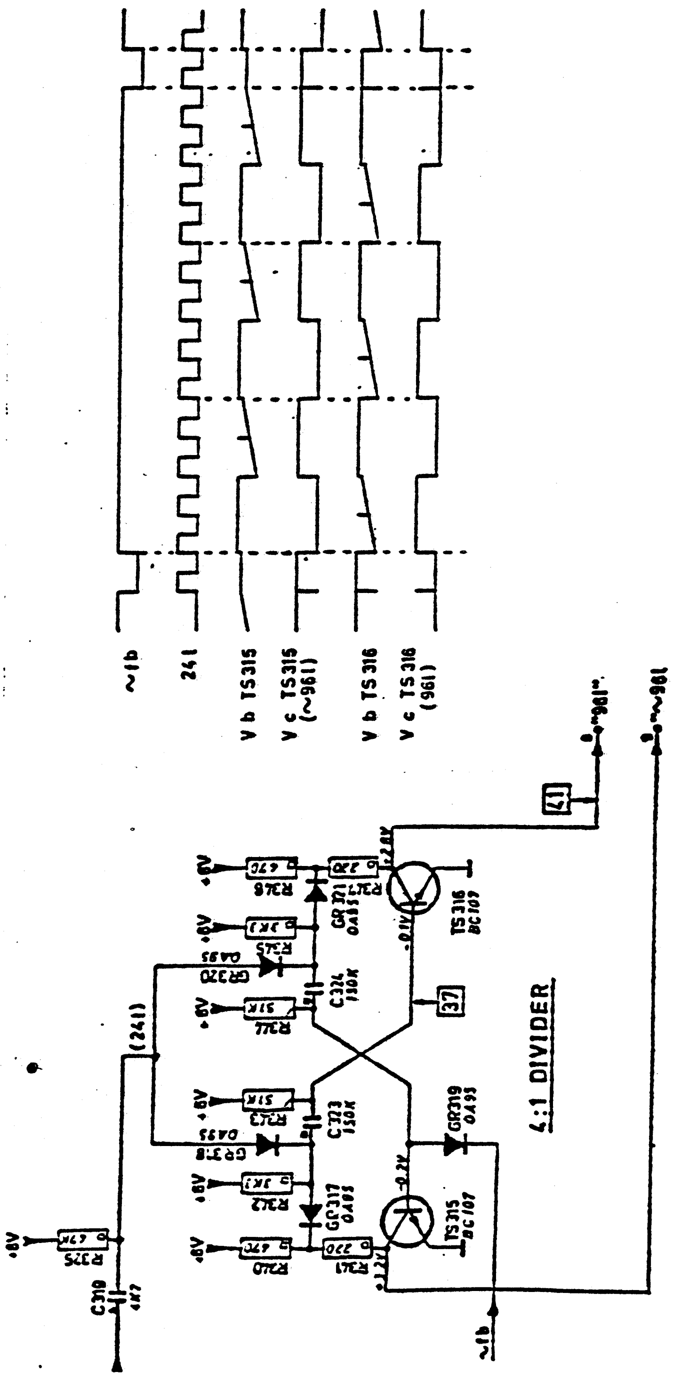


Fig. 1 Circuit diagram for all three sections of the negative ion generator. Current consumption of the unit is a little too high for use with ordinary batteries; we recommend you run it from a battery eliminator pack or a 12 V car battery.

Forklaring

37354

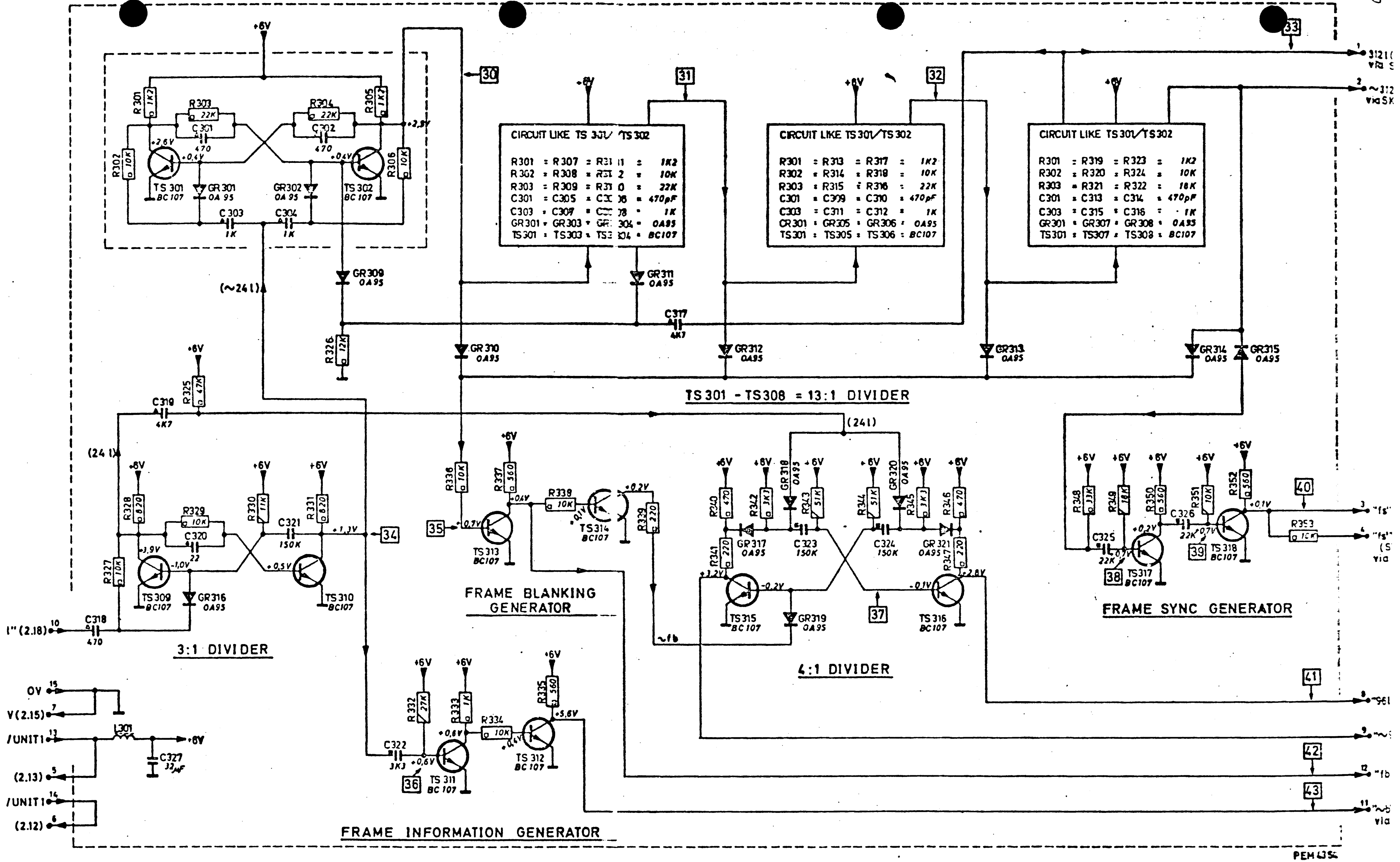

580 KHz Amp.
+
R18
180
R17
180
R15
390
L2
C9
1n
C11
68n
3,5 Vpp
580 KHz
R16
2K2
T5
1,5 V
300mVpp
BC 147
0,9V
5V
R14
330
C10
2n2
C12
68n
C13
10μ/16 V
D1
5V1



~1b
241
V b TS 315
V c TS 315 (~961)
V b TS 316
V c TS 316 (961)
4:1 DIVIDER
TS 315 BC 107
TS 316 BC 107
C 310 4K7
C 323 150K
C 324 150K
GR 317 OA 95
GR 318 OA 95
GR 319 OA 95
GR 320 OA 95
GR 321 OA 95
(241)
37
41
+6V

37354

B 28



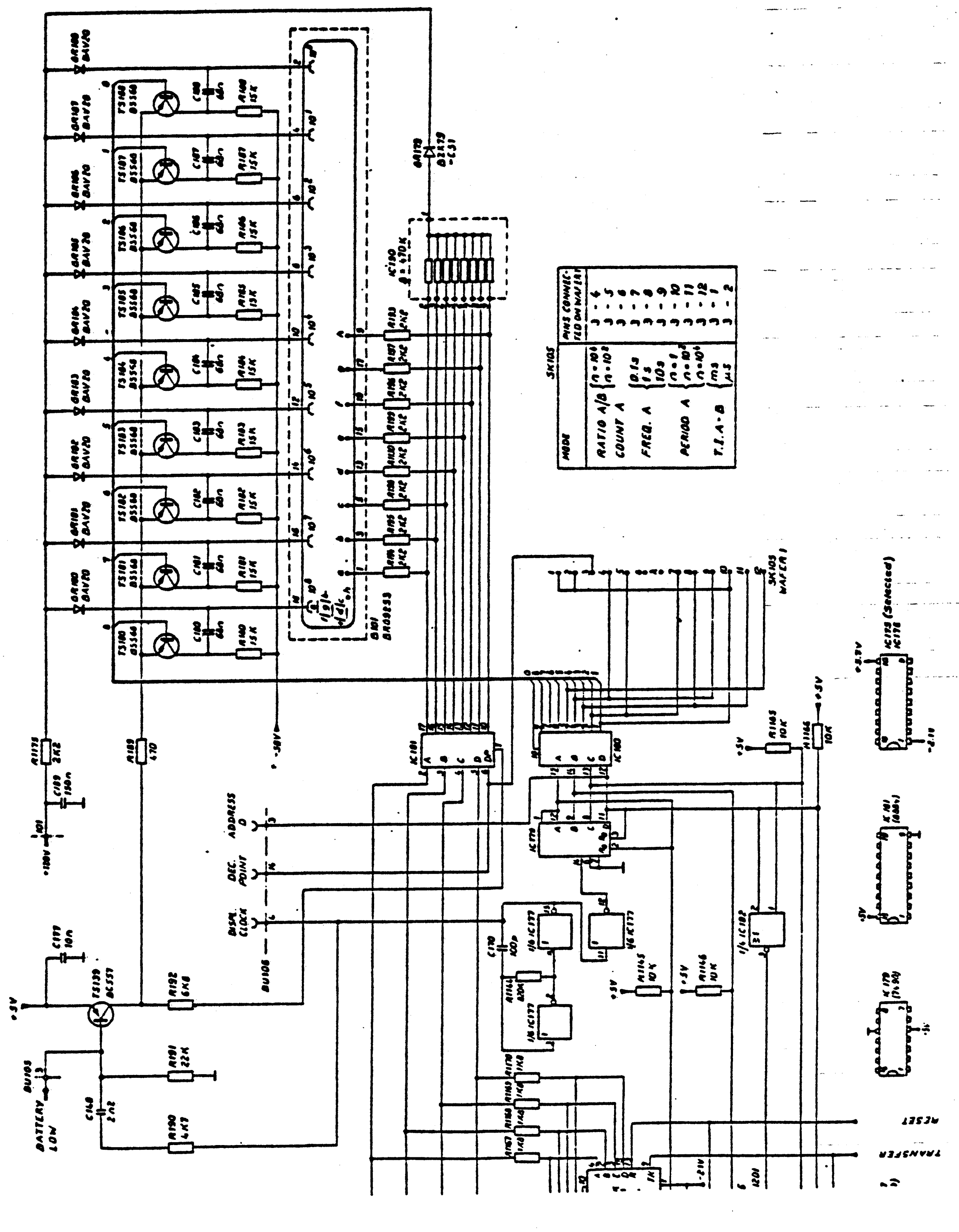
UNIT 3 FRAME INFORMATION

um: BC 107 → BC 207 B (from version /05)
R 330 → 10K5 1% (from version /03)

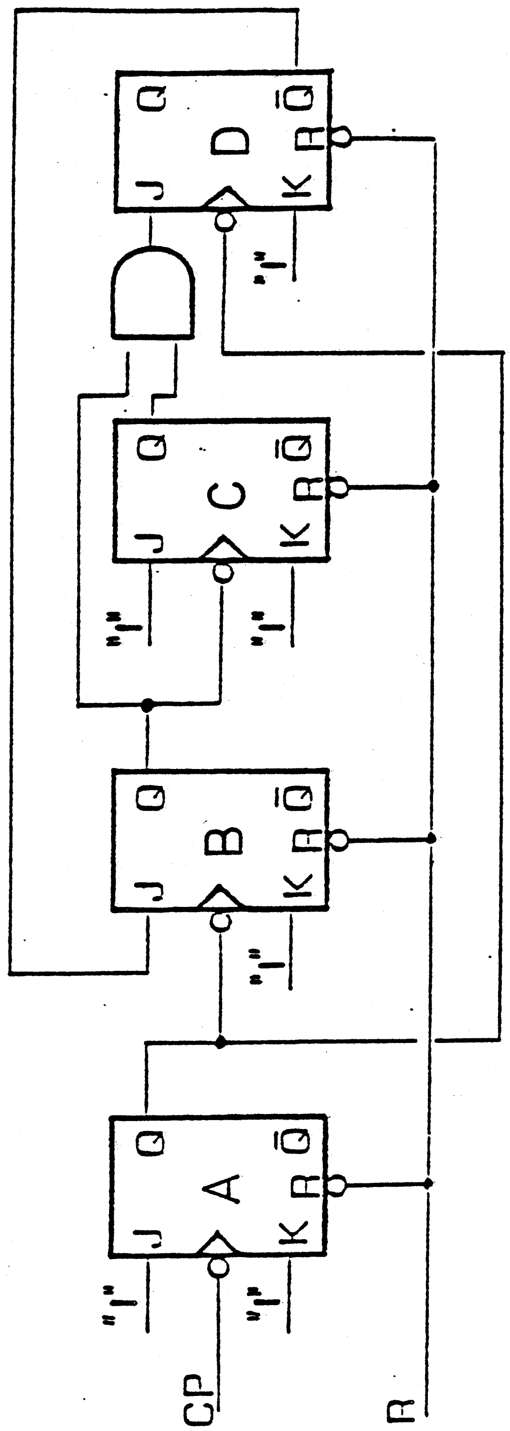
B 28

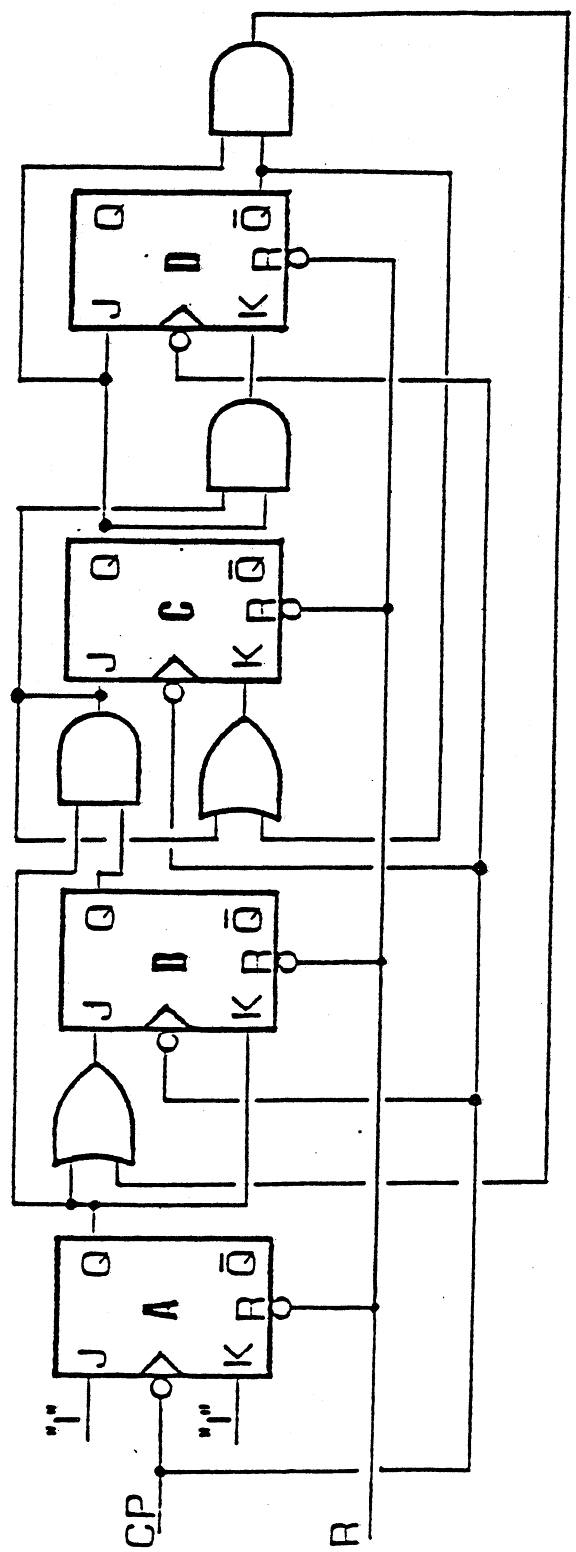
4 : 1 Divider

This generator supplies the gate circuit in unit 2c with the frame information pulses "~ 96 l" and "96 l" used in pattern SK3/1 - "BL/WH". The generator is an astable multivibrator consisting of TS315 and TS316.
Synchronization is effected by means of the positive-going "24 l" transients via GR318 and GR320.
Via GR319 a negative-going frame blanking pulse ensures that the divider is stopped during this period, and consequently started in the same phase after each frame blanking pulse. The working principle is shown in Fig. II-24.
At moment t_1 the oscillator is stopped by means of "~ fb" pulses which keep TS315 cut off.
At moment t_2 the positive-going transient of the "24 l" pulse via GR318 will drive TS315 into saturation. The voltage drop at the collector will charge C323 via GR315 to a negative value. This voltage keeps TS316 cut off for a period depending on the discharge time of C323 via R343.
At moment t_3 the generator is synchronized by means of the "24 l" pulses via GR320.
TS316 is now conducting, and the process is repeated, only this time TS315 is cut off.

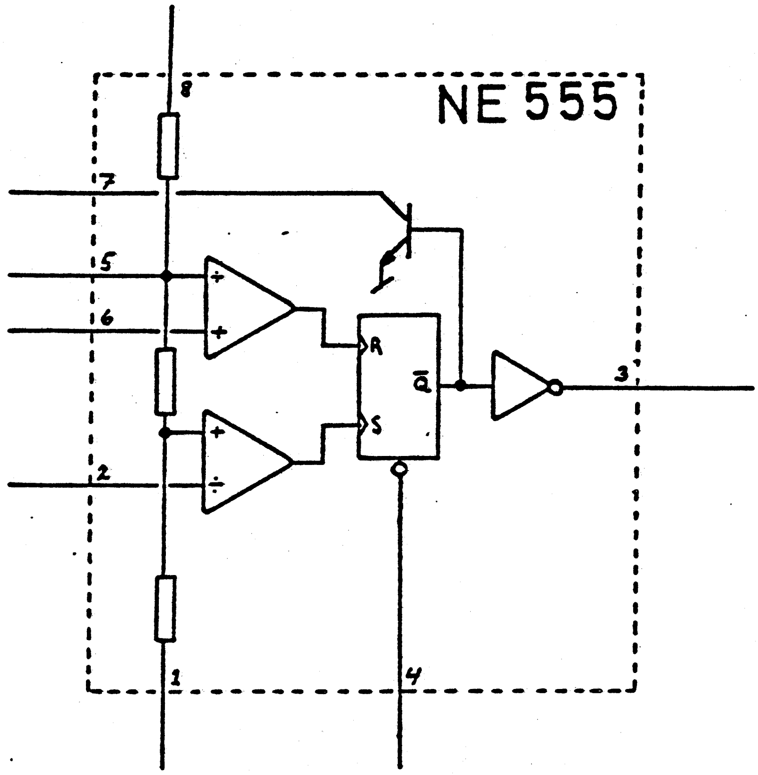


PM 6612

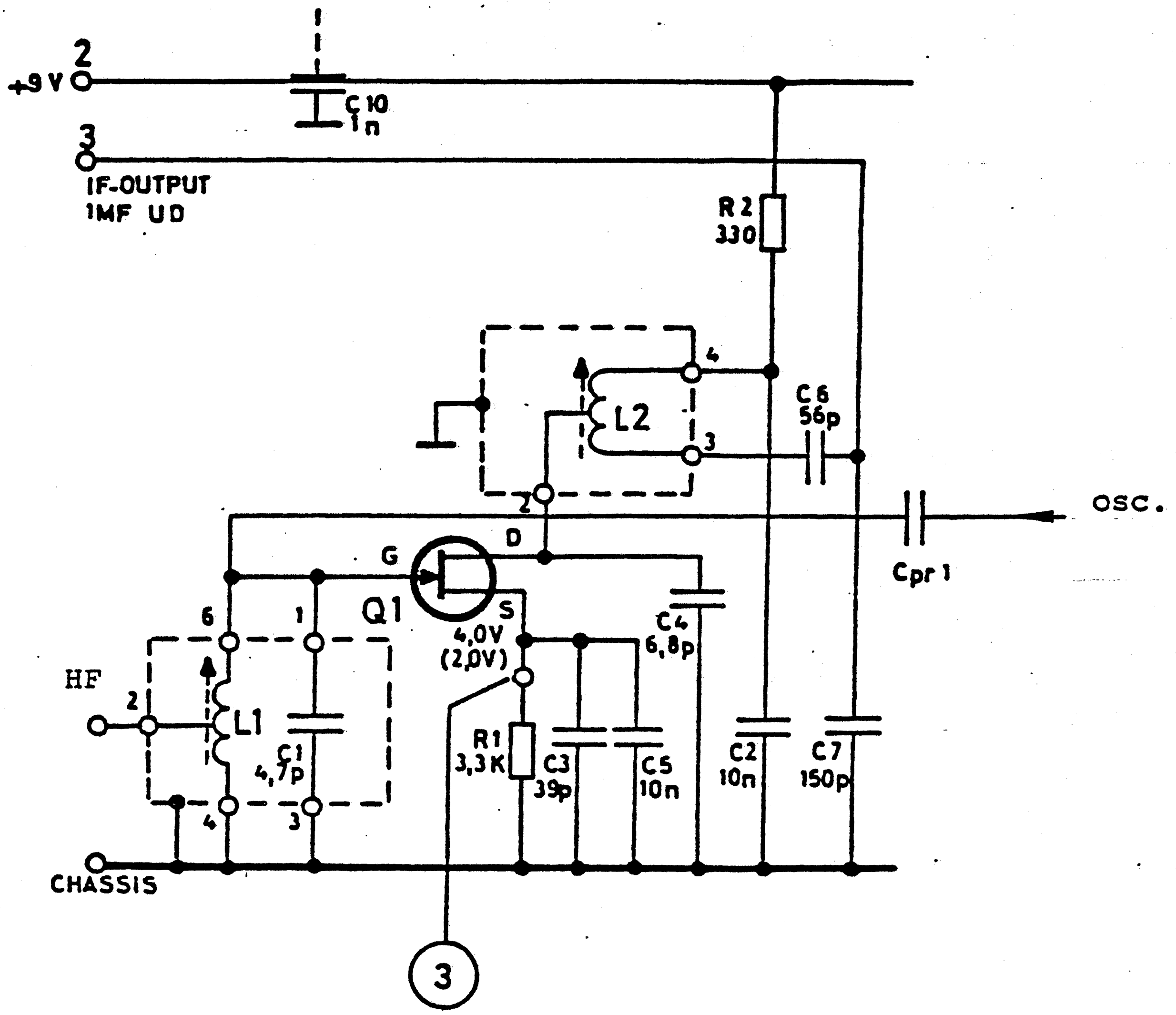

A
B
C
D
J
K
Q
Q̄
R
"1"
CP
R

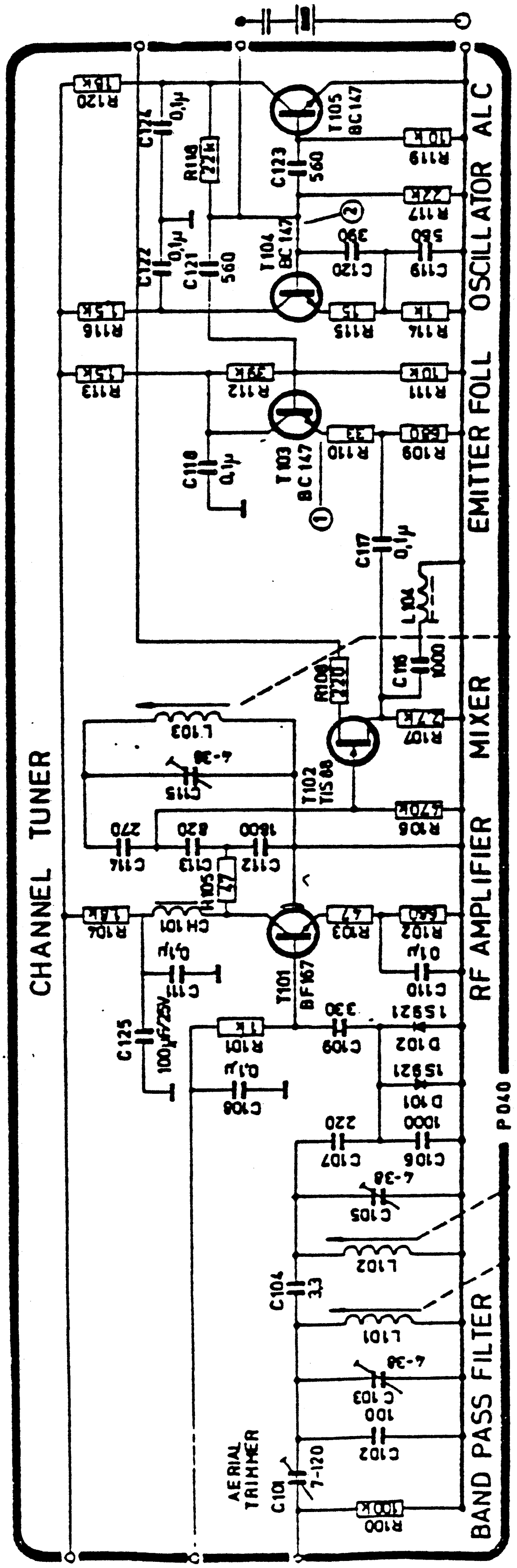


37354



1. GND.
2. Trigger.
3. Output.
4. Reset.
5. Control voltage.
6. Thres hold.
7. Discharge.
8. VCC.


+9V
2
C10
1n
3
IF-OUTPUT
IMF UD
R2
330
4
C6
56p
L2
3
2
OSC.
D
G
Cpr1
Q1
6
1
S
4,0V
(2,0V)
C4
6,8p
HF
2
L1
C1
4,7p
R1
3,3K
C3
39p
C5
10n
C2
10n
C7
150p
4
3
CHASSIS
3

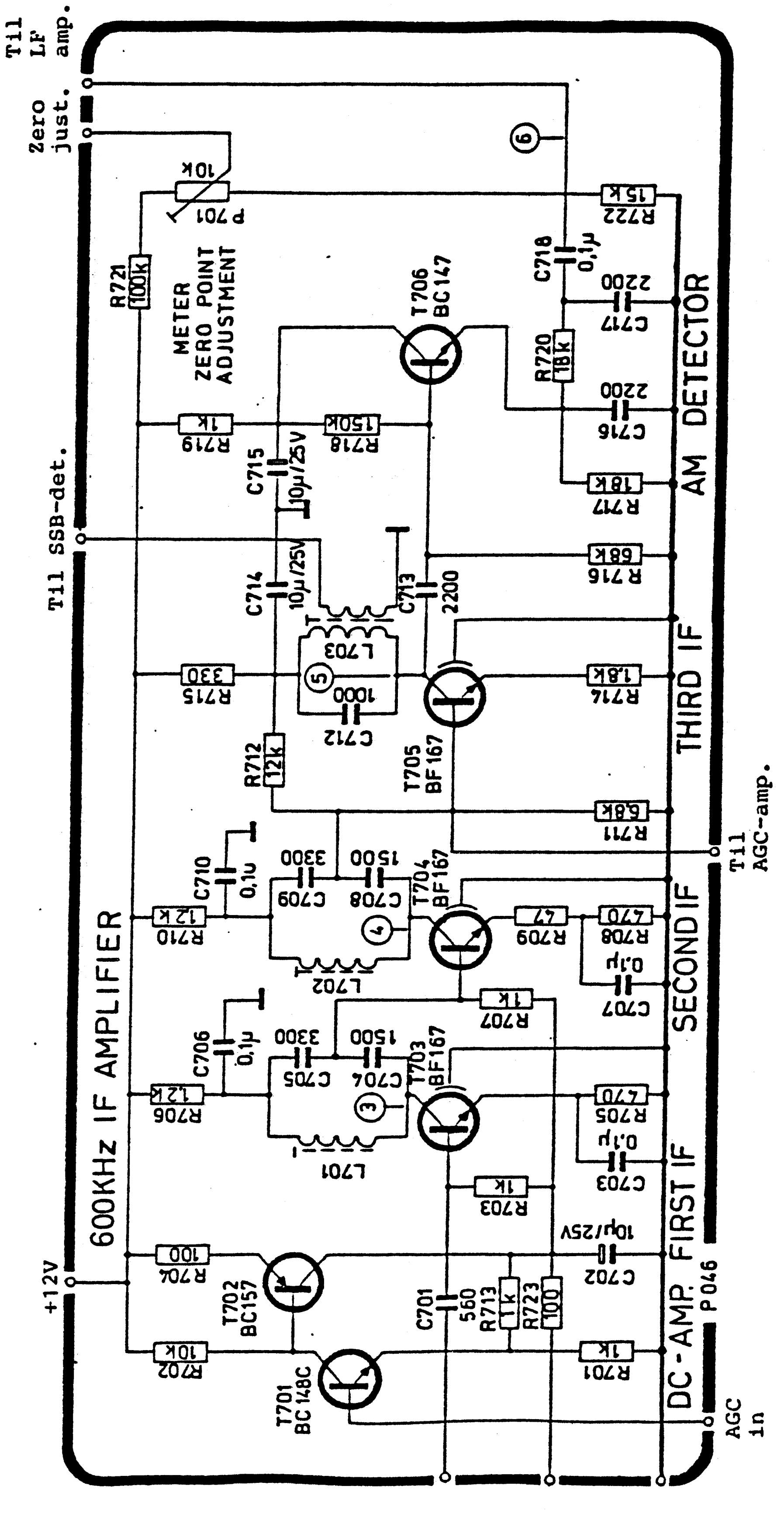


SP Sailor

37354

Metalindustriens Svendeprøvekommissioner

KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN

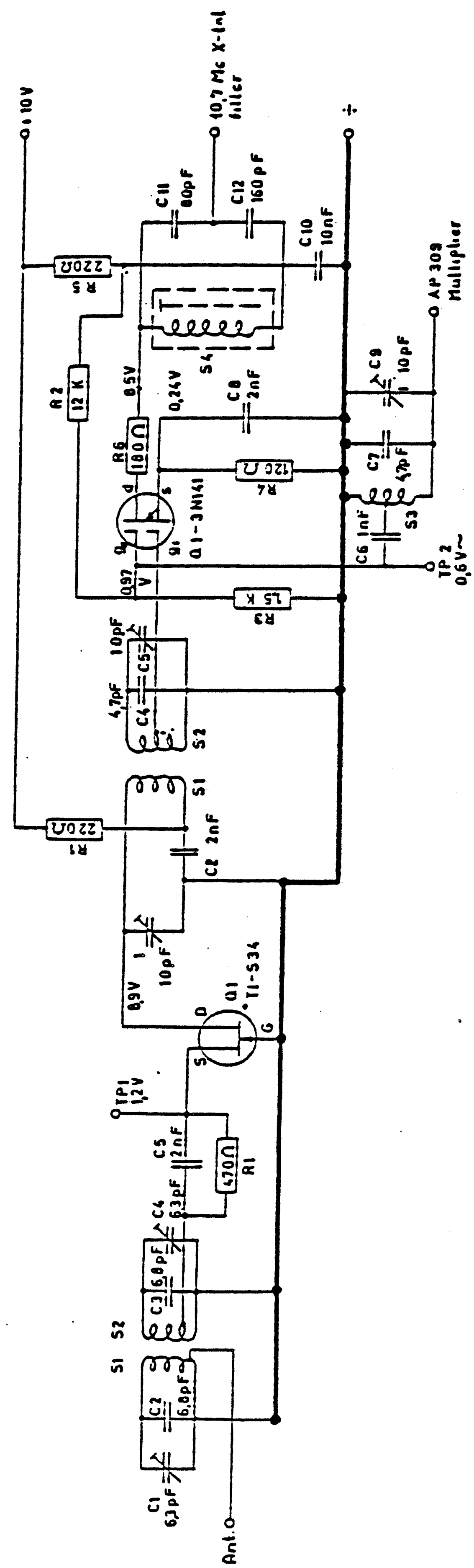


37354

Metalindustriens Svendeprøvekommissioner

C 36

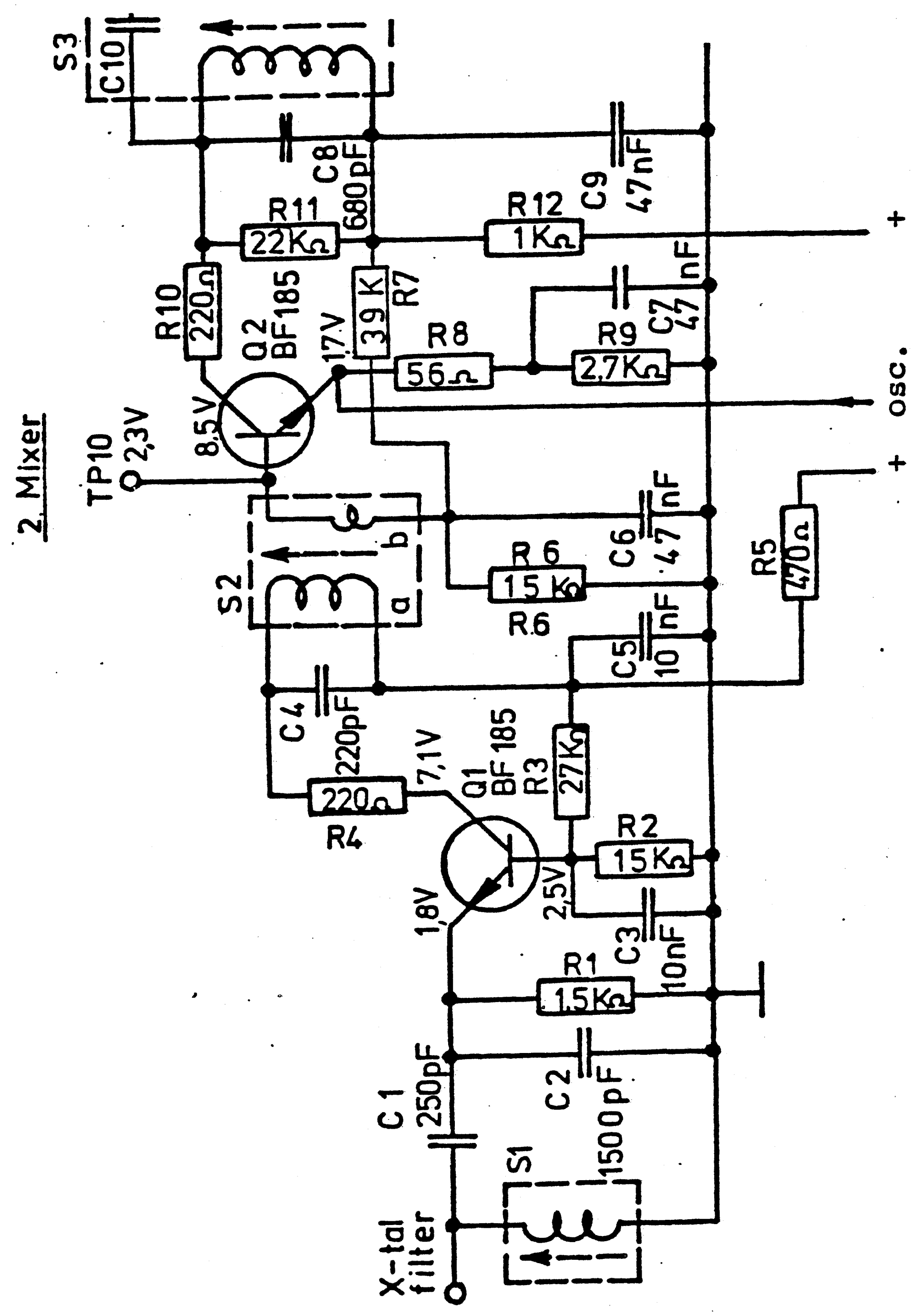
KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN

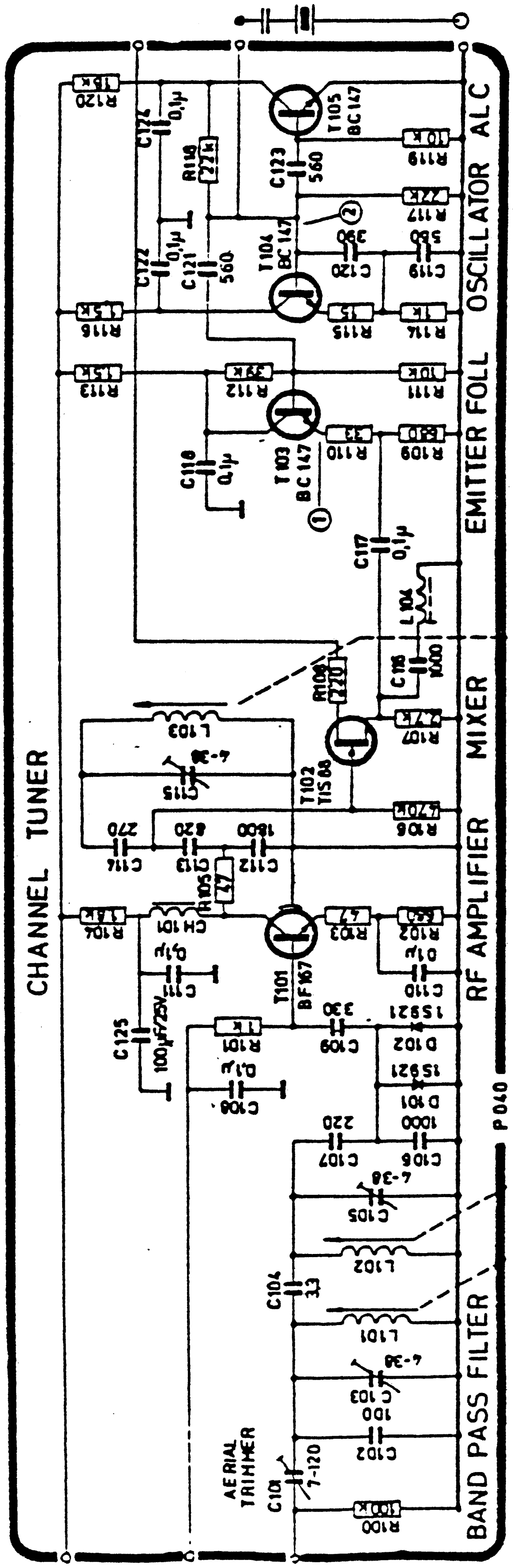


37354

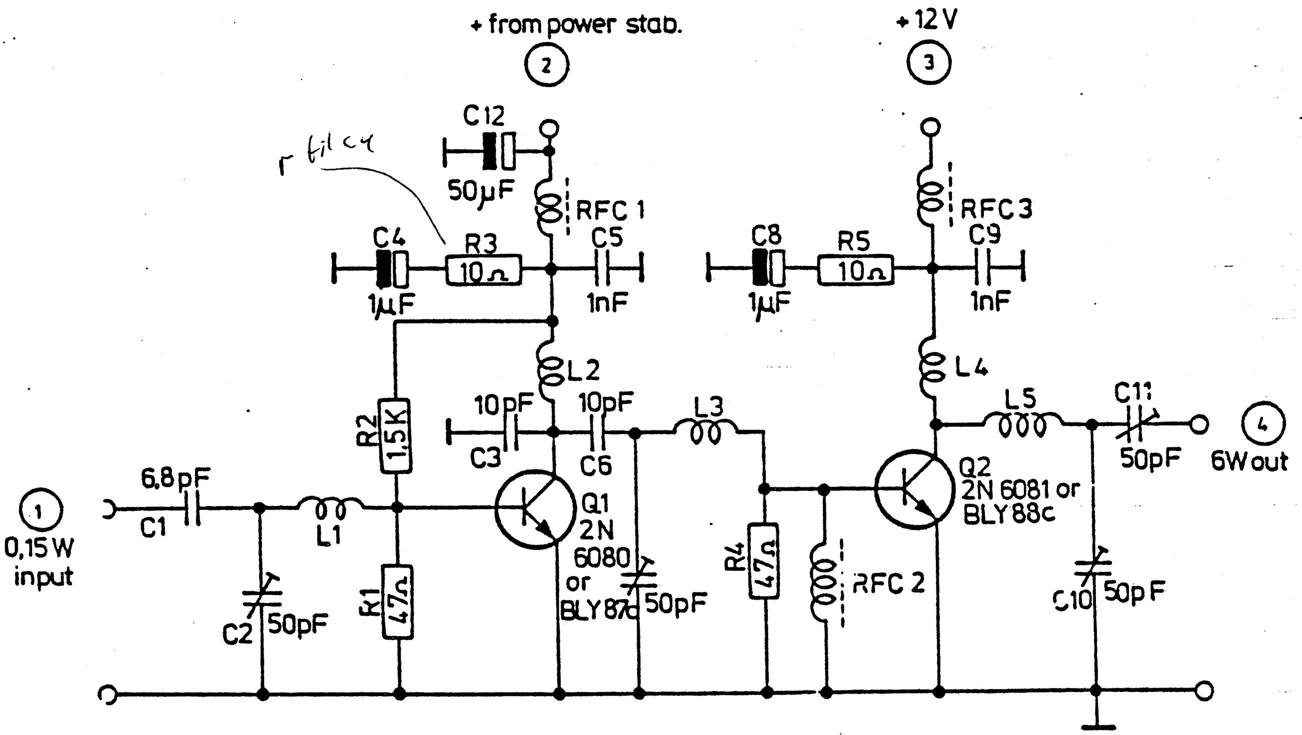
Metalindustriens Svendeprøvekommissioner

KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN





CHANNEL TUNER
BAND PASS FILTER
RF AMPLIFIER
MIXER
EMITTER FOLL
OSCILLATOR
ALC
P 040
AERIAL TRIMMER
T101 BF167
T102 TIS88
T103 BC147
T104 BC147
T105 BC147
D101 1S921
D102 1S921
L101
L102
L103
L104
CH101

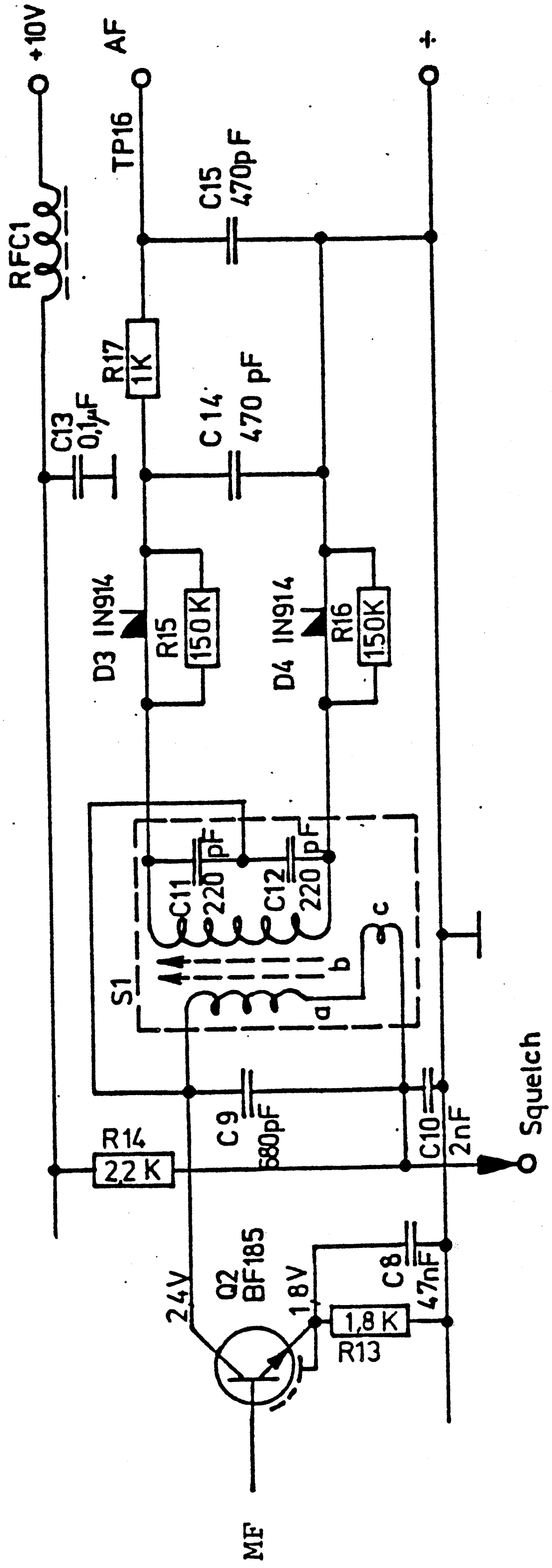

+ from power stab.
2
+ 12 V
3
C12
50μF
RFC 1
C4
R3
10Ω
C5
1μF
1nF
C8
R5
10Ω
C9
RFC3
1μF
1nF
L2
L4
10pF
10pF
C3
C6
L3
L5
C11
50pF
4
6W out
R2
1,5K
6,8pF
C1
L1
1
0,15 W
input
Q1
2N
6080
or
BLY87c
50pF
R4
47Ω
RFC 2
Q2
2N 6081 or
BLY 88c
C10
50pF
C2
50pF
R1
47Ω

37354

Metalindustriens Svendeprøvekommissioner

C 40

KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN

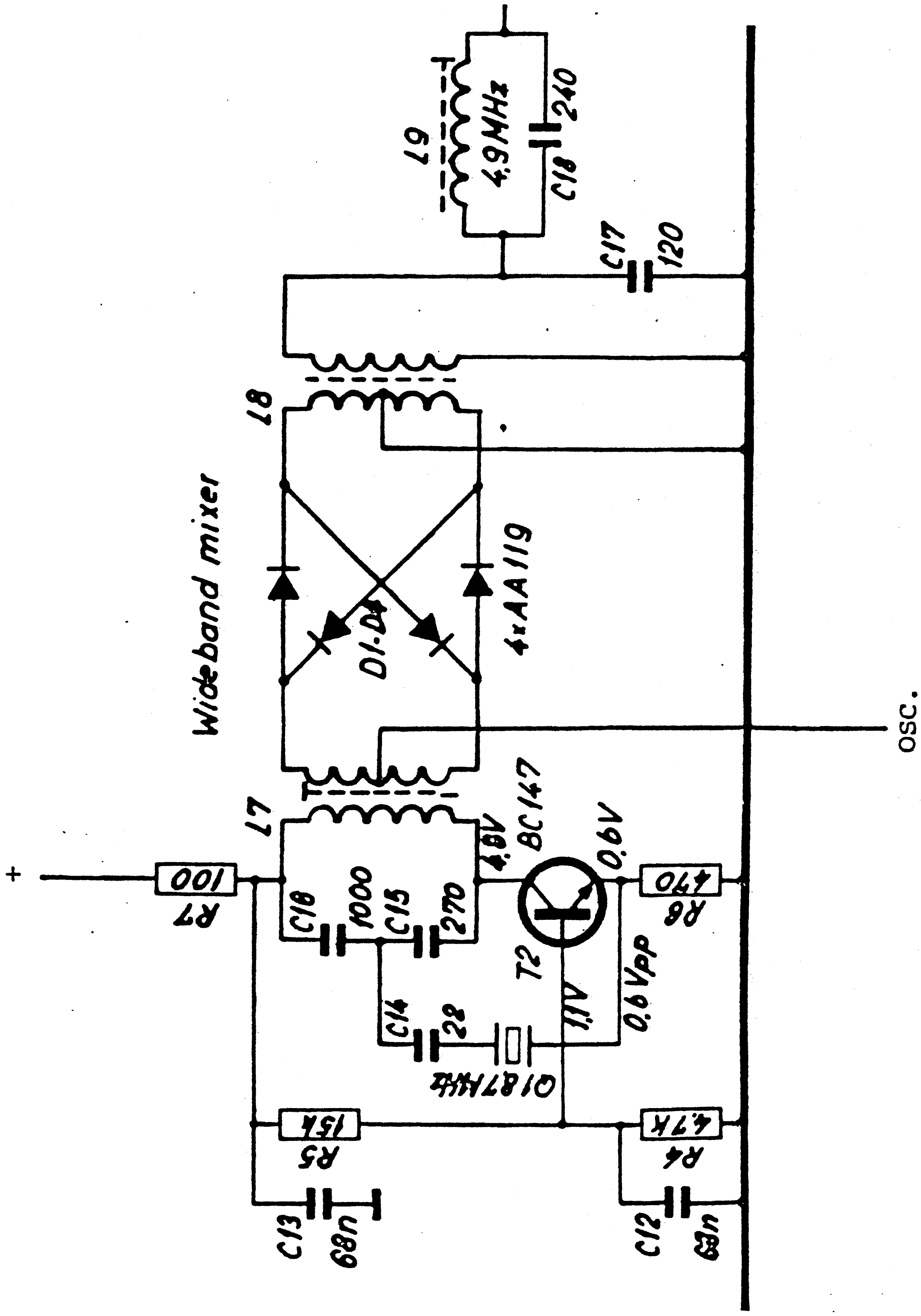


37354

Metalindustriens Svendeprøvekommissioner

C 41

KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN

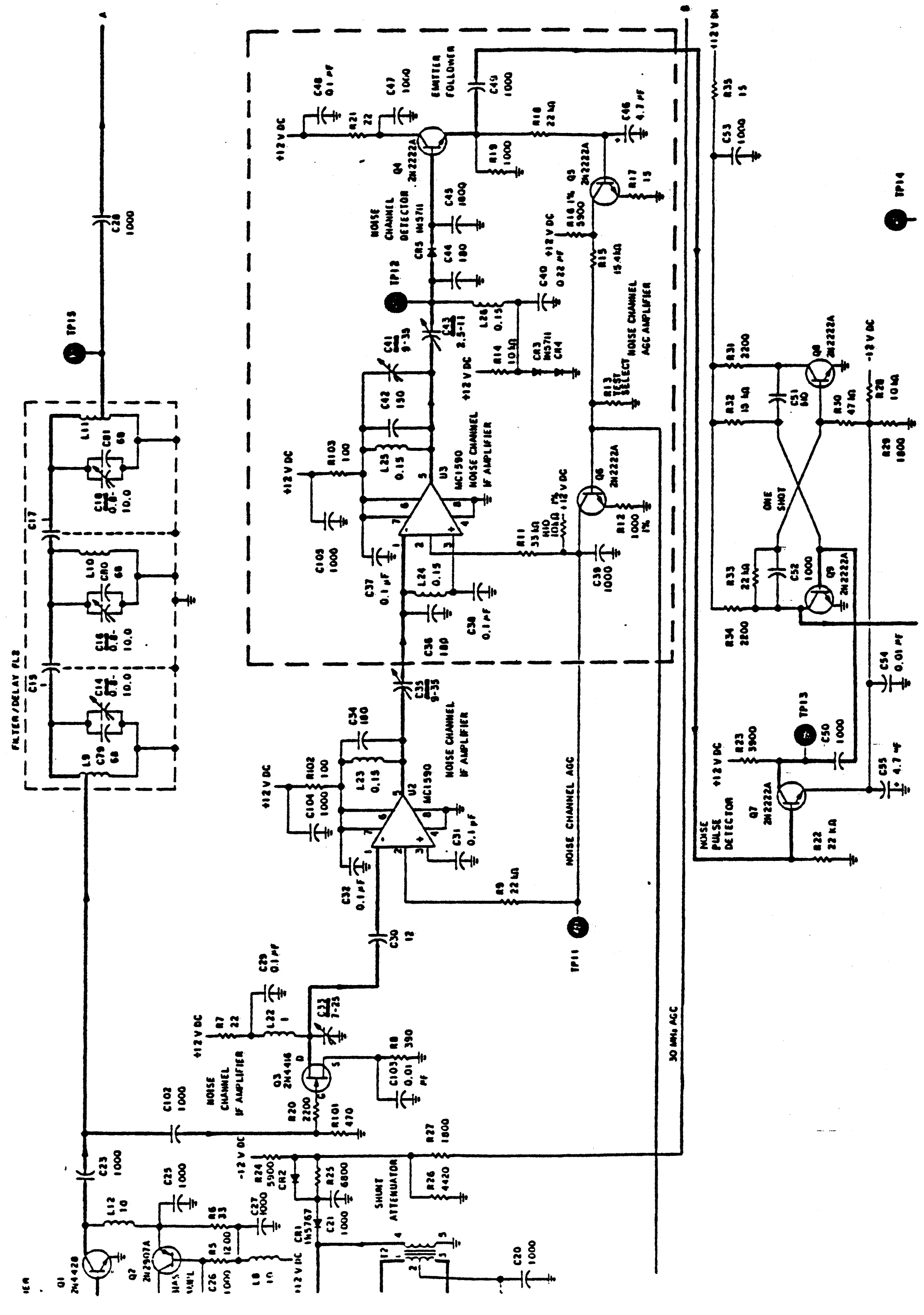


37354

Metalindustriens Svendeprøvekommissioner

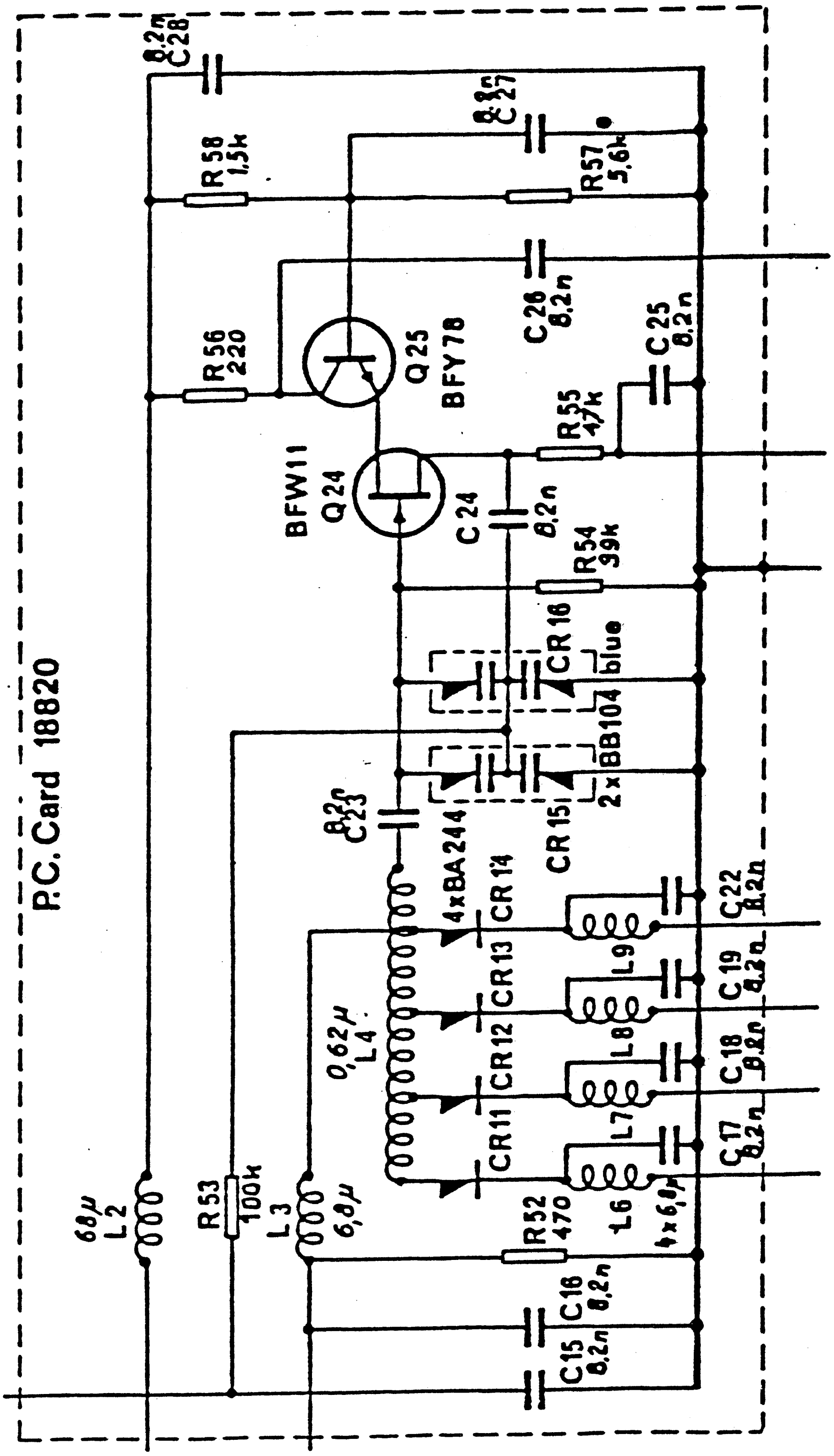
C42

KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN



TR10 modtager

37354



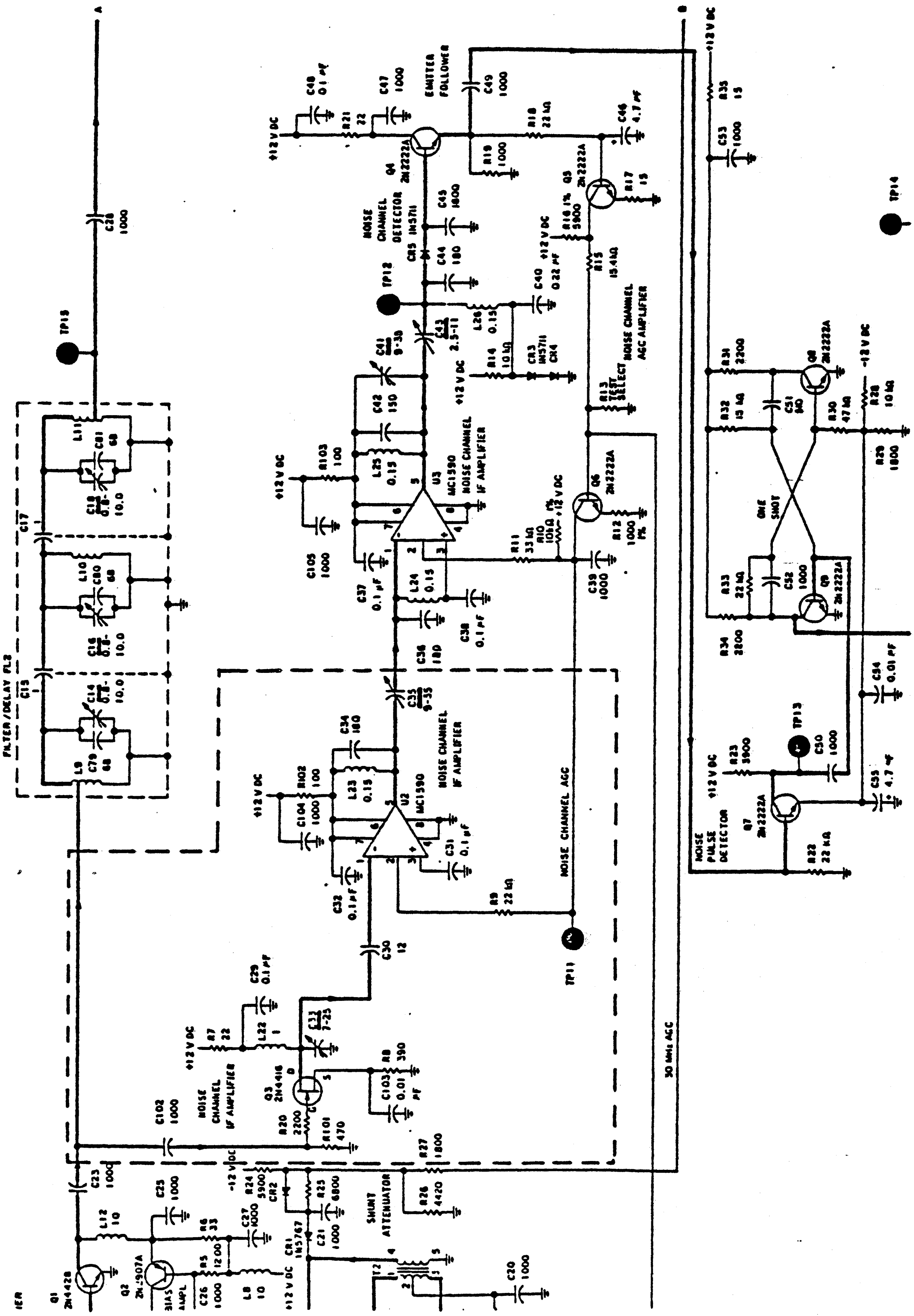
Sailor.

37354

Metalindustriens Svendeprøvekommissioner

C 44

KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN

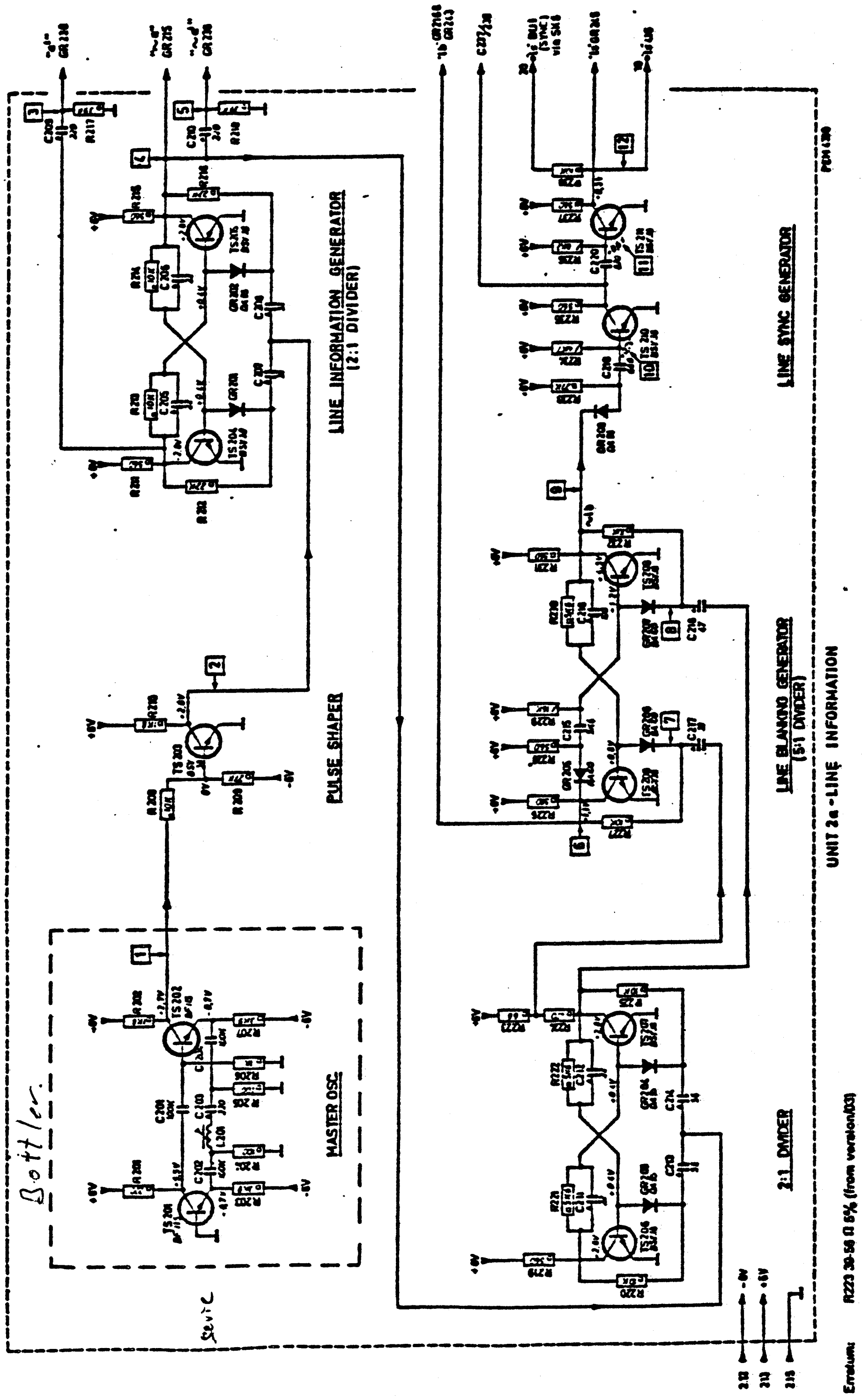


37354

Metalindustriens Svendeprøvekommissioner

C 45

KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN

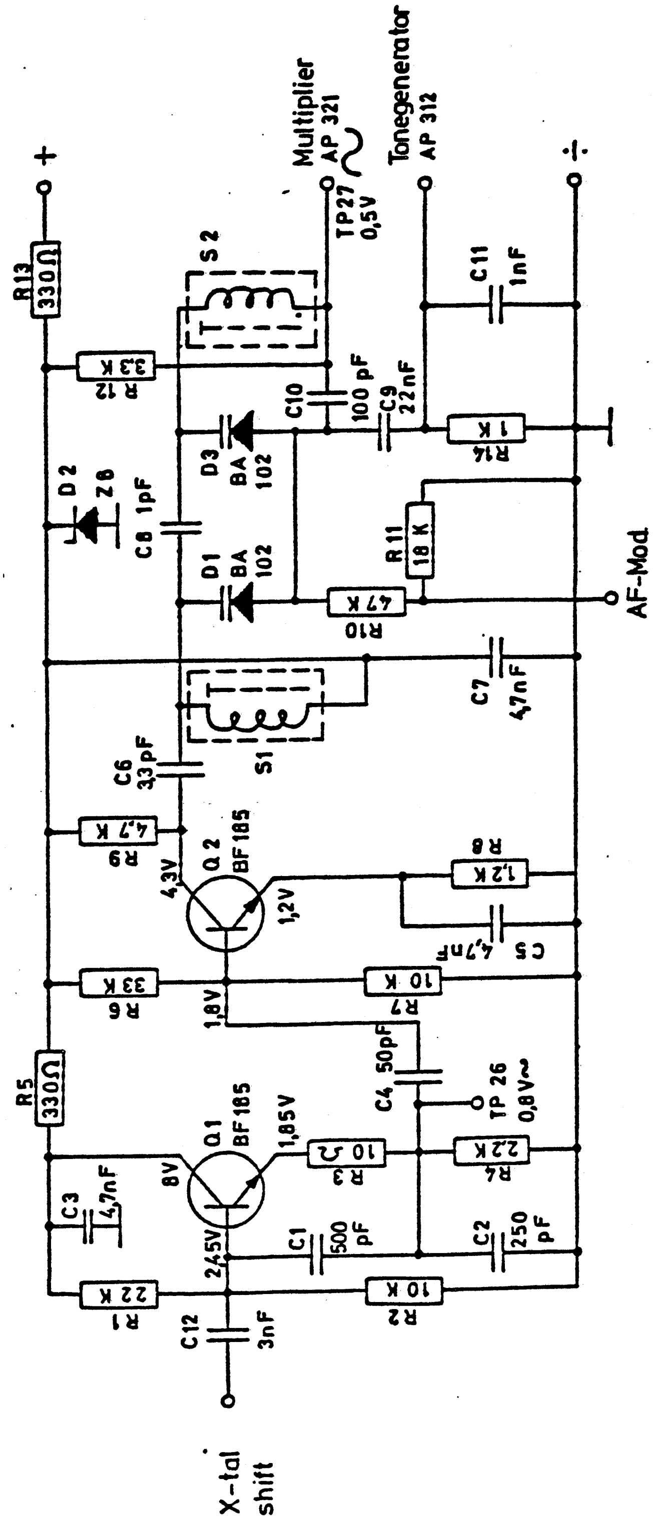


37354

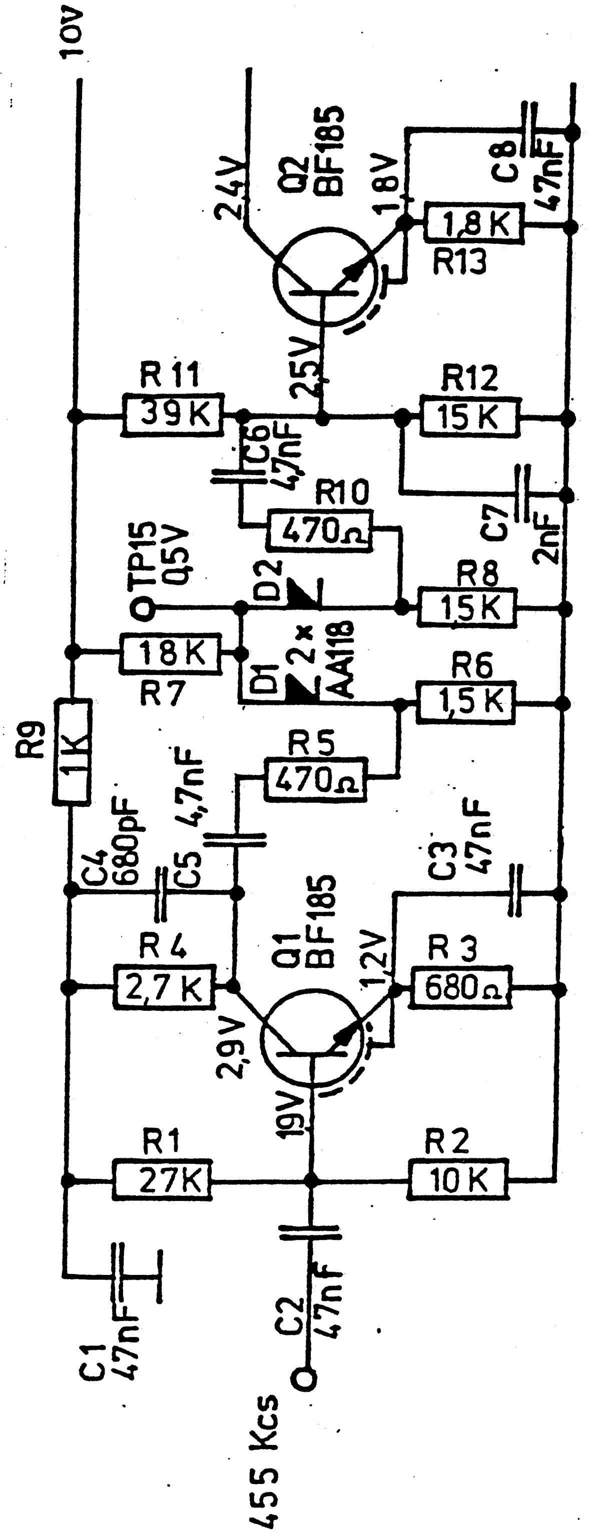
Metalindustriens Svendeprøvekommissioner

C 46

KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN



37354



10V
24V
Q2
BF185
1,8V
C8
47nF
1,8K
R13
R 11
39K
25V
R12
15K
C6
4,7nF
R10
470Ω
C7
2nF
TP15
0,5V
D2
R8
1,5K
18K
R7
2×
AA118
D1
R6
1,5K
R9
1K
R5
470Ω
4,7nF
C4
680pF
C5
C3
47nF
Q1
BF185
1,2V
R 4
2,7 K
R 3
680Ω
2,9V
19V
R1
27K
R2
10K
C1
47nF
C2
47nF
455 Kcs

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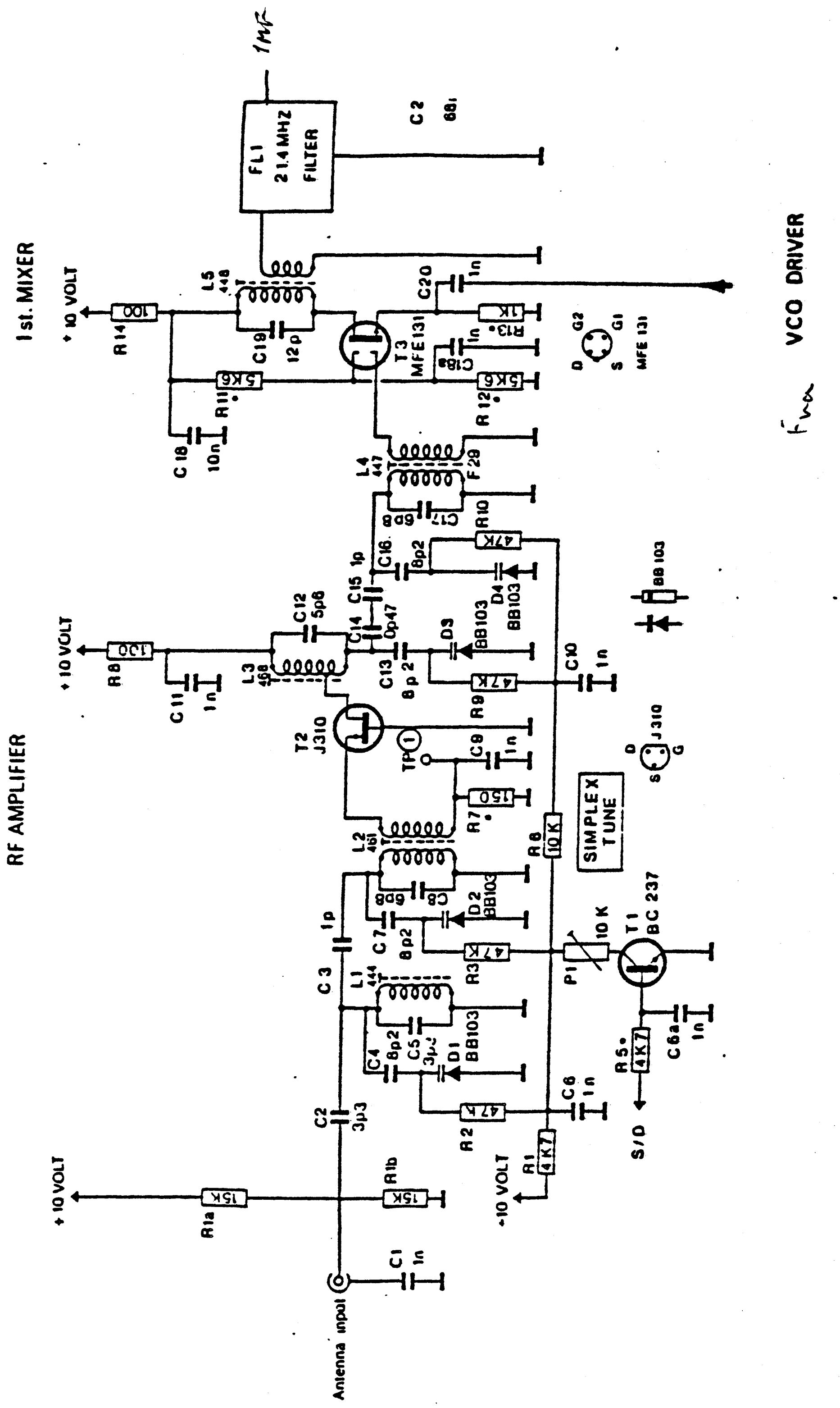
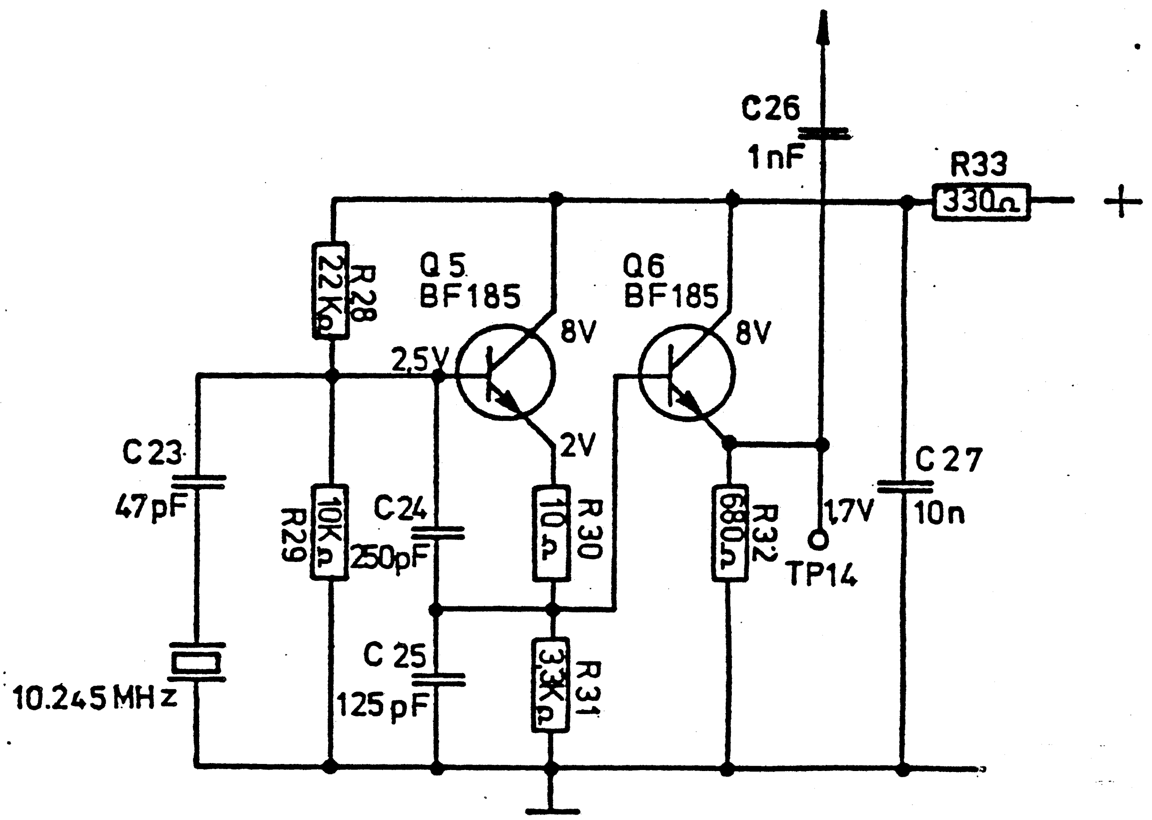
Metalindustriens Svendeprøvekommissioner

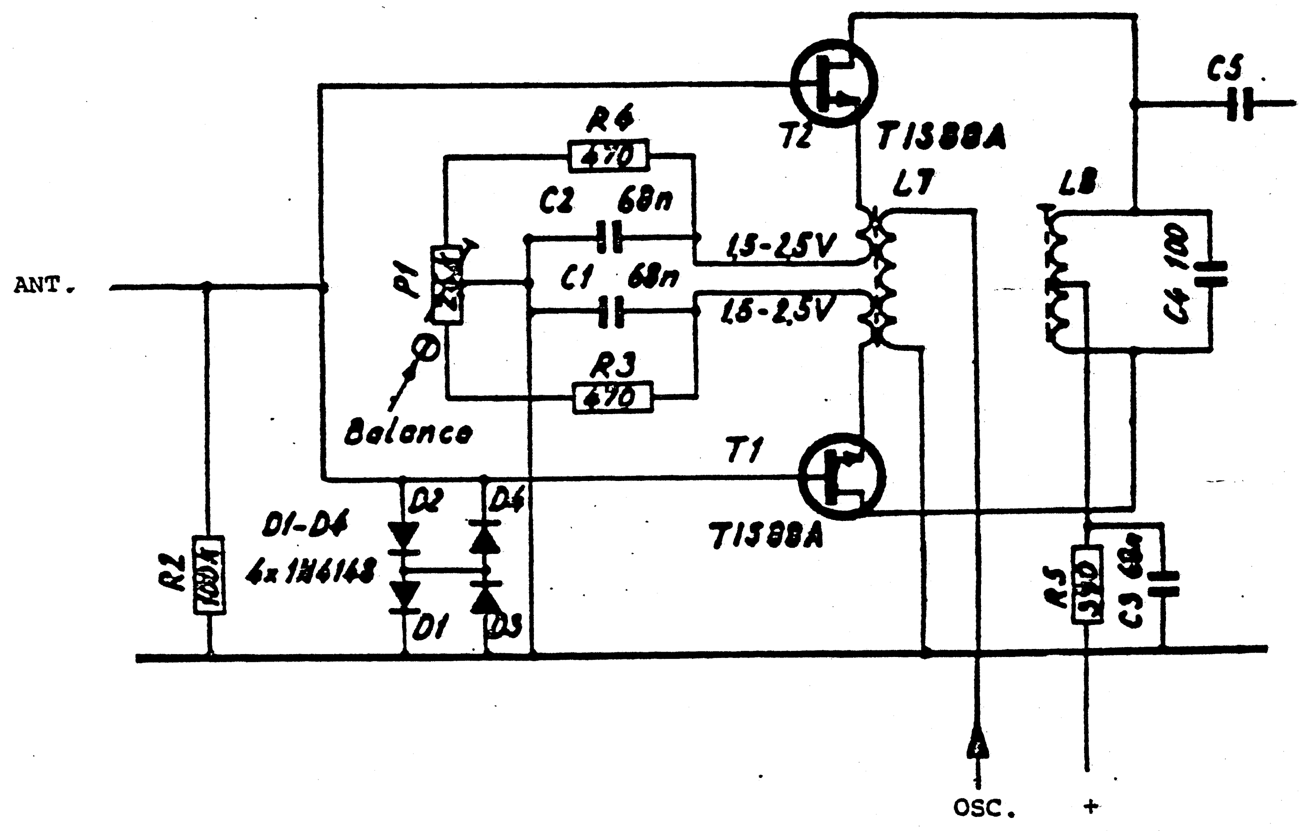
KREDSLØBSOPGAVER FOR ELEKTRONIKMEKANIKERBRANCHEN

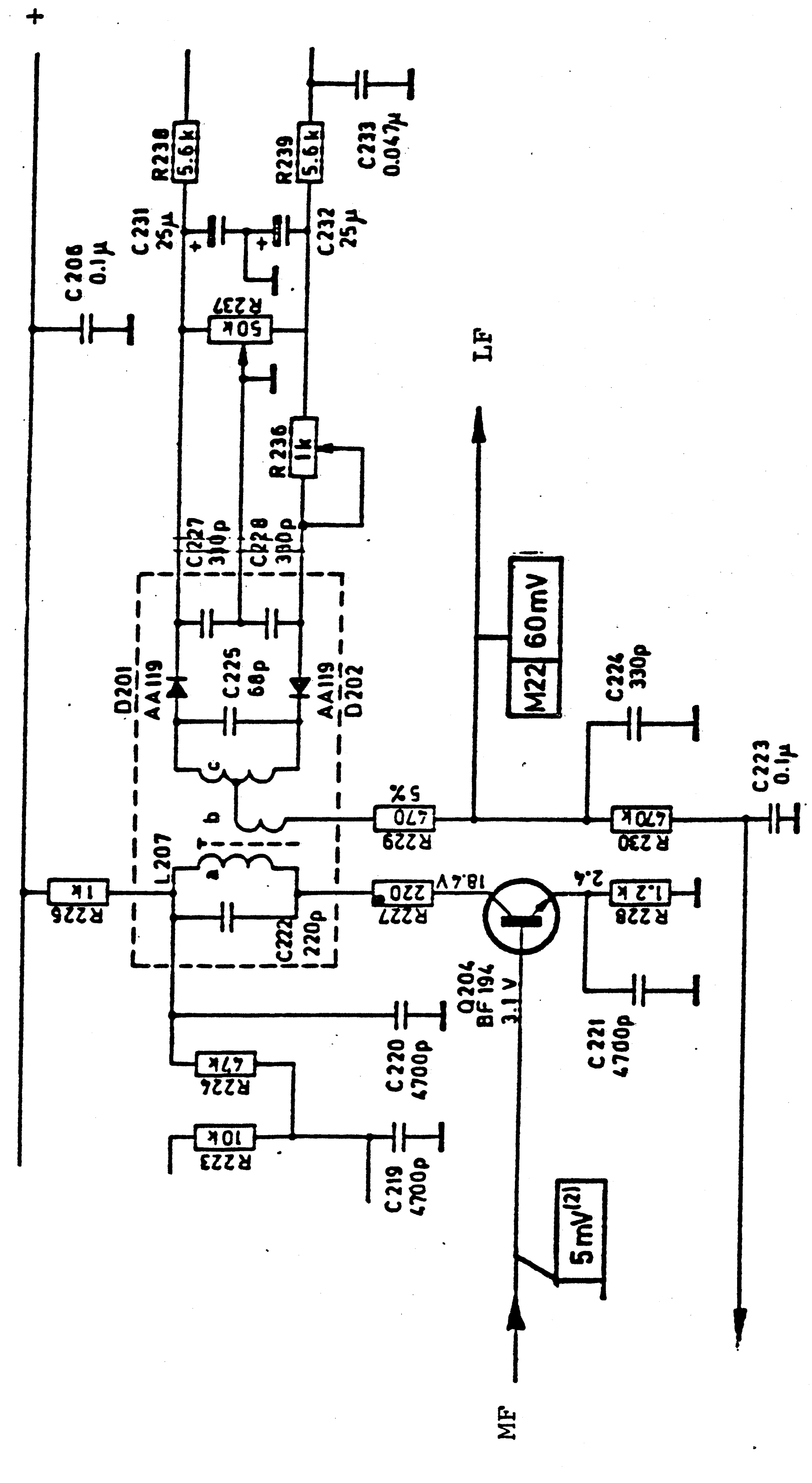


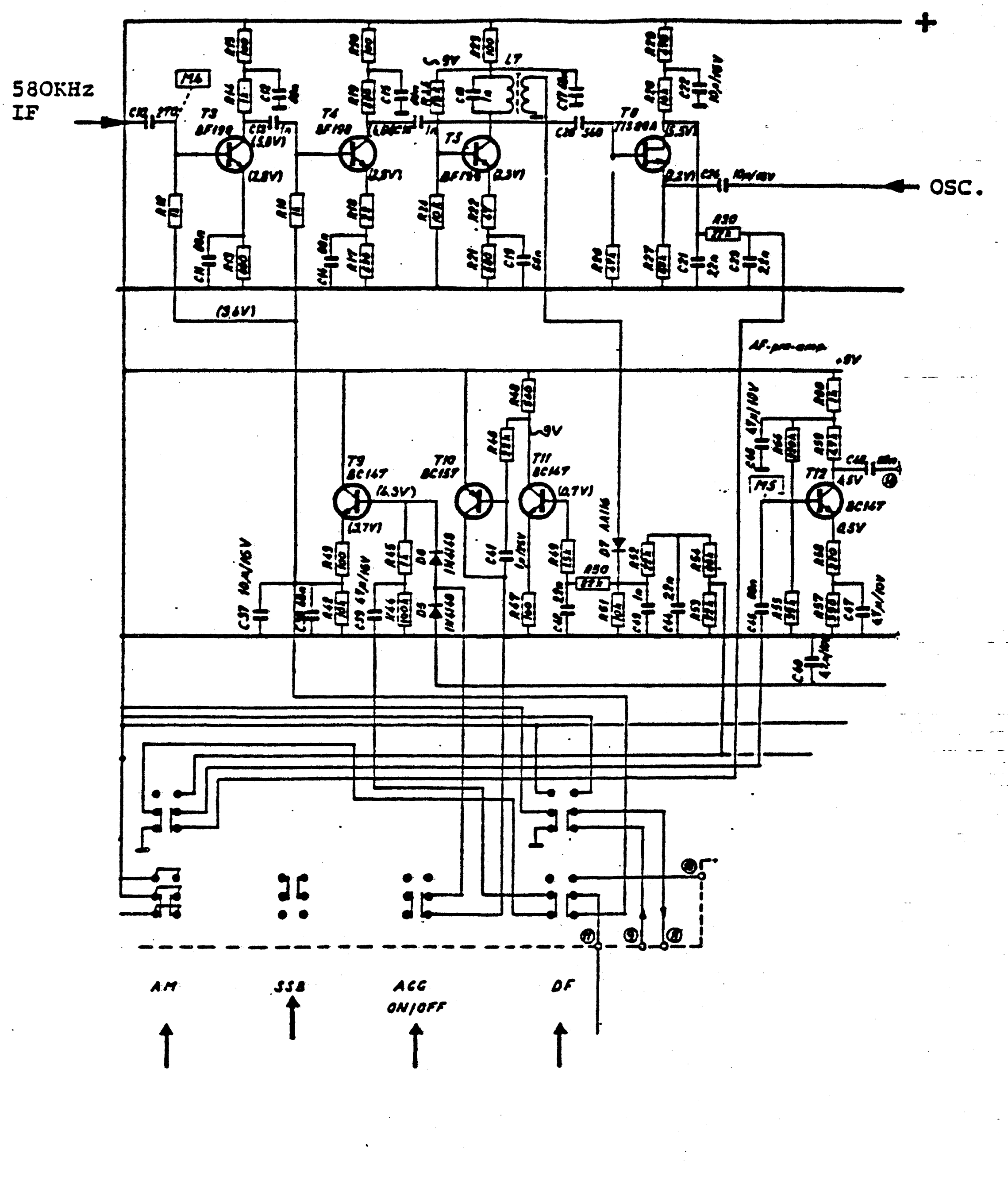
Sailor.



C26
1nF
R33
330Ω
+
Q5
BF185
Q6
BF185
R28
22KΩ
8V
8V
2,5V
2V
C23
47pF
10K Ω
R29
C24
250pF
10 Ω
R30
680Ω
R32
1,7V
TP14
C27
10n
10.245 MHz
C 25
125 pF
3,3KΩ
R31


C5
T2
TIS88A
R6
470
C2
68n
L7
L8
1,5-2,5V
C1
68n
1,5-2,5V
C4 100
P1
Balance
R3
470
ANT.
T1
TIS88A
D1-D4
4x 1N4148
D2
D4
D1
D3
R2
R5
C3 68n
OSC.
+


+
R238
5.6 k
R239
5.6 k
C233
0.047µ
C231
25µ
C232
25µ
C208
0.1µ
R237
50k
LF
R236
1k
C227
330p
C228
330p
60mV
M22
D201
AA119
C225
68p
AA119
D202
C224
330p
C223
0.1µ
L207
R229
470
5%
R230
470k
R226
1k
R227
220
18.4V
2.4
R228
1.2 k
C222
220p
Q204
BF 194
3.1 V
C221
4700p
C220
4700p
R224
47k
R223
10k
C219
4700p
5mV(2)
MF


580KHz
IF
OSC.
+
T3
BF198
T4
BF198
T5
BF198
T8
AF-pre-amp.
T9
BC147
T10
BC157
T11
BC147
T12
BC147
AM
SSB
AGC
ON/OFF
DF