Q1 ASSEMBLER - KARL'S VERSION I/O PROGRAMMING
8/78 VERSION
HAS COM1671 I/O INFO

1.0 System Board

1.1 Real-Time Clock (RTC) - I/O Address 00

OUT 00, 7 6 5 4 3 2 1 0

CONTROL

Bits 0 through 3

P3	P2	P1	P0	Programmable Clock Period - ms
0	0	0	0	1000.00
0	0	0	1	666.66
0	0	1	0	454.54
0	0	1	1	371.75
0	1	0	0	333.33
0	1	0	1	250.00
0	1	1	0	166.66
0	1	1	1	83.33
1	0	0	0	41.66
1	0	0	1	27.77
1	0	1	0	20.83
1	0	1	1	13.88
1	1	0	0	10.4166
1	1	0	1	6.944
1	1	1	0	5.20833
1	1	1	1	2.604166

Bit 4 = 1 Enable Clock
= 0 Disable Clock

Bits 5 through 7: Don't Care

IN 00, 7 6 5 4 3 2 1 0
This instruction reads the status of the real-time clock.

STATUS
Bit 0 = 1, Clock Mark

INTERRUPT
The real-time clock issues an Interrupt request as bit 0 goes to one. Bit 0 is reset to 0 after status is read.

PROGRAMMING
Output control word with bit 4 set to 0 to disable and reset RTC Input status to reset bit 0, clock mark.

Output control word with bit 4 set to 1 and code for desired clock period in bits 0 through 3.

The clock period need only to be programmed once for each rate desired. The first interrupt will occur at 1/2 the programmed clock period. Subsequent interrupts will occur at the programmed period. The clock will continue to run regardless if status is read or not.

1.2 Serial I/O Unit - address 10,11

1.2.1 OUT 10, 7 6 5 4 3 2 1 0

CONTROL

1.2.1.1 Register Select: Bit 3 = 0

A-REGISTER

7 6 5 4 3 S2 S1 S0	
0 0 0 0 0 0 0 0	Select Control Register 1 for read or write.
0 0 0 0 0 0 0 1	Reset interrupt line. The following special sequence of instructions is required: LI,A 1 OUT 010 OUT 010 IN 011
0 0 0 0 0 0 1 0	Select Control Register 2 for read or write.
0 0 0 0 0 1 0 0	Select Status Register for read, or Syn & DLE Register.
0 0 0 0 0 1 1 0	Select RCVR Holding Register for read, or TRANS Holding Register for write.

1.2.1.2 Mode Control: Bit 3 = 1 (DOES RESET TO COM16T1 CHIP IF SET)

A-REGISTER

R3 R2 R1 R0 3 2 I1 I0

Bit 0 (1_0) = 1 EIA/MIL 188 voltage or teletype current loop interface.
Bit 1 (1_0) = 1 Tristate interface.
Bit 2 = Don't care.
Bits 4 through 7 – Baud rate, (R_0 R_3)

R3	R2	R1	R0	BAUD RATE
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	200
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1,200
1	0	0	1	1,800
1	0	1	0	2,400
1	0	1	1	3,600
1	1	0	0	4,800
1	1	0	1	7,200
1	1	1	0	9,600
1	1	1	1	19,200

1.2.2 OUT 11, 7 6 5 4 3 2 1 0
Write into Register Selected by previous OUT 10

1.2.3 IN 11, 7 6 5 4 3 2 1 0
Read Register Selected by previous OUT 10

1.3 Serial I/O Register Format

1.3.1 Control Register 1 – S0 = 0
S1 = 0
S2 = 0

Bit 0
Controls data terminal ready line
= 1 Enables carrier and data set ready interrupts
= 0 Enables only ring indicator interrupt

Bit 1

Controls request to send line

= 1 with clear to send true enables transmitter and allows transmitter holding register empty (THRE) interrupts to be generated.

= 0 disables transmitter and turns off request to send line. Any character in the transmitter register will be completely transmitted before transmitter is turned off.

Bit 2

= 1 enables Serial I/O to receive data into receiver holding register, update receiver status bits 1, 2, 3, and 4 (see status register format), and to generate data received interrupts.

= 0 disables receiver and clears the receiver status bits.

Bit 3

A) In the asynchronous mode, a logical 1 enables checking of parity on received data and generaltion of parity for transmitted data.

B) In the synchronous mode, a logical 1 enables check of parity on received data only.

Bit 4

A) In the asychronous mode, a logical 1 enables the echoplex mode.

B) In the synchronous mode, a logical 1 enables stripping of received DLE Character; also parity checking is disabled.

Bit 5

A) In the asynchronous mode, Bit 5 controls the number of stop bits to be transmitted:

= 1 with transmitter enabled, causes a single stop bit to be transmitted.

= 0 causes 2-STOP Bit transmission for character length of 6, 7, or 8 bit, and one-and-a half stop bits for character length of 5.

B) In the synchronous mode:

= 1 with bit 6=0, enables transmit parity, otherwise no parity is generated.

= 1 with bit 6=1, the content of the DLE register is transmitted prior to the next character loaded in the transmitter holding register as part of the transmit transparent mode.

Bit 6

A) controls break condition in the asynchronous mode.

= 1 holds transmitted data in a space condition, starting at the end of any current transmitted character.

B) Controls transparent transmission in the synchronous mode.

= 1 enables transparent transmission, idle transmitter time will be filled with DLE-SYN character transmission and a DLE can be forced ahead of any character in the transmitter holding register (see bit 5 above.)

Bit 7

= 0 configures the Serial I/O into an internal data and control loop mode and disables the ring interrupt. In this diagnostic mode, the following loops are connected internally.

1. Transmit data connected to received data
2. DTR control line connected to DSR Input
3. RTS connected to CTS and carrier detector

= 1 enables ring interrupts and returns Serial I/O to normal configuration.

1.3.2 Control Register 2 - S0 = 0
S1 = 1
S2 = 0

Bits 0, 1 & 2
Control transmitter and receiver clocks

2 1 0	
0 0 0	Selects remote 1X clock for the receiver & transmitter
0 0 1	Selects 32X clock provided by the programmable baud rate generator
0 1 0	Selects transmitter clock input as remote 32X clock.

All other combinations of Bits 0, 1, and 2 are invalid.

Bit 3

A) In the asynchronous mode, this bit must = 1.

B) In the synchronous mode, a logical 1 causes all DLE and SYNC characters in the transparent mode to be stripped and no data received interrupt to be issued. the SYNC detect status bit it set with reception of the next assembled byte.

Bit 4

= 1 selects odd parity)
= 0 selects even parity) When parity is enabled

Bit 5

= 0 selects asynchronous character mode
= 1 selects synchronous character mode

Bits 6 and 7
Controls character length:

Bits

7 6	Character length
0 0	8 bits
0 1	7 bits
1 0	7 bits
1 1	5 bits

1.3.3 Status Register (Read Only) - S0 = 0
S1 = 0
S2 = 1

Bit 0
= 1 transmitter holding register is empty (THRE) while the transmitter is enabled.

Bit 1
= 1 data received, receiver holding register contains an assembled character, if the receiver is enabled.

Bit 2
= 1 overrun error

Bit 3
= 1 indicate previous character was DLE if DLE strip is enabled (Bit 4 of control Register 1), otherwise indicates last character received contained parity error if receiver parity (Bit 3 of control register 1) is also enabled.

Bit 4
= 1 indicates framing error in asynchronous mode.

= 1 indicates SYN character received in synchronous mode.

Bit 5
= 1 indicated carrier detected.

Bit 6
= 1 indicates data set ready.

Bit 7
= 1 indicates a change in status of data set ready or carrier detector input while data terminal ready (bit 0 of control register 1) is a logical 1, or the ring indicator is turned on with DTR a logical 0.

Inputting from the receiving holding register, S0 = 0, S1 = 1, S2 = 1, clears the data ready status Bit 1.

Outputting to the transmitter holding register, S0 = 0, S1 = 1, S2 = 1, clears the THRE status Bit 0.

Outputting to S0 = 0, S1 = 0, S3 = 1, loads both the SYN and DLE registers. After writing into SYN register, the Serial I/O is conditioned to write into the DLE if S0 = 0, S1 = 0, S2 = 1 is addressed again prior to another write operation. Any intervening read or write operation with other addresses resets this condition such that the next S0 = 0, S1 = 0, S2 = 1, selects will address the SYN register.

1.4 Serial I/O Interrupts

The following conditions generate interrupts:

1. Data received
2. Transmitter holding register empty
3. Data carrier goes on and DTR is on
4. Data carrier goes off and DTR is on
5. Data set ready goes on and DTR is on
6. Data set ready goes off and DTR is on
7. Ring indicator goes on and DTR is off

2.0 Keyboard Display Interface
Address 01

The keyboard is an input/output device. It is an electronic unit which produces a subtle audible click when a key is depressed. Each key position generates an eight-bit code with the exception of the four shift keys and a repeat key. The repeat key inputs the code of a previously depressed key at an approximate rate of ten characters per second.

MODE SHIFTING

Depressing the alpha key or the unshifted condition produces Mode 1. Keys depressed in Mode 1 will cause the keyboard to output codes corresponding to the lower case, or unshifted, characters depicted on the keytops.

Depressing the shift or shift lock keys produces Mode 2. This keyboard mode is indicated by the illumination of the shift lock keytop. Keys depressed in Mode 2 will cause the keyboard to output codes corresponding to the upper case, or shifted, characters depicted on the keytops.

Depressing the third numeric shift key produces Mode 3. This keyboard mode is indicated by the illumination of the third numeric keytop. Keys depressed in Mode 3 will cause the keyboard to output codes corresponding to the upper lengths depicted on the keytops.

Depressing the fourth shift key produces Mode 4. This keyboard mode is indicated by the illumination of the fourth shift keytop. Keys depressed in Mode 4 will cause the keyboard to output codes corresponding to additional special characters. Depressing a shift or control shift key will reset the shift lock. All shift modes can externally programmed; however, depressing shift keys will over-ride this external control.

IN,01

Loads the A-register with a data byte from the keyboard buffer, and clears the buffer to a hexadecimal 00 .

OUT,01

Keyboard Control

In the A-register, the status bit assignments are:

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7 6 5 4 3 2 1 0
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Bit 0 - Click: keyboard produces an audible click

Bit 1 - Beep: keyboard produces an audible beep

Bit 2) In combination, control the shift keys and
Bit 3) keyboard mode. See table below.

Bit 4 - Illuminates K1 keytop

Bit 5 - Illuminates K2 keytop

Bit 6 - Illuminates K3 keytops

Bit 7 - Illuminates insert mode keytop

Bit 3	Bit 2	Alpha	Shift	Third	Fourth	Mode
0	0	X	OFF	OFF	OFF	1
0	1	OFF	X	OFF	OFF	2
1	0	OFF	OFF	X	OFF	3
1	1	OFF	OFF	OFF	X	4
X	X	ON	OFF	OFF	OFF	1
X	X	OFF	ON	OFF	OFF	2
X	X	OFF	OFF	ON	OFF	3
X	X	OFF	OFF	OFF	ON	4

Keyboard Interrupts
The keyboard attempts to interrupt the processor whenever a key is depressed.

Display

Address 03,04

The display is an output device. It is a fully buffered electronic unit, capable of displaying up to 12 lines of data under program control. Each line contains a minimum of 47 character positions. Each character code is seven bits long. When a data byte is written from the processor to the display, the high-order bit is ignored. After one line is filled, the next character will automatically appear in position 1 of the next line.

To write a character on the display, address the device and output the first character. Control instructions may be issued to reset the display to character position 1 of line 1, nondistructively blank or restore the display, or step the display to the next character position.

OUT,03
Writes a character on the display

IN,04
Status
Bit 6 = 0 for 12 line = 1 for 6 line
Bit 5 = 1 for LITE; = 0 for LMC

OUT,04
Display Control
The control bit assignments for the A-register are:

7 6 5 4 3 2 1 0

Bit 0 - Reset: resets display to leftmost position of line 1

Bit 1 - Blank: display is blanked, but display buffer is not erased

Bit 2 - Unblank: buffer contents restored to display

Bit 3 - Step: character position is advanced one space to the right or to position 1 of the next line if prior position was at the end of a line

3.0 Printer Interface

Serial Impact Printer - Address 05,06,07
Separate addresses are used for printing and paper or carriage motion as follows.

OUT,05
Print Character

IN,05
Status
The printer status byte has the following format:

7 6 5 4 3 2 1 0

Bit 5 - Out of ribbon if bit = 1

Bit 6 - Error occured if bit = 1

Bit 7 - Printer busy if bit = 1

OUT,06

Moves the carriage in a direction determined by a previous OUT,07. The number of increments moved is normally determined by a 10 bit number. The low-order 8 bits are the contents of the A-register when OUT,06 is given. The highest two bits are the lowest two bits of the A-register when a previous OUT,07 is given. The increments are 1/48 of an inch in the vertical direction and 1/60 of an inch in the horizontal direction.

OUT,07

7 6 5 4 3 2 1 0

Bit 0)
Bit 1) - See OUT,06

Bit 2 - 0 = Forward Motion; 1 = Reverse Motion

Bit 3 - 0 = Carriage Motion; 1 = Paper Motion

Bit 4 - Lower ribbon

Bit 5 - Raise ribbon

Bit 6 - Provides expanded horizontal resolution of 1/120 of an inch

Bit 7 - Resets the printer and the interface electronics and moves the carriage to the extreme left position. Should be used before any other commands are given to the printer. It should also be used when an error condition occurs.

Printer Interrupts
The printer is ready to accept data or control instructions when bit 7 of the status byte = 0. The printer interrupts as bit 7 becomes 0.

3.2 DOT MATRIX PRINTER

OUT 08 with bit 7 = 0
Printer character or control command

OUT 08 with bit 7 = 1

IN 08
STATUS

Bit 0 - Printer Selected

Bit 1-4 = zero

Bit 5 - Paper Out

Bit 6 - Fault

Bit 7 - Busy

4.0 Disk Controller Board

Address 09,0A,0B

The Q1 single and double density disk have 77 tracks with from 8 to 511 bytes per record. The rotational speed of the disk is 360 r.p.m. It has a recording density of 3200 bpi on single density and 6400 bpi on double density and a data transfer rate of 250 kilobits per second and 500 kilobits per second for the single density disks respectively. Quad density disks have 154 tracks with the same recording density and transfer rate as the double density disks.

IN,09

Read Data

This instruction transfers one parallel byte of data from the disk controller to the processor's accumulator.

OUT,09

Write Data

This instruction transfers one parallel byte of data from the A-register to the disk controller.

IN,0A

Status

This instruction makes disk unit status information available for interrogation by the processor. The format of the status byte is:

7 6 5 4 3 2 1 0

Bit 0 - Parallel multiplexor busy

Bit 1 - Equals a one if a double sided disk is up to a speed in a quad density drive.

Bit 2 - 0

Bit 3 - 0

Bit 4 - Track 0: The selected drive's head is located at track 0

Bit 5 - INDEX: = 1 when index hole passes under photodetector

Bit 6 - SD Ready: The selected disk is loaded properly and is up to speed

Bit 7 - Busy: AMDET - controller has detected an address mark

OUT,0A

Disk Control 1

This instruction in conjuction with the contents of the A-register, selects the appropriate disk within the system, or performs a step track.

A-Register

7 6 5 4 3 2 1 0

Bit 0 - Select drive 1 and load head

Bit 1 - Select drive 2 and load head

Bit 2 - Select drive 3 and load head

Bit 3 - Select drive 4 and load head

Bit 4 - Select drive 5 and load head

Bit 5 - Select drive 6 and load head

Bit 6 - Select drive 7 and load head

Bit 7 - Select side 1 (Don't care on 800 drives)

OUT,0B

Disk Control 2

This instruction, in conjuction with the contents of the A-register, initiates either a read, or write operation.

A-register

7 6 5 4 3 2 1 0

Bit 0 thru 3 - Don't care

Bit 4 - Single density: sets controller to read single density

Bit 5 - 1 step

Bit 6 - 1 up direction for step track

Bit 7 - Write gate: sets controller and drive for write operation.

Disk Interrupt
The disk controller does not use the interrupt system. The controller is busy during a step or write operation.