SERVICE MANUAL

With price

SYSTEM UNIT

FP-1000/FP-1100 (GX-205)

JANUARY 1983

CASIO®

This service manual has been published to support you in understanding of the electrical circuit and its performance in the hardware of Casio FP-1000/1100 personal computers. However, we recommend that you study the theory of the Z80 microprocessor logic and the other Casio reference manuals published separately in conjunction with this service manual for easy and definite understanding of the central processing unit.

CONTENTS

1. INTRODUCTION

1) System Outline:

This system unit (Central Process Unit) consists of two logic printed circuit boards. One is called the main circuit board on which the main CPU μPD780C-1 (Z80A compatible) as the main system microprocessor is located, and the other is called the sub circuit board on which the sub CPU μPD7801G as a supplement to the main CPU is located. Such a system is called a dual process system, which enables high speed processing and extensive external memory.

2) Main Logic Printed Circuit Board:

The main CPU controls and performs various calculations, logic operations and general interfaces along with the sub CPU.
64K bytes capacity of dynamic-type RAM has been used to reduce the number of components and simplify the entire system.
In the 36K bytes of the ROM memory, the C82-BASIC language interpreter has been written for the BASIC language programming mode. The contents in the ROM memory is transferred to the RAM memory area as soon as the unit power switch is turned on. In other words, a computer operator can access to the C82-BASIC programming immediately without creating a trouble.
For external peripheral devices, the interface is divided in two ways causing various peripheral devices such as ROM/RAM memory packs, general purpose expansion box, display units, mini floppy disk drive, etc. to be connected for expandable memory.

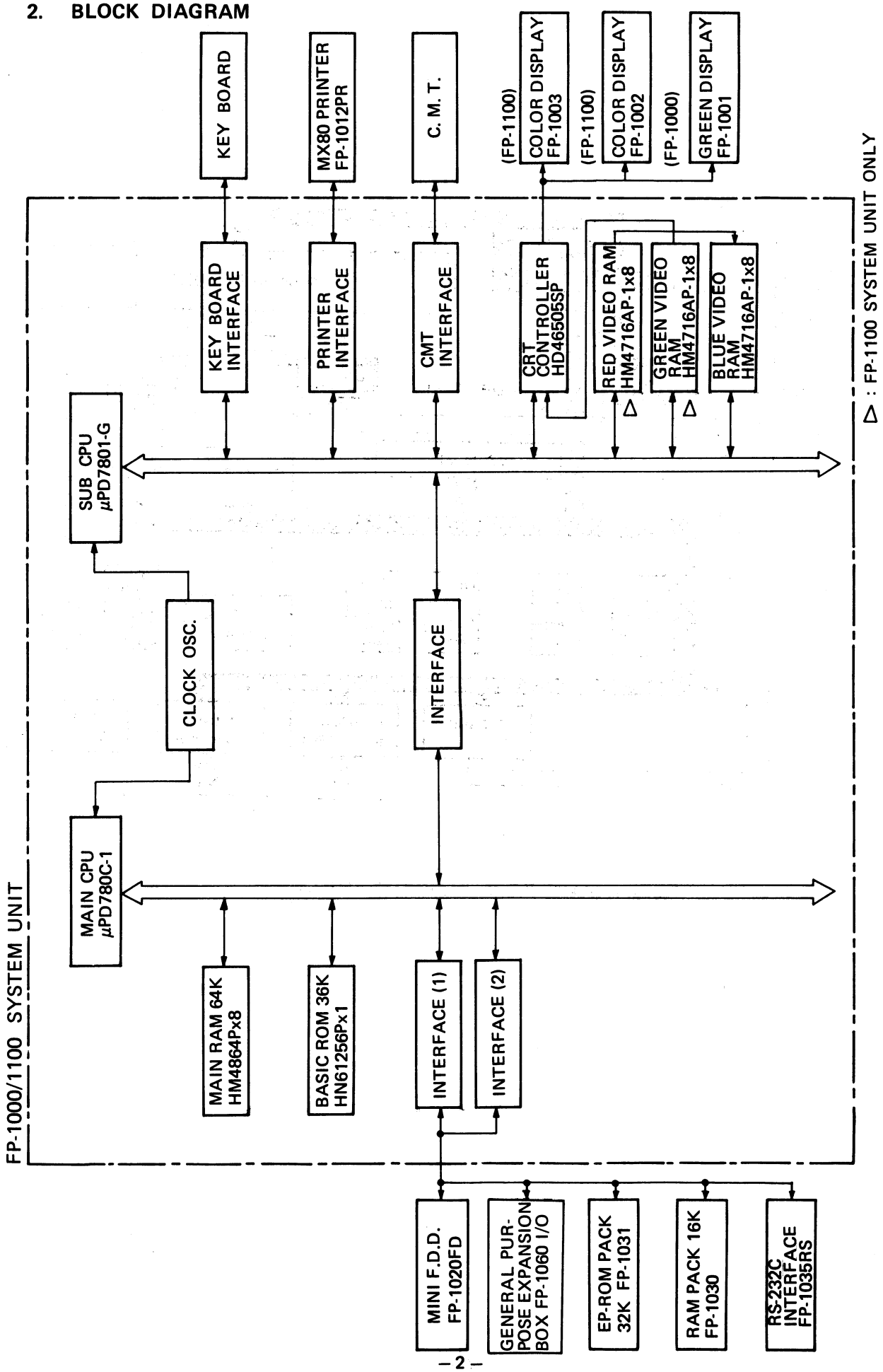
3) Sub Logic Printed Circuit Board:

On this sub printer circuit board is the sub CPU μPD780G-1. Its main function controls various peripheral devices connected externally through the interfaces along with the main CPU.
Also one of the major circuits located on this P.C.B. is the video RAM circuit which reserves 48K bytes of memory capacity for the color display signal or 16K bytes of memory capacity for the green display signal respectively.
It makes display of 80 characters in the horizontal and 25 lines in the vertical direction, and 640 dots in the horizontal and 200 dots in the vertical for the high resolution graphic mode.
A built-in CMT control circuit and graphic printer I/O (Centronix compatible) circuit can be connected to a cassette tape player for saving data or program and a graphic printer for hard copy directly without installing an intermediate device.

4) Optional Peripheral Devices:

Various optional peripheral devices can be provided for a suitable system.
With one Casio FP-1060IO general purpose expansion box, a maximum of 4 ROM memory packs or RAM memory packs (any combination of RAM and ROM packs allowed), or up to 8 packs with two general purpose expansion boxes can be installed. However, connecting one general purpose expansion box with another general expansion box cannot be done.
For external memory, a maximum of 4 units (4 FP-1020 FD) mini floppy disk drives can be connected by using 2 general purpose expansion boxes. Though one general purpose expansion box is able to connect 3 units of FP-1020FD (6 drives), it does not mean that 6 units of FP-1020 FD can be connected to one system unit by using two general purpose expansion boxes. Therefore, the CPU can access a total of 8 disks ON-LINE.

2. BLOCK DIAGRAM



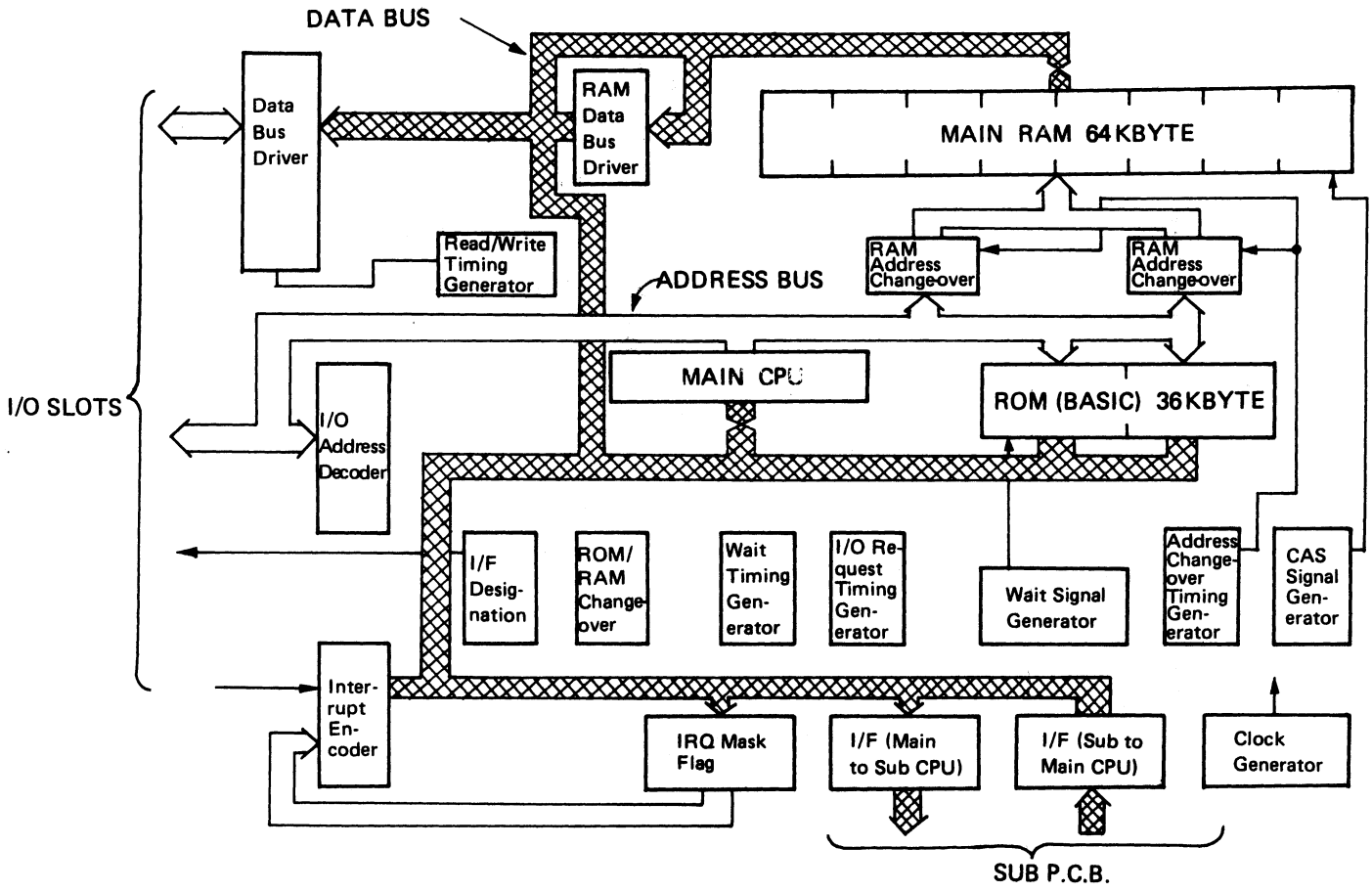


Fig. 2-1 MAIN P.C.B. BLOCK DIAGRAM

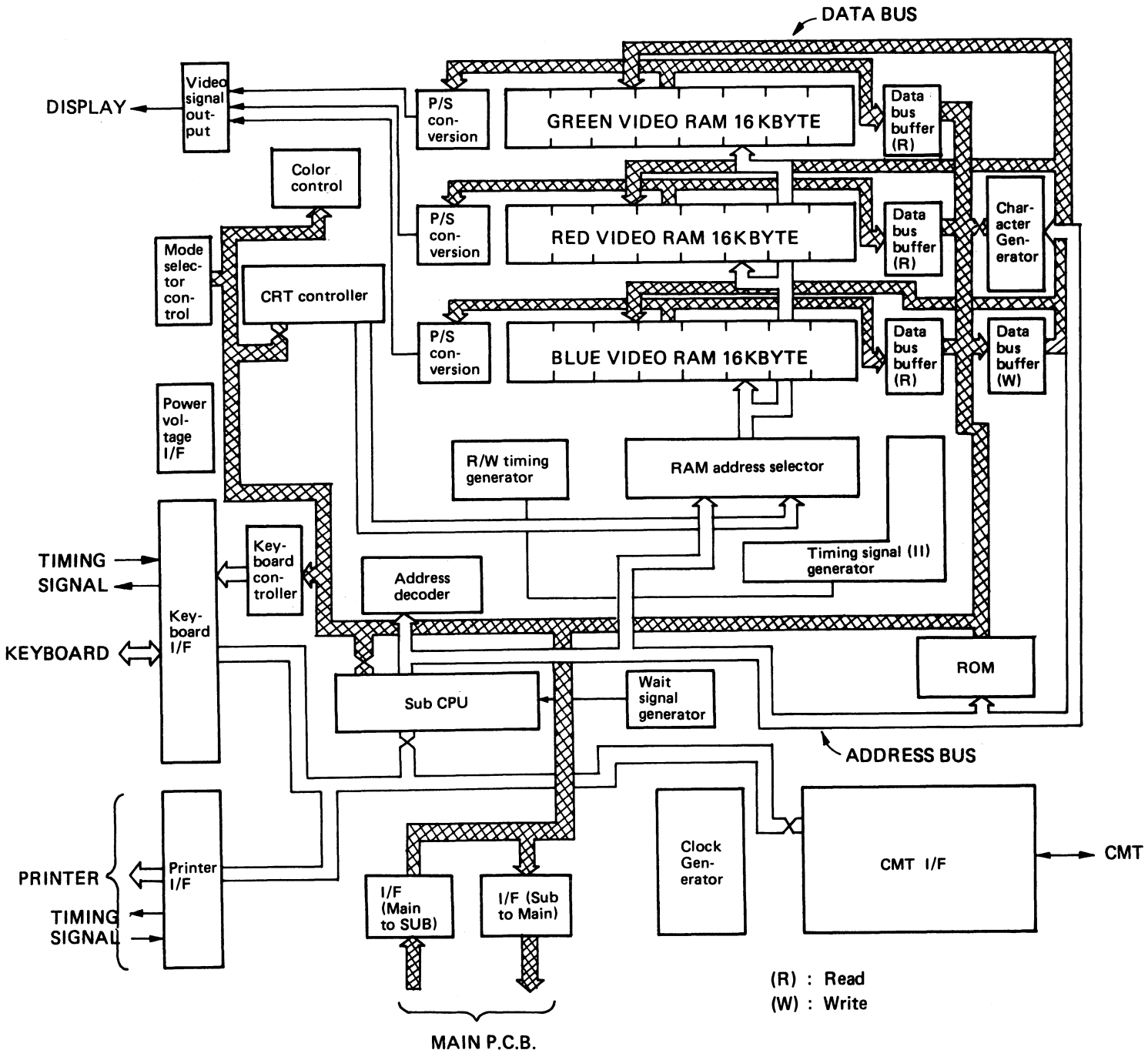


Fig. 2-2 SUB P.C.B. BLOCK DIAGRAM

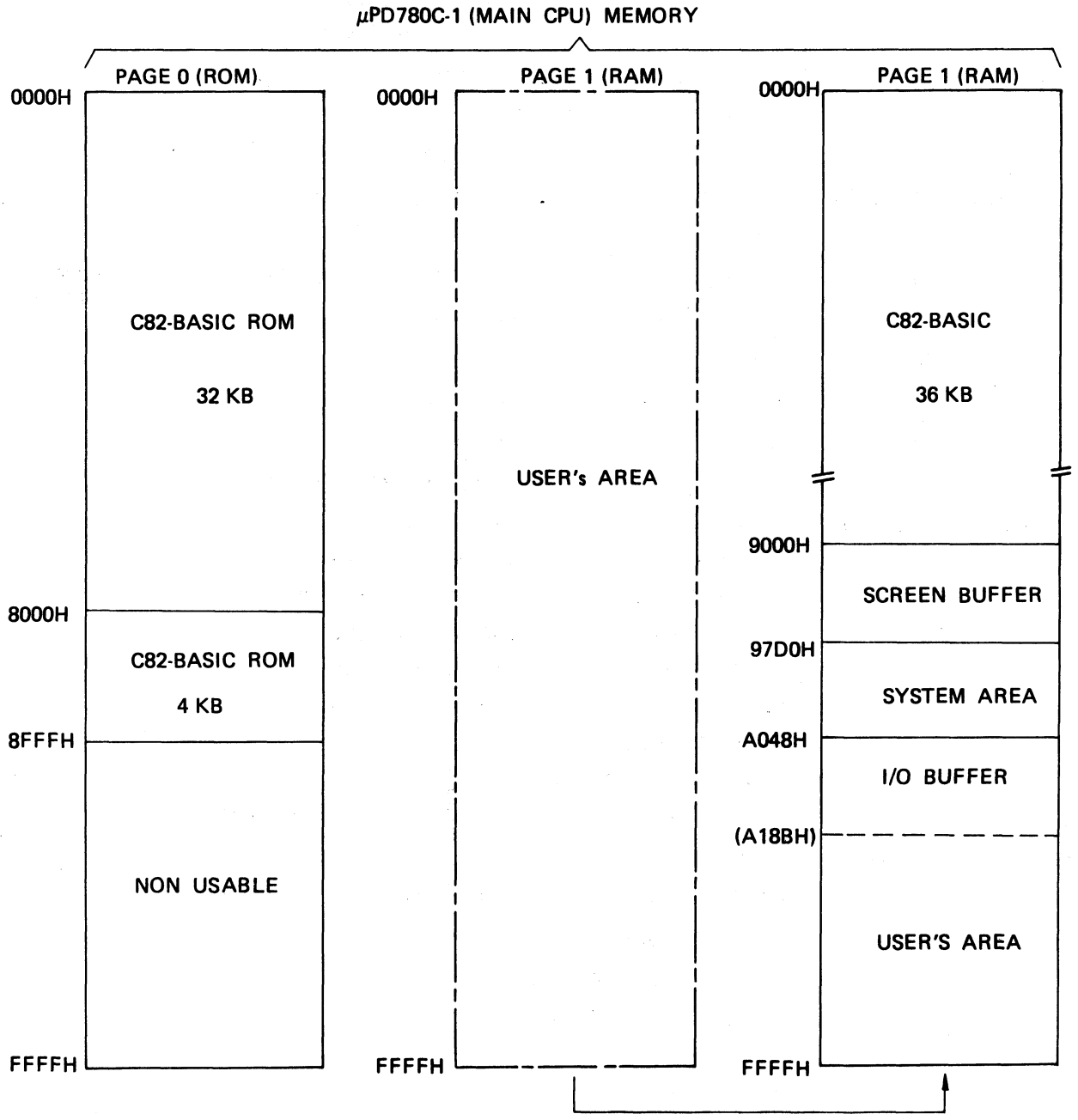
3. SPECIFICATIONS

DEVICE	MODEL NO.	DESCRIPTION
SYSTEM UNIT	FP-1000 FP-1100	MAIN CPU CHIP : μPD780C-1 (Z80A COMPATIBLE, 4 MHz) SUB CPU CHIP : μPD780G-1 (8-BIT MICROPROCESSOR) MEMORY ROM : MAIN 32KBYTE SUB 4KBYTE RAM : MAIN 64KBYTE SUB 48KBYTE (FP-1100, VIDEO RAM) 16KBYTE (FP-1000, VIDEO RAM) CRT CONTROLLER : HD46505SP DIMENSIONS : 450mm (W) x 310mm (D) x 85mm (H) CPU 450mm (W) x 220.5mm (D) x 71mm (H) KEYBOARD POWER SOURCE : 100, 117, 220, 230, or 240 ACV POWER CONSUMPTION : 49W, MAXIMUM 70W WEIGHT : 10.1 KG (CPU UNIT AND KEYBOARD)
DISPLAY	FP-1001	INPUT SIGNAL : COMPOSITE COLOR : GREEN (MONO COLOR) CRT SIZE : 12 INCH DISPLAY CHARACTERS : 80/40 CHARACTERS x 25 LINES (2000/1000 CHARACTERS) RESOLUTION : HIGH RESOLUTION 640 (H) x 200 (V) DOTS DIMENSIONS : 317mm (W) x 379mm (H) x 322mm (D) POWER SOURCE : 100/120/230 POWER CONSUMPTION : 29W
	FP-1002	INPUT SIGNAL : R.G.B. (SEPARATE) COLORS : 8 COLORS, RED, BLUE, GREEN, YELLOW, CYAN, MAGENTA, WHITE, BLACK CRT SIZE : 14 INCH DISPLAY CHARACTERS : 40 CHARACTERS x 25 LINES (1000 CHARACTERS) RESOLUTION : 320 (H) x 200 (V) DOTS, MEDIUM DIMENSIONS : 366mm (W) x 422mm (H) x 380mm (D) POWER SOURCE : 100/120/230 POWER CONSUMPTION : 55W
	FP-1003	INPUT SIGNAL : R.G.B. (SEPARATE) COLORS : 8 COLORS, RED, BLUE, GREEN, YELLOW, CYAN, MAGENTA, WHITE, BLACK CRT SIZE : 14 INCH DISPLAY CHARACTERS : 80/40 CHARACTERS x 25 LINES (2000/1000 CHARACTERS)

		RESOLUTION	: 640 (H) x 400 (V) DOTS (MONO COLOR) 320 (H) x 200 (V) DOTS (FULL COLOR) HIGH RESOLUTION
		POWER SOURCE	: 100/120/230
		POWER CONSUMPTION	: 68W
		DIMENSIONS	: 366mm (W) x 422mm (H) x 380mm (D)
EXTERNAL MEMORY	FP-1020FD	DISK SIZE	: 5.25 INCH, TWO SIDE
		CAPACITY	: 320KBYTE (UNFORMAT) x 2 DRIVES
	CMT	INTERFACE	: FSK (FREQUENCY SHIFT KEYING), "0"=1,200, "1"=2,400 Hz
		BAUD RATES	: 300/1200
	FP-1030	CHIP	: C-MOS RAM
		MEMORY CAPACITY	: 16KBYTE (MAXIMUM 128KBYTE)
	FP-1031	CHIP	: EP-ROM
		CAPACITY	: MAXIMUM 32KBYTE PER PACK
PRINTER	FP-1012PR	PRINTER TYPE	: EPSON TYPE 3
		PAPER WIDTH	: 101.6mm ~ 254mm (4" ~ 10")
		PRINTING SPEED	: 80 CPS (NORMAL SIZE)
		DIGIT NUMBER	: 80/40/132/66 DIGITS
		CHARACTERS	: ASCII COMPATIBLE
		INTERFACE	: CENTRONIX COMPATIBLE
		POWER SOURCE	:
		POWER CONSUMPTION	:
		DIMENSIONS	: 374 (W) x 107 (H) x 305mm (D)
OTHER	FP-1035RS	INTERFACE	: RS-232C COMPATIBLE
		BAUD RATES	: 150/300/600/1200/2400/4800/9600
MANUAL		OPERATION MANUAL C82-BASIC REFERENCE MANUAL GUIDE TO FP-1000/1100 HARDWARE MANUAL SERVICE MANUAL	

NOTE: For further details of specifications, refer to each peripheral device service manual or operation manual.

4. MEMORY MAP



As soon as the power switch is turned on, memory in the page 1 (RAM) is allocated this way.

Screen Buffer:

Data which is displayed on the screen is stored in this memory area and the screen edition is executed to data in this screen buffer.

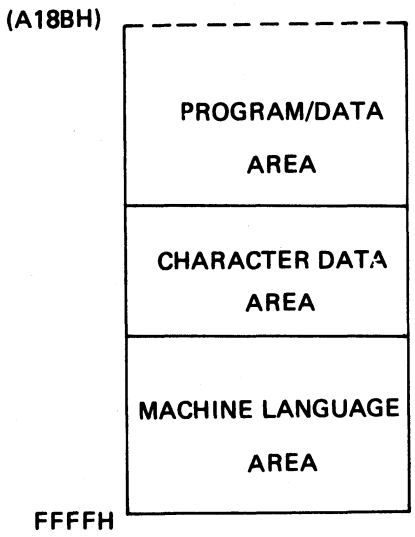
System Area:

Refer to the work area which the C82-BASIC utilizes.

I/O Buffer:

This memory area is used as input and output buffer. It varies depending upon the MOUNT sentence.

User's Area:
User can use this area for storing data or program. It is stored from the forefront address of the memory area. The forefront address is stored at 9DE8H and 9DE9H addresses. The area is allocated for program/data area, character data area and machine language area from the forefront of the area.

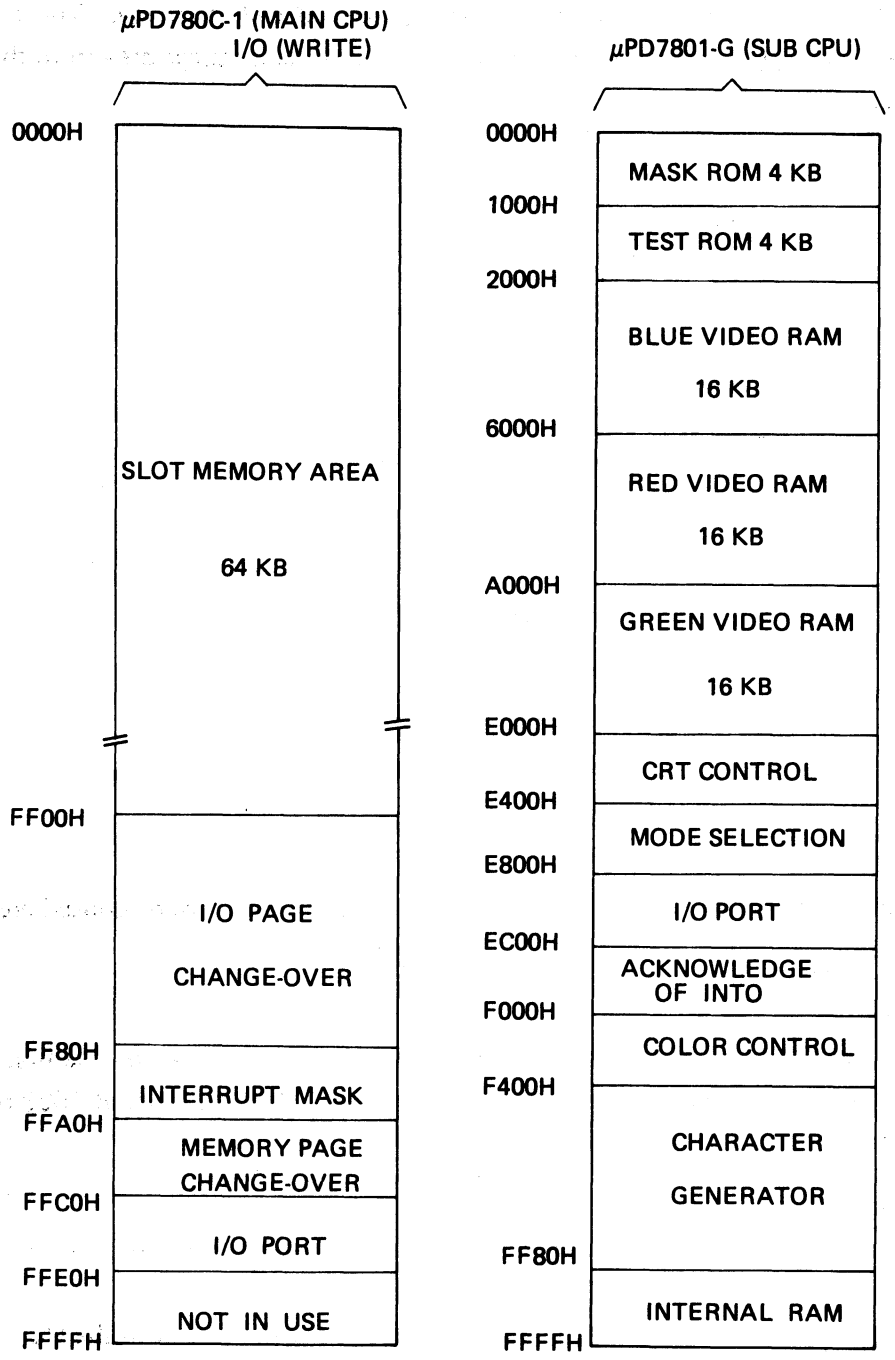


Program/Data Area:
The program and data written by the BASIC are stored in this area. Size of unused area can be obtained by the FREE function.

Character Data Area:
The character variable value is stored in this area. The area is programmed by the first parameter in the CLEAR sentence. After the power switch is turned on, this area is set at 1023 byte.
The size of unused area can be obtained by the FREE function.

Machine Language Area:
The BASIC is not able to control this area, and machine language sub routine, etc. is stored in the area.
The forefront address of the machine language area is second parameter+1 in the CLEAR sentence.

As Input "CLEAR A, B":
The forefront address of the machine language area is B+1 and the forefront address of the character data area is B−A+1.


μPD780C-1 (MAIN CPU)
I/O (WRITE)
0000H
SLOT MEMORY AREA
64 KB
FF00H
I/O PAGE
CHANGE-OVER
FF80H
INTERRUPT MASK
FFA0H
MEMORY PAGE
CHANGE-OVER
FFC0H
I/O PORT
FFE0H
NOT IN USE
FFFFH
μPD7801-G (SUB CPU)
0000H
MASK ROM 4 KB
1000H
TEST ROM 4 KB
2000H
BLUE VIDEO RAM
16 KB
6000H
RED VIDEO RAM
16 KB
A000H
GREEN VIDEO RAM
16 KB
E000H
CRT CONTROL
E400H
MODE SELECTION
E800H
I/O PORT
EC00H
ACKNOWLEDGE
OF INTO
F000H
COLOR CONTROL
F400H
CHARACTER
GENERATOR
FF80H
INTERNAL RAM
FFFFH

FUNCTION	ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
I/O PAGE CHANGE-OVER	FF00-FF7F	W	–	–	–	–	D3	D2	D1	D0
INTERRUPT MASK	FF80-FF9F	W	SUBINT	–	–	INTS	INTD	INTC	INTB	INTA
MEMORY PAGE CHANGE-OVER	FFA0-FFBF	W	–	–	–	–	–	–	Page change-over	I/F DESIG-NATION
DATA TRANSFER TO SUB CPU	FFC0-FFDF	W	D7	D6	D5	D4	D3	D2	D1	D0
PERIPHERAL DEVICE DESIGNATION	FF00-FF7F	R	D7	D6	D5	D4	D3	D2	D1	D0
DATA TRANSFER FROM SUB CPU	FF80-FFFF	R	D7	D6	D5	D4	D3	D2	D1	D0

I/O MEMORY MAP (MAIN CPU)

FUNCTION	ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
MASKED ROM IN SUB CPU	0000-0FFF	R	D7	D6	D5	D4	D3	D2	D1	D0
TEST ROM	1000-1FFF	R	D7	D6	D5	D4	D3	D2	D1	D0
BLUE VIDEO RAM	2000-5FFF	R/W	D7	D6	D5	D4	D3	D2	D1	D0
RED VIDEO RAM	6000-9FFF	R/W	D7	D6	D5	D4	D3	D2	D1	D0
GREEN VIDEO RAM	A000-DFFF	R/W	D7	D6	D5	D4	D3	D2	D1	D0
DESIGNATION OF CONTROL REGISTER IN HD46505	E000	W	–	–	–	D4	D3	D2	D1	D0
CONTROL REGISTER IN HD46505	E001	R/W	D7	D6	D5	D4	D3	D2	D1	D0
ACCESSING CRT CONTROL	E000-E3FF	*	*	*	*	*	*	*	*	*
MODE SELECTION	E400-E7FF	R	–	–	SW6	SW5	SW4	SW3	SW2	SW1
KEYBOARD CONTROL	E400-E7FF	W	–	–	Key input enable	Buzzer con-trol	D3	D2	D1	D0
DATA TRANSFER FROM MAIN CPU	E800-EBFF	R	D7	D6	D5	D4	D3	D2	D1	D0
DATA TRANSFER TO MAIN CPU	D800-EBFF	W	D7	D6	D5	D4	D3	D2	D1	D0
ACKNOWLEDGE OF INTO	EC00-EFFF	W	–	–	–	–	–	–	–	–
COLOR CONTROL	F000-F3FF	W	D7	D6	D5	D4	D3	D2	D1	D0
CHARACTER GENERATOR	F400-FF7F	R	D7	D6	D5	D4	D3	D2	D1	D0
RAM IN SUB CPU	FF80-FFFF	R/W	D7	D6	D5	D4	D3	D2	D1	D0

SUB CPU MEMORY MAP

4-1. EP-ROM MEMORY PACK

The EP-ROM memory pack can store program and data up to maximum 32KB.
The same method as the RAM memory pack for loading program and data is adopted.
Application program by BASIC and machine languages, data and constants, can often be saved and loaded by using the BASIC commands such as INP, PACI, PACO or LOAD "PACKO", etc.
There are 4 pcs. of 28-pin sockets on the circuit board of the EP-ROM memory pack which EP-ROMs can be mounted on. Though 3 different types of EP-ROM are available for the memory pack, a mixture of these EP-ROMs is not permitted.
To install EP-ROMs type 2732 and 2764, short pad A and open pad B on the circuit board and vice versa for type 2716.
The 24-pin dip configuration of 2716 and 2732 types must be mounted on the 28-pin socket in the following manner. When less than 4 pcs. of the ROMs are mounted on the circuit board, they must be mounted in order of A, B, C and D.

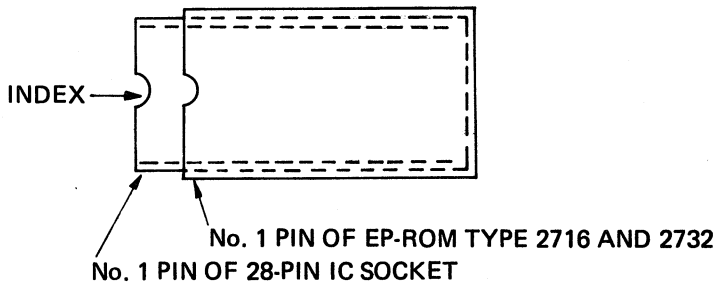


Fig. 4-1 IC SOCKET CONFIGURATION

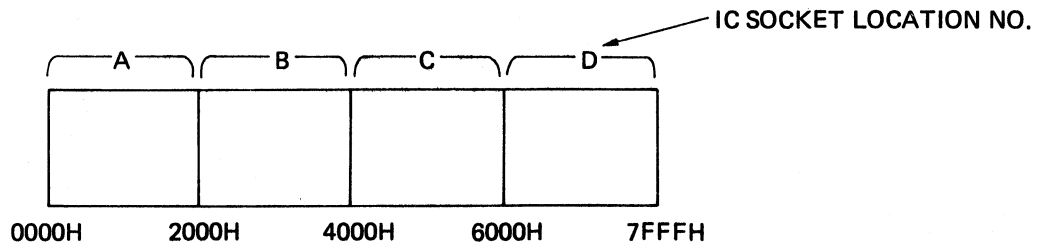


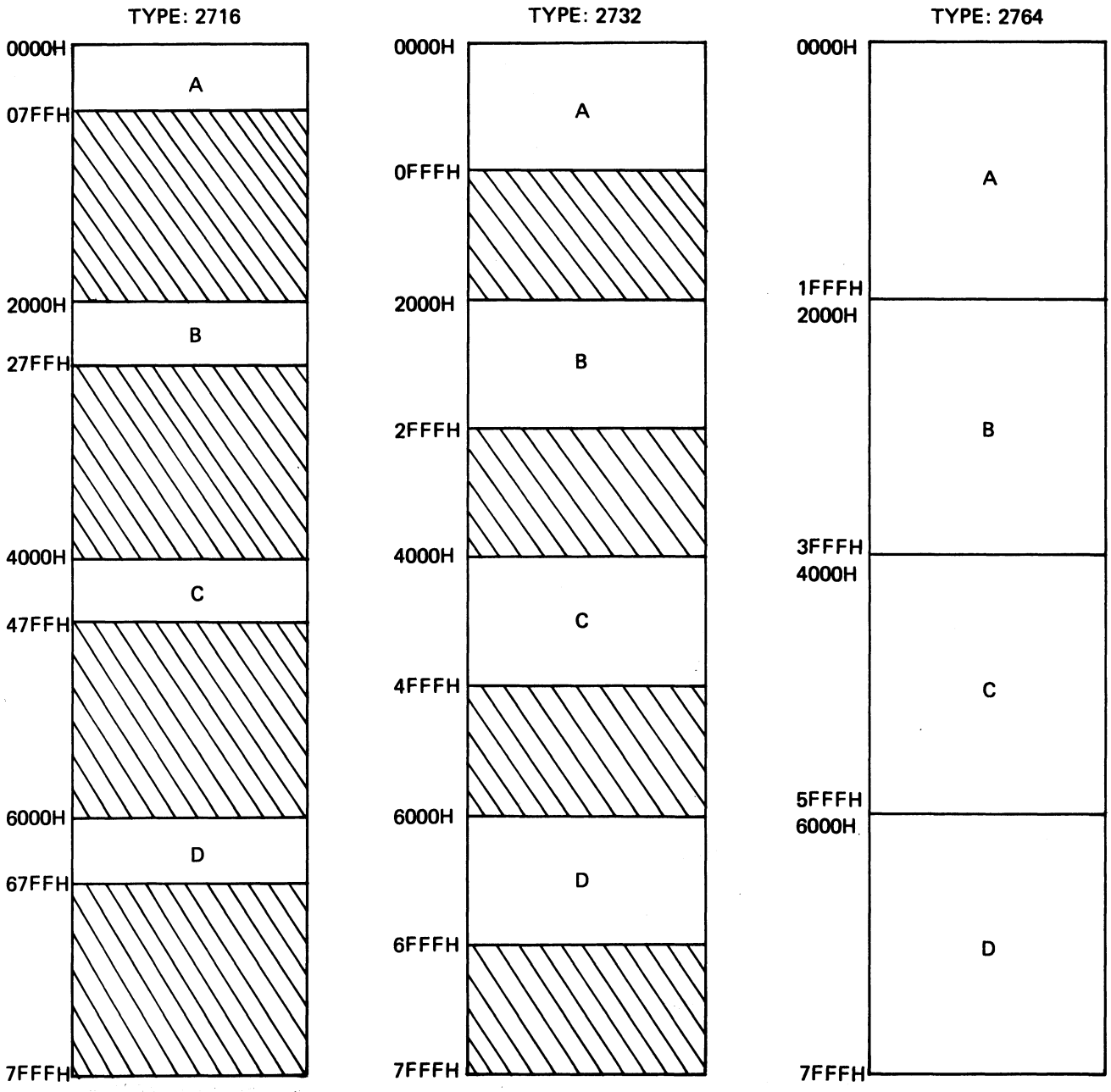
Fig. 4-2 MEMORY ADDRESS ALLOCATION

NOTE: For details of the EP-ROM memory allocation, refer to the "MEMORY MAP FOR EP-ROM PACK"at page 12.

4-2. MEMORY MAP FOR EP-ROM PACK (FP-1031)

ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0000-7FFF	R	D7	D6	D5	D4	D3	D2	D1	D0

I/O MEMORY MAP FOR EP-ROM PACK (32KBYTES)



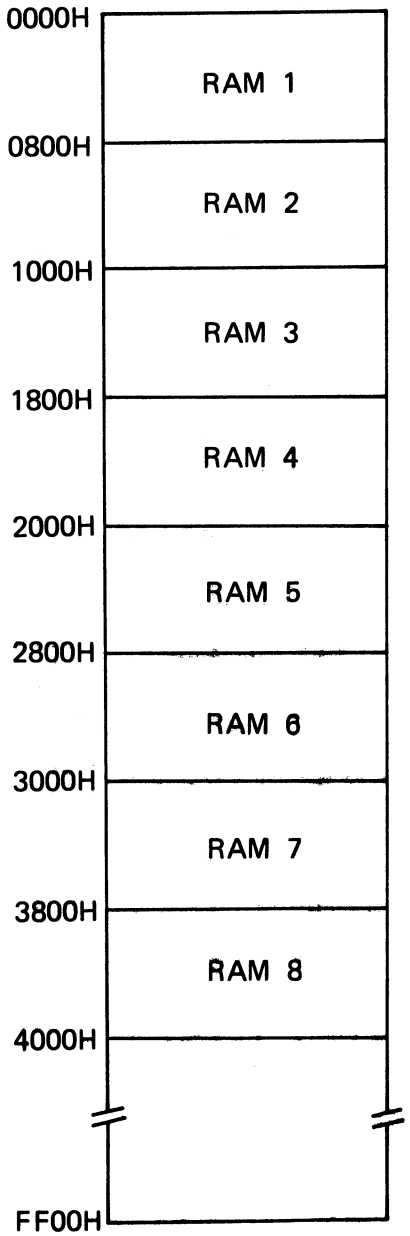
NOTE: 1. A, B, C and D in the above memory maps indicate socket locations on the circuit board of the EP-ROM memory pack.

2. Shadow areas in the above memory maps are non-usable areas.

4-3. MEMORY MAP FOR CMOS RAM PACK (FP-1030)

ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0000-3FFF	R/W	D7	D6	D5	D4	D3	D2	D1	D0

I/O MEMORY ADDRESS FOR C-16K MEMORY PACK (16KBYTES)

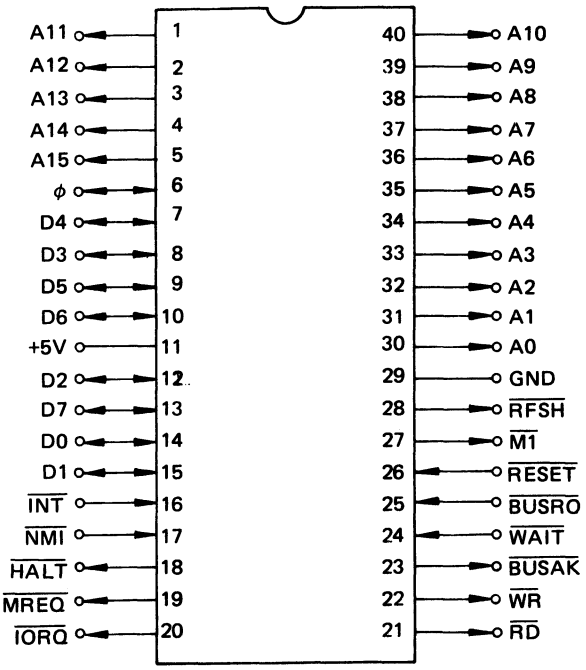


NOTE: RAM 1, RAM 2 . . . RAM 8 in the above memory map designate each RAM chip on the circuit board of the C16K RAM memory pack.

5. CPU FUNCTIONAL DESCRIPTION

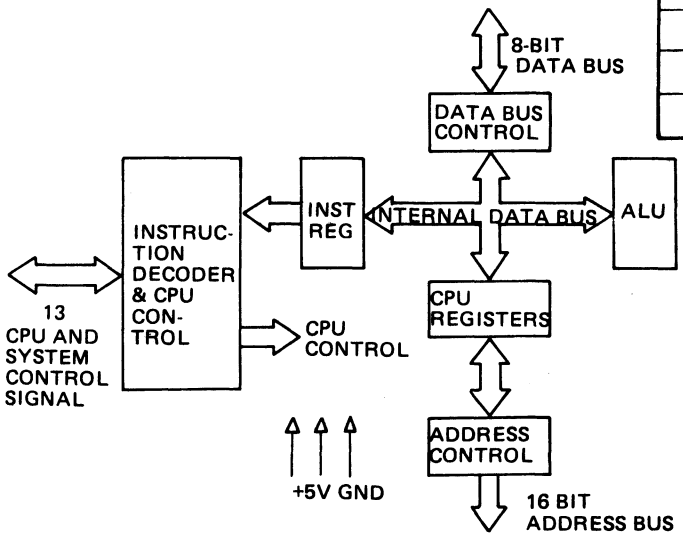
5-1. μPD780C-1 (MAIN CPU)

PIN ASSIGNMENT

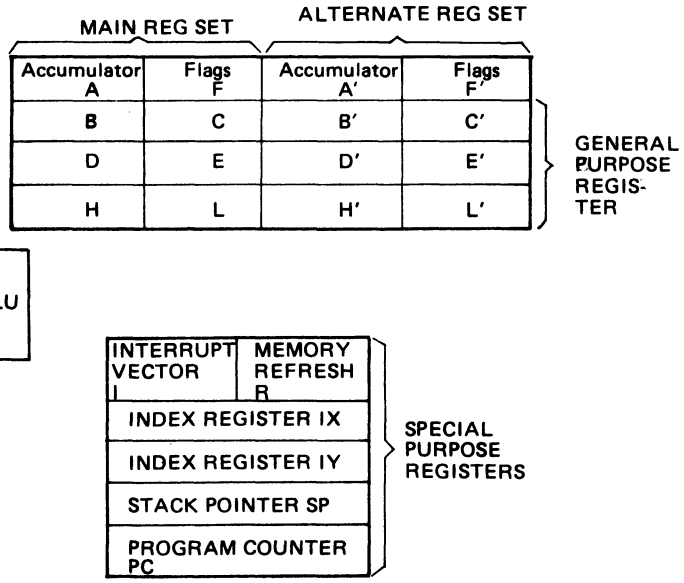


A0 ~ A15	:	Address bus
D0 ~ D7	:	Data bus
$\overline{M1}$	:	Machine cycle one
$\overline{MREQ}$	:	Memory request
$\overline{IORQ}$	:	Input/Output request
$\overline{RD}$	:	Read
$\overline{WR}$	:	Write
$\overline{RFSH}$	:	Refresh
$\overline{HALT}$	:	Halt state
$\overline{WAIT}$	:	Wait
$\overline{INT}$	:	Interrupt request
$\overline{NMI}$	:	Non maskable interrupt
$\overline{RESET}$	:	Reset
$\overline{BUSRQ}$	:	Bus request
$\overline{BUSAK}$	:	Bus acknowledge
φ	:	Clock
+5V	:	Power voltage, DC +5V
GND	:	Signal ground

BLOCK DIAGRAM



REGISTER CONFIGURATION



SIGNAL NAME	IN/OUT	DESCRIPTION
$\overline{HALT}$	O	This signal indicates that the CPU entered the HALT condition after execution of the HALT instruction. To come out of the HALT condition, the $\overline{INT}$ or the $\overline{NMI}$ or the $\overline{RESET}$ signal is necessary. The CPU executes the NOP instruction and repeats the memory refresh operation even it is in the HALT condition. Active when low.
$\overline{WAIT}$	I	While the $\overline{WAIT}$ signal is in active condition, the CPU holds its WAIT condition. Slow speed memory and I/O device can be connected directly to the CPU by utilizing this signal. The memory refresh does not occur during WAIT condition. Active when low.
$\overline{INT}$	I	This terminal is for the interrupt request signal. The CPU shifts to execution of the interrupt process program after the end of instruction process which the CPU is currently executing. Active when low.
$\overline{NMI}$	I	This terminal is for the non-maskable interrupt request signal. The CPU, without concerning interrupt permit condition, jumps over to address 0066 (16) after the end of instruction process which the CPU is currently executing when the $\overline{NMI}$ signal becomes active. The $\overline{NMI}$ signal has priority over the $\overline{INT}$ signal. Active at negative edge trigger.
$\overline{RESET}$	I	The CPU is reset when this signal becomes active. Active when low.
$\overline{BUSRQ}$	I	When the $\overline{BUSRQ}$ signal becomes active, the CPU sets the address bus (A0 ~ A15), data bus (D0 ~ D7) and the system control terminals ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$) of 3 states in high impedance after the end of instruction which is currently operating. Therefore, other devices can use the above stated external bus. Active when low.
$\overline{BUSAK}$	O	This signal indicates that the CPU has set the address bus, the data bus and the system-control terminals of 3 states in high impedance by receiving the $\overline{BUSRQ}$ signal. Active when low.
Ø	I	Single phase clock input terminal. +5 voltage level.
A0 ~ A15	O	These output terminals are 16-bit address bus and output the memory address and I/O device numbers. Also the refresh address is output to the lower 7 bits at the memory refresh. 3 states and active when high.

SIGNAL NAME	IN/OUT	DESCRIPTION
D0 ~ D7	I/O	8 bit-data bus and used for transfer data between the CPU and I/O device or between the CPU and memory. 3 states and active when high.
$\overline{M1}$	O	This signal indicates the machine cycle which it has begun to execute and is the OP code fetch cycle. Active when low.
$\overline{MREQ}$	O	This signal indicates that address information necessary for memory read and write is output to the address bus and it is output to be used to synchronize the memory refresh. 3 states and active when low.
$\overline{IORQ}$	O	During M1 cycle: This signal requests the outside to transmit the interrupt response vector through the data bus when the maskable interrupt is acknowledged. Other than M1 cycle: This signal indicates that I/O device number necessary for I/O read and write operations is output to the address bus. 3 states and active when low.
$\overline{RD}$	O	This signal indicates that the data bus is being input and, memory or I/O device transmit data to the CPU by synchronizing with it through data bus. 3 states and active when low.
$\overline{WR}$	O	This signal indicates that the data bus is being output and is used for transfer data to memory or I/O device through the data bus from the CPU by synchronizing with the signal. 3 states and active when low.
$\overline{RFSH}$	O	At M1 cycle, this signal indicates that the refresh address for dynamic RAM is being output to lower 7 bits of the address bus. The dynamic RAM is able to read the refresh address by utilizing the $\overline{MREQ}$ signal which is output simultaneously at time of $\overline{RFSH}$ signal output. Active when low.

THE REGISTERS IN μPD780C-1

Exclusive registers:

1) Program counter (PC) . . . 16 bits
   This register reserves 16-bit address information of program which is to be executed next.

2) Stack point (SP) . . . 16 bits
   This register reserves the forefront address information of the stack memory in external memory (RAM area).

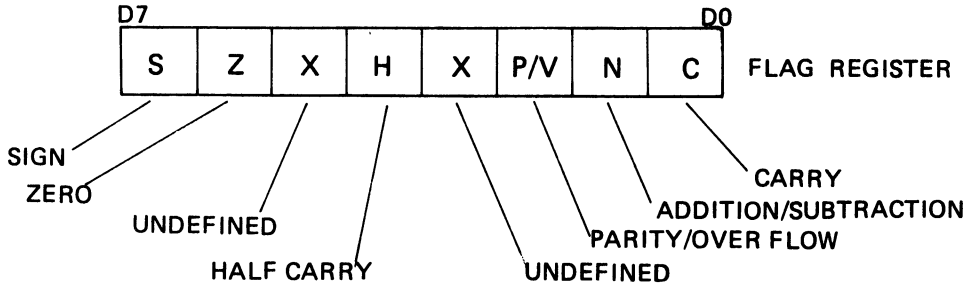
3) Index register (IX and IY) . . . 16 bits
   Both IX and IY index registers are 16-bit registers and used for index addressing.

4) Interrupt page address register (I) . . . 8 bits
   This register reserves higher 8 bits of indirect address used for the interrupt mode 2 among three different kinds of the interrupt modes (0, 1, 2).

5) Memory refresh register (R) . . . 7 bits
   This is a 7-bit register to reserve refresh address of dynamic RAM.

Accumulator (A, A') and Flag register (F, F') . . . 8 bits

This chip has 2 sets of accumulators A and A' (8 bits) and individual registers F and F' (8 bits) for each accumulator.
The accumulator reserves calculation results and the flag register reserves status which comes from the results of calculation.
Exchange between AF and AF' can be executed by the EX AF, AF' instruction.
Type of flag register is as follows.



GENERAL REGISTERS:

The chip has 2 sets (main and sub) of registers and each set consists of an 8-bit register (B, C, D, E, H, L or B', C', D', E', H', L'). They can be used as a pair of registers (BC, DE, HL or BC', DE', HL'). Exchange between the main and the sub register pairs is executed by the EXX instruction. Exchange between the contents in the DE and contents in the HL is executed by the EX DE, HL instruction.

TIMING

Instruction machine cycle of the μPD780C-1 is executed with the following three pairs of basic machine cycle.

Instruction OP code · fetch (M1 cycle)
Memory read/write · cycle
Input/output · cycle

Furthermore, the relation among machine cycle state and clock is as follows.

1 instruction · cycle = 2 ~ 6 machine cycles
1 machine · cycle (M) = 3 ~ 6 states
1 state (T) = 1 clock

1) Instruction OP code · fetch (M1 cycle) :
The OP code · fetch · cycle (M1 cycle) should be executed in front of each instruction cycle. After the M1 cycle is started, the contents of program counter (PC) are output to the address bus and $\overline{MREQ}$ signal becomes active after half the clock cycle. Because of this, the $\overline{MREQ}$ signal can be utilized directly as a chip select signal of the dynamic memory.
When $\overline{RD}$ signal becomes active, data (OP code) is output to the data bus so that the CPU reads the data at the rising edge of the clock at T3 state.
Reading and operation of the OP code are executed in the CPU at T3 and T4 and refresh signal ($\overline{RFSH}$) which refreshes external dynamic memory, and refresh address (A0 ~ A6) are output simultaneously.

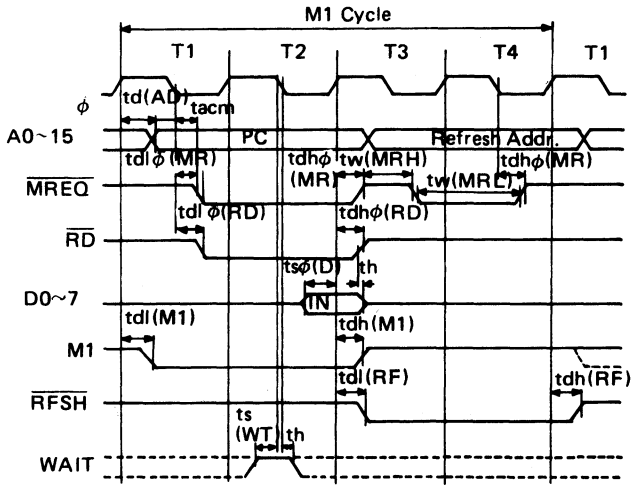


Fig. 5-1 INSTRUCTION FETCH CYCLE

2) Memory·read/write·cycle
In case the $\overline{WAIT}$ signal is not used at timing of read and write other than the OP code·fetch, the cycle ends in three states respectively.
The $\overline{MREQ}$ signal becomes active after address information is output (half clock later), so it can be directly utilized for the enable signal of dynamic memory.

Memory read cycle:

$\overline{MREQ}$ signal and $\overline{RD}$ signal are used the same as the fetch cycle. However, it reads data at falling edge of the clock at T3.

Memory write cycle:

$\overline{WR}$ signal becomes active after written data on data bus became stable, and the written data does not vary during the half clock after $\overline{WR}$ signal became inactive. So, $\overline{WR}$ signal can be utilized as R/W signal of semiconductor memory in general.

3) Input/output cycle

This cycle is executed for input and output commands. Wait state (Tw) is automatically enclosed in this cycle to sample the $\overline{WAIT}$ signal.

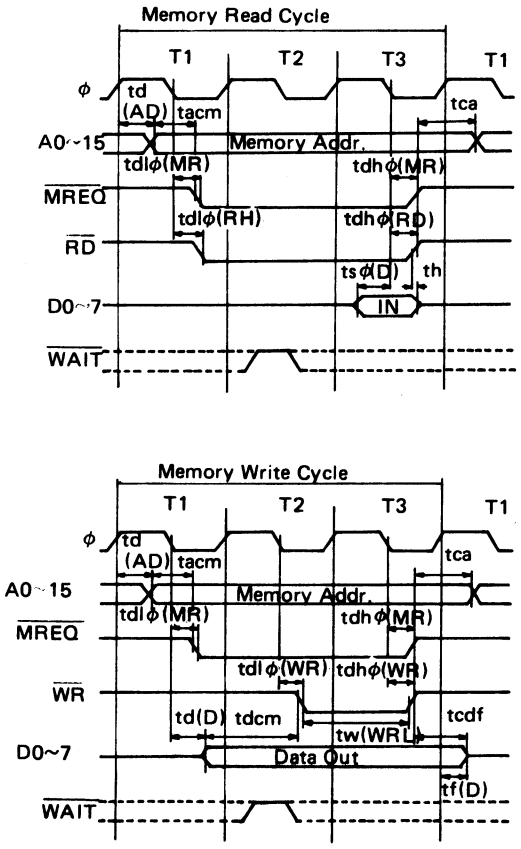


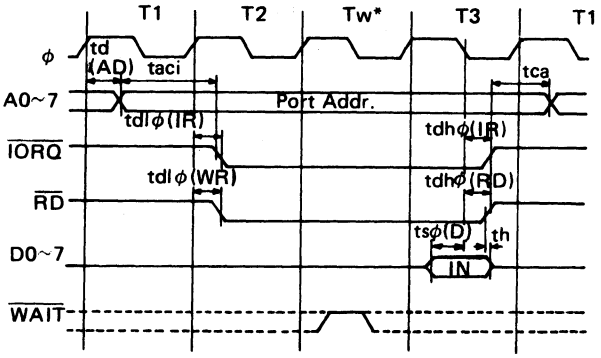
Fig. 5-2 MEMORY READ/WRITE CYCLE

I/O read cycle:

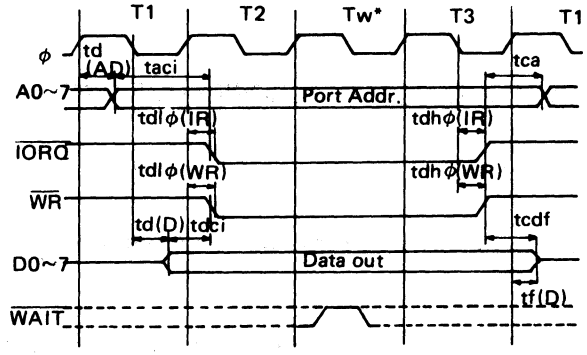
Data from an I/O device are input into the CPU at the falling edge of the clock at T3 state.

I/O write cycle:

I/O device takes in data on the data bus at the rising edge of $\overline{WR}$ signal because there are stable periods of written data at the front and back of the $\overline{WR}$ signal active period.



READ CYCLE



WRITE CYCLE

Fig. 5-3 I/O WRITE AND READ CYCLES

DMA FUNCTION

μPD780C-1 can disconnect bus from it for an external device when the request is made by external device.

Utilizing this function, direct data transfer between memory and an I/O without going through the CPU is possible. Such function is called direct memory access (DMA).

Request signal ($\overline{BUSRQ}$) is sampled at the rising edge of clock at the last state in each machine cycle and becomes bus request/acknowledge cycle. During this cycle, the following conditions occur.

1) A0 ~ A15, D0 ~ D7: in high impedance condition
2) Control signal of 3 states : in high impedance condition
3) $\overline{BUSAK}$: active
4) All interrupts are prohibited.
5) Memory refresh operation is stopped.

$\overline{BUSRQ}$ signal is always sampled at the rising edge of clock in bus request/acknowledge cycle, then the condition is released from the cycle when the signal becomes inactive.

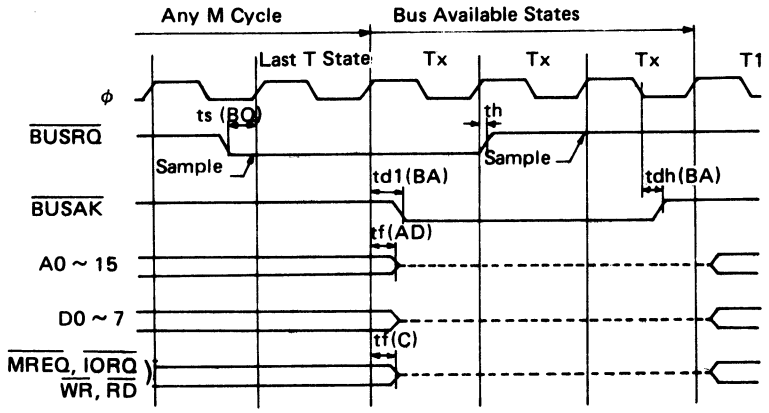


Fig. 5-4 BUS REQUEST/ACKNOWLEDGE CYCLE

INTERRUPT FUNCTION

μPD780C-1 has two interrupts, non-maskable interrupt and maskable interrupt.

1) Non-maskable interrupt

This interrupt cannot be masked by software and it saves the contents of the PC and the IFF (interrupt admit flip-flop) by $\overline{\text{NMI}}$ signal. Then jumps over to address 0066 (16) later on. $\overline{\text{NMI}}$ signal is sampled at the rising edge of clock at the last state of each instruction. The interrupt enters the interrupt process cycle if $\overline{\text{NMI}}$ signal is active.

At the interrupt process cycle, the interrupt executes the OP fetch-code during M1 cycle and it saves the contents of the PC and the IFF at M2 and M3. Then it automatically jumps over to address 0066 (16) after that.

After the end of non-maskable interrupt process, it can return contents of the PC and the IFF which were saved when the RETN instruction is executed.

2) Maskable interrupt

Interrupt can be masked by software and it cannot be accepted if one of the following conditions is met.

2-1. When non-maskable interrupt occurs simultaneously.
2-2. When $\overline{\text{BUSAK}}$ signal is active (low).
2-3. When the IFF is in reset condition.

Also, there are three different kinds of maskable interrupt. Each interrupt process is different from the others (the IFF can be reset by any mode).

Mode 0 :

It executes instruction read by M1 cycle. RST or CALL instruction is used as the execution instruction. The mode is set when IM 0 instruction is executed or the reset which resets the CPU occurs.

Mode 1 :

It saves the PC contents then jumps over to address 0038 (16). Mode 1 is designated by execution of IM 1 instruction.

Mode 2 :

It executes indirect call based on the contents of I register and read data.

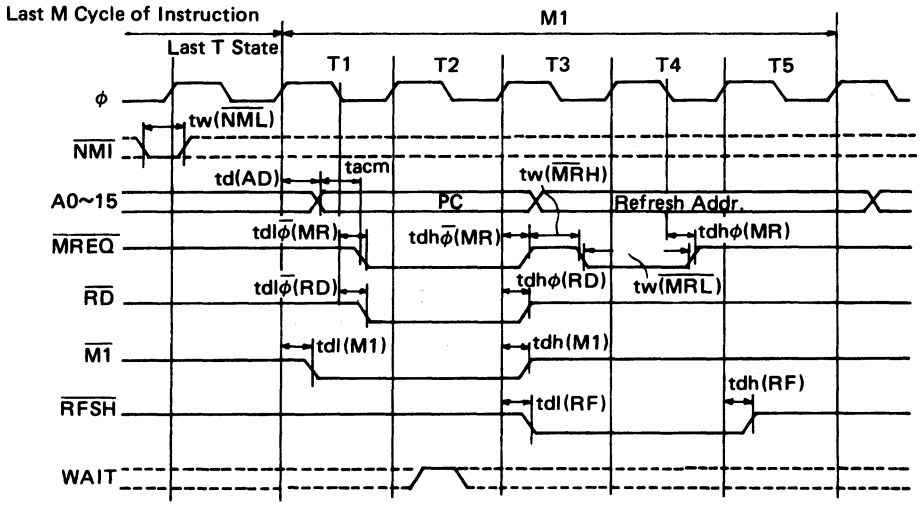
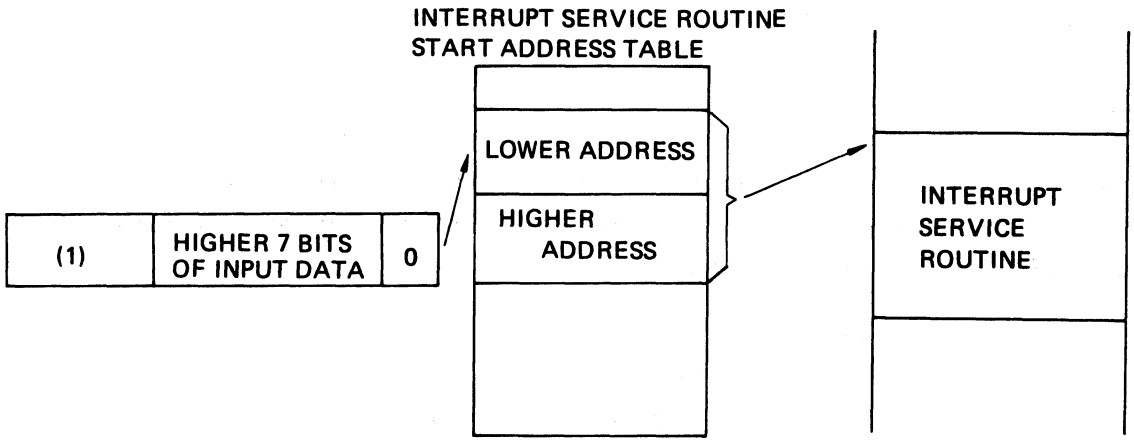


Fig. 5-5 NON-MASKABLE INTERRUPT REQUEST FUNCTION



First, start address table for interrupt service routine is accessed by 16 bits which consists of higher 8 bits of the I register content and lower 8 bits of read data (normally the lowest bit is 0). Second, it jumps over to interrupt service routine based on the contents of the selected start address table.

Mode 2 is designated by execution of IM 2 instruction.

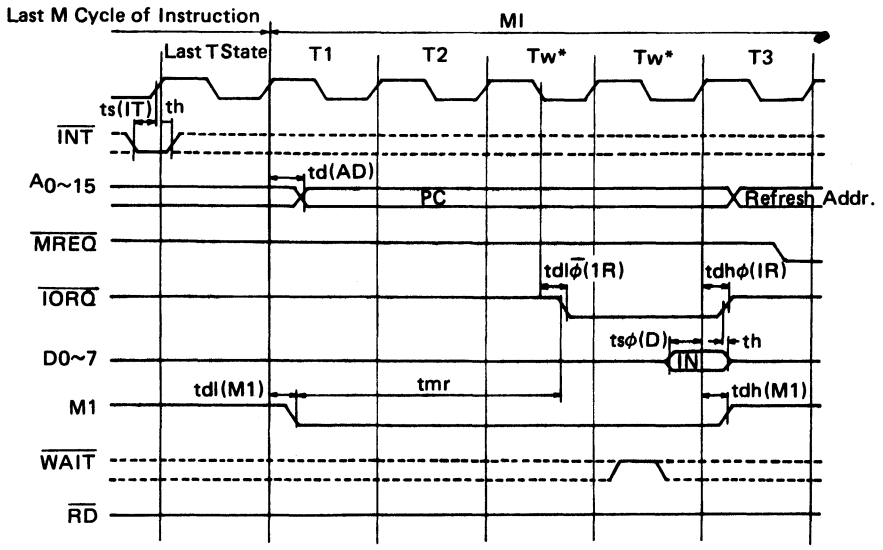


Fig. 5-6 INTERRUPT REQUEST/ACKNOWLEDGE-CYCLE

When $\overline{INT}$ signal becomes active, the signal is sampled at the rising edge of clock at the last state of each instruction and special M1 cycle of which two wait states (TW*) are added. It reads in data from surrounding area at the rising edge of T3 in M1 cycle and executes process with a mode which is selected by program in mode 0 ~ 2.

RESET FUNCTION

μPD780C-1 is reset when signal which is active for period of more than 3 clocks is input into the $\overline{RESET}$ terminal. Then the following conditions occur. Program will start from address 0000 (16) if the $\overline{RESET}$ input is released ("1") later on.

0000 ⟶ PC
0 ⟶ IFF
00 ⟶ I register and R register
Set interrupt mode 0
A0 ~ A15, D0 ~ D7 : high impedance condition
All control outputs : inactive condition

INSTRUCTION SET

μPD780C-1 instruction outline is listed at the following page.

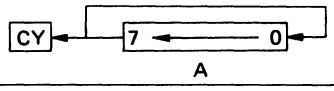
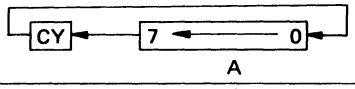
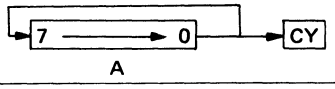
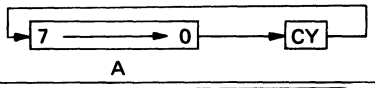
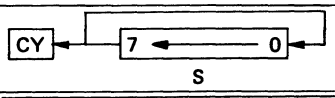
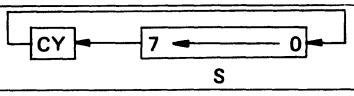
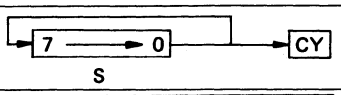
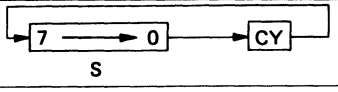
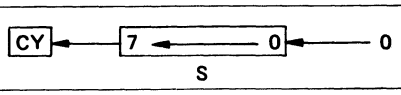
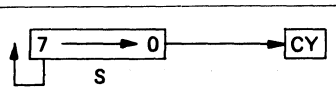
Symbol in the table

b ≡ 8-bit register or bit instruction of memory
cc ≡ flag term code
NZ ≡ non zero
Z ≡ zero
NC ≡ non carry
C ≡ carry
PO ≡ parity odd or no over-flow
PE ≡ parity even or over-flow
P ≡ positive
M ≡ negative (minus)
d ≡ 8-bit destination register or memory address
dd ≡ 16-bit destination register or memory address
e ≡ relative jump or displacement for index addressing
L ≡ call address by RST instruction (0, 8, 16 (10), 24 (10), 32 (10), 40 (10), 48 (10), 56 (10)
n ≡ 8-bit binary number or address
nn ≡ 16-bit binary number or address
r ≡ 8-bit general registers (A, B, C, D, E, H, L)
S ≡ 8-bit source register or memory address
Sh ≡ 8-bit register or memory bit "b" (0 ~ 7)
SS ≡ 16-bit source register or memory address
L ≡ lower 8 bits of 16-bit register
H ≡ higher 8 bits of 16-bit register
( ) ≡ content in memory or I/O port

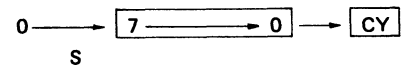
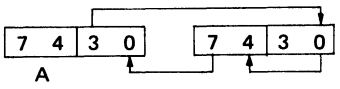
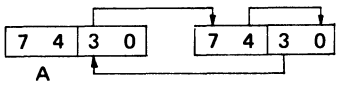
Addressing

(1) Immediate
(2) Immediate extended
(3) Modified page zero
(4) Relative
(5) Extended
(6) Indexed
(7) Register
(8) Implied
(9) Register indirect
(10) Bit

	MNEMONIC	SYMBOLIC OPERATION	COMMENT
8-BIT LOAD INSTRUCTION	LD r, s	r ← s	s ≡ r, n, (HL), (IX + e), (IY + e)
	LD d, r	d ← r	d ≡ (HL), (IX + e), (IY + e)
	LD d, n	d ← n	d ≡ (HL), (IX + e), (IY + e)
	LD A, s	A ← s	s ≡ (BC), (DE), (nn), I, R
	LD d, A	d ← A	d ≡ (BC), (DE), (nn), I, R
16-BIT LOAD INSTRUCTION	LD dd, nn	dd ← nn	dd ≡ BC, DE, HL, SP, IX, IY
	LD dd, (nn)	dd ← (nn)	dd ≡ BC, DE, HL, SP, IX, IY
	LD (nn), ss	(nn) ← ss	ss ≡ BC, DE, HL, SP, IX, IY
	LD SP, ss	SP ← ss	ss ≡ HL, IX, IY
	PUSH ss	$(SP-1) \leftarrow ss_H$; $(SP-2) \leftarrow ss_L$	ss ≡ BC, DE, HL, AF, IX, IY
	POP dd	$dd_L \leftarrow (SP)$; $dd_H \leftarrow (SP+1)$	dd ≡ BC, DE, HL, AF, IX, IY
EXCHANGE	EX DE, HL	DE ↔ HL	
	EX AF, AF'	AF ↔ AF'	
	EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	
	EX (SP), ss	$(SP) \leftrightarrow ss_L$, $(SP+1) \leftrightarrow ss_H$	ss ≡ HL, IX, IY
MEMORY BLOCK TRANSFER INSTRUCTION	LDI	(DE) ← (HL), DE ← DE + 1, HL ← HL + 1, BC ← BC − 1	
	LDIR	(DE) ← (HL), DE ← DE + 1, HL ← HL + 1, BC ← BC − 1, Repeat until BC = 0	
	LDD	(DE) ← (HL), DE ← DE − 1, HL ← HL − 1, BC ← BC − 1	
	LDDR	(DE) ← (HL), DE ← DE − 1, HL ← HL − 1, BC ← BC − 1, Repeat until BC = 0	
MEMORY BLOCK SEARCH	CPI	A − (HL), HL ← HL + 1, BC ← BC − 1	A − (HL) sets the flags only A is not affected
	CPIR	A − (HL), HL ← HL + 1, BC ← BC − 1 Repeat until BC = 0 or A = (HL)	
	CPD	A − (HL), HL ← HL − 1, BC ← BC − 1	
	CPDR	A − (HL), HL ← HL − 1, BC ← BC − 1, Repeat until BC = 0 or A = (HL)	
8-BIT CALCULATION INSTRUCTION	ADD A, s	A ← A + s	CY is the carry flag s ≡ r, n, (HL) (IX + e), (IY + e)
	ADC A, s	A ← A + s + CY	
	SUB s	A ← A − s	
	SBC A, s	A ← A − s − CY	
	AND s	A ← A ∧ s	
	OR s	A ← A ∨ s	
	XOR s	A ← A ⊕ s	
	CP s	A − s	
	INC d	d ← d + 1	d ≡ r, (HL) (IX + e), (IY + e)
	DEC d	d ← d − 1	

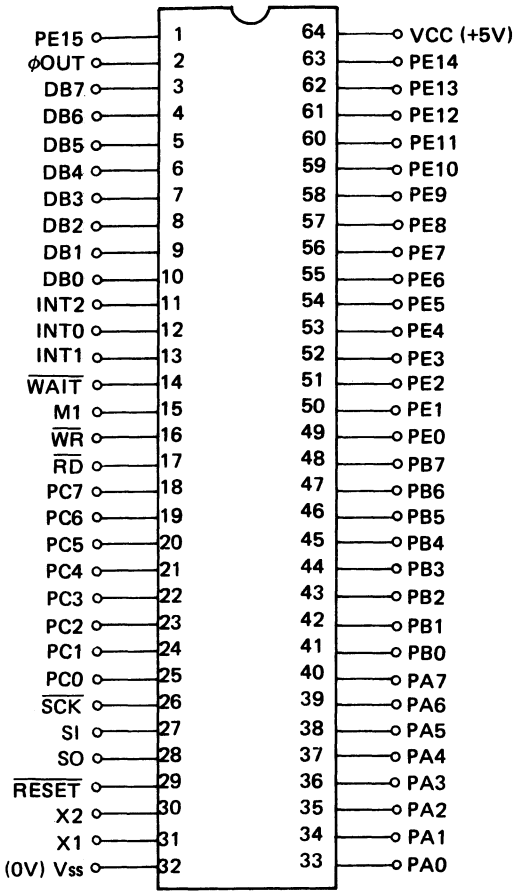
	MNEMONIC	SYMBOLIC OPERATION	COMMENT
16-BIT CALCULATION INSTRUCTION	ADD HL, ss	HL ← HL + ss	ss ≡ BC, DE, HL, SP
	ADC HL, ss	HL ← HL + ss + CY	
	SBC HL, ss	HL ← HL − ss − CY	
	ADD IX, ss	IX ← IX + ss	ss ≡ BC, DE, IX, SP
	ADD IY, ss	IY ← UY + ss	ss ≡ BC, DE, IY, SP
	INC dd	dd ← dd + 1	dd ≡ BC, DE, HL, SP, IX, IY
	DEC dd	dd ← dd − 1	dd ≡ BC, DE, HL, SP, IX, IY
OTHER OPERATION	DAA	Converts A contents into packed BCD following add or subtract.	Operands must be in packed BCD format
	CPL	$A \leftarrow \overline{A}$	
	NEG	A ← 00 − A	
	CCF	$CY \leftarrow \overline{CY}$	
	SCF	CY ← 1	
CPU CONTROL	NOP	No operation	
	HALT	Halt CPU	
	DI	Disable Interrupts	
	EI	Enable Interrupts	
	IM 0	Set interrupt mode 0	8080A mode
	IM 1	Set interrupt mode 1	Call to 0038H
	IM 2	Set interrupt mode 2	Indirect Call
ROTATION INSTRUCTION	RLCA		
	RLA		
	RRCA		
	RRA		
	RLC s		s ≡ r, (HL), (IX + e), (IY + e)
	RL s		
	RRC s		
	RR s		
	SLA s		
	SRA s		

CONTINUE . . .

	MNEMONIC	SYMBOLIC OPERATION	COMMENT
	SRL s		s ≡ r, (HL), (IX + e), (IY + e)
	RLD	 (HL)	
	RRD	 (HL)	
BIT FUNCTION	BIT b, s	$Z \leftarrow \overline{s_b}$	Z is zero flag s ≡ r, (HL), (IX +e), (IY +e)
	SET b, s	$s_b \leftarrow 1$	
	RES b, s	$s_b \leftarrow 0$	
INPUT/OUTPUT INSTRUCTION	IN A, n	A ← (n)	Set flags
	IN r, (C)	r ← (C)	
	INI	(HL) ← (C), HL ← HL + 1, B ← B − 1	
	INIR	(HL) ← (C), HL ← HL + 1, B ← B − 1 Repeat until B = 0	
	IND	(HL) ← (C), HL ← HL − 1, B ← B − 1	
	INDR	(HL) ← (C), HL ← HL − 1, B ← B − 1 Repeat until B = 0	
	OUT n, A	(n) ← A	
	OUT (C), r	(C) ← r	
	OUTI	(C) ← (HL), HL ← HL + 1, B ← B − 1	
	OTIR	(C) ← (HL), HL ← HL + 1, B ← B − 1 Repeat until B = 0	
	OUTD	(C) ← (HL), HL ← HL − 1, B ← B − 1	
	OTDR	(C) ← (HL), HL ← HL − 1, B ← B − 1 Repeat until B = 0	
JUMP INSTRUCTION	JP nn	PC ← nn	
	JP cc, nn	If condition cc is true PC ← nn, else continue	cc ≡ NZ, Z, NC, C, PO, PE, P, M
	JR e	PC ← PC + e	
	JR kk, e	If condition kk is ture PC ← PC + e, else continue	kk ≡ NZ, Z, NC, C
	JP (ss)	PC ← ss	ss ≡ HL, IX, IY
	DJNZ e	B ← B − 1, if B = 0 continue, else PC ← PC + e	
CALL INSTRUCTION	CALL nn	$(SP-1) \leftarrow PC_H$, $(SP-2) \leftarrow PC_L$, PC ← nn	
	CALL cc, nn	If condition cc is false continue, else same as CALL nn	cc ≡ NZ, Z, NC, C, PO, PE, P, M
	RST L	$(SP-1) \leftarrow PC_H$, $(SP-2) \leftarrow PC_L$, $PC_H \leftarrow 0$, $PC_L \leftarrow L$	
RETURN INSTRUCTION	RET	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP + 1)$	
	RET cc	If condition cc is false continue, else same as RET	cc ≡ NZ, Z, NC, C, PO, PE, P, M
	RETI	Return from interrupt, same as RET	
	RETN	Return from nonmaskable interrupt	

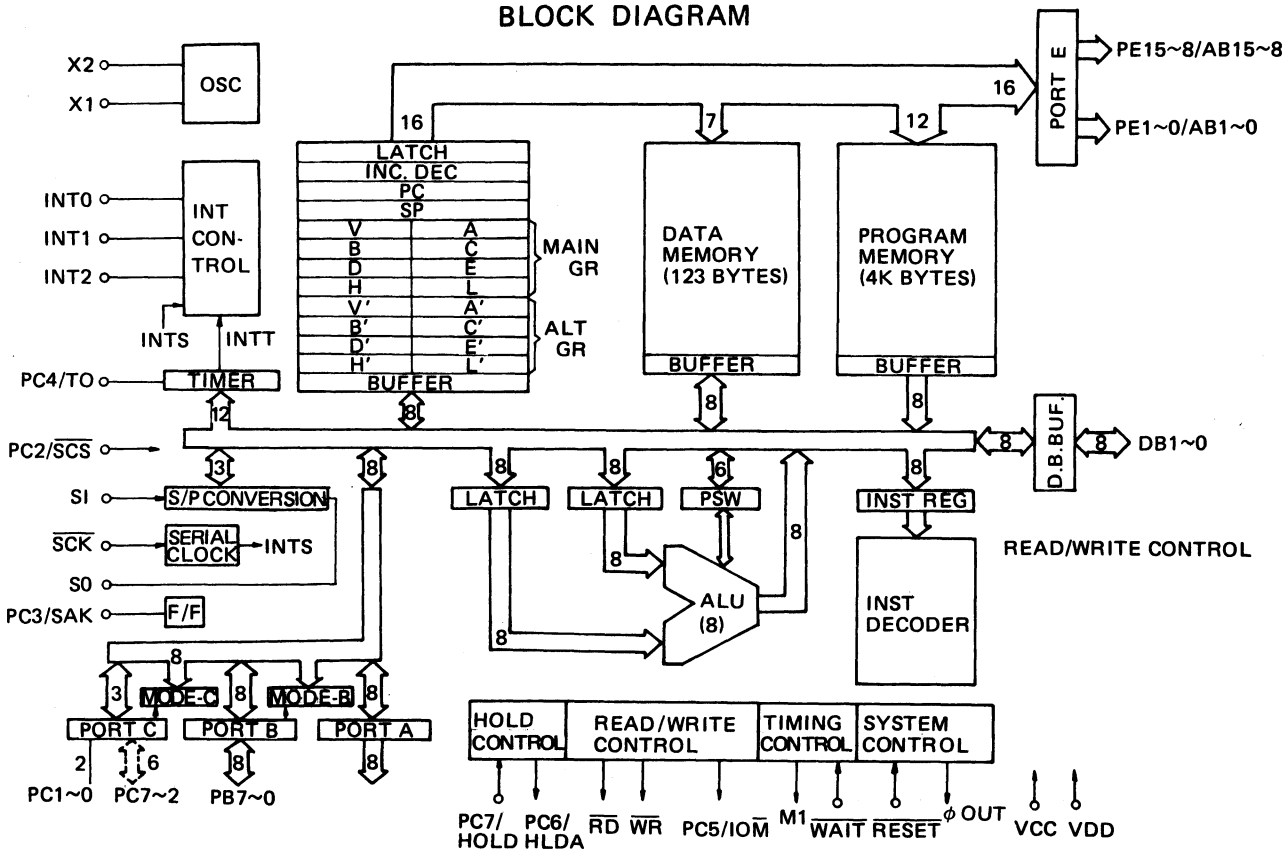
5-2. μPD7801G (SUB CPU)

PIN ASSIGNMENT



PA7 ~ PA0	:	Port A
PB7 ~ PB0	:	Port B
PC7 ~ PC0	:	Port C
$\overline{WR}$	:	Write strobe
$\overline{RD}$	:	Read strobe
SAK (PC3)	:	Serial acknowledge
SCS (PC2)	:	Serial chip select
TO (PC4)	:	Timer out
IO/$\overline{M}$ (PC5)	:	IO/Memory
HLDA (PC6)	:	Hold acknowledge
HOLD (PC7)	:	Hold request
DB7 ~ DB0	:	Data bus
PE15 ~ PE0	:	Port E
M1	:	Machine cycle 1
$\overline{WAIT}$	:	Wait request
INT0, INT1, INT2	:	Interrupt request
X1, X2	:	Crystal
φOUT	:	Clock out
$\overline{SCK}$	:	Serial clock
SI	:	Serial input
SO	:	Serial output
$\overline{RESET}$	:	Reset

BLOCK DIAGRAM



SIGNAL NAME	I/O	DESCRIPTION
PA7 ~ PA0	O	These gates are 8-bit output port and have latch function. Data is exchanged between the latches and the accumulator by the transfer command. Contents in the latch can be set flexibly by calculation operation or logic operation. Data set once in the latch is reserved until commands which operate Port A are executed or the reset condition occurs.
PB7 ~ PB0	I/O	These gates are 8-bit input and output ports and have latch function. The Port·B are to be set for input port or output port in a bit unit by the MODE·B register. They should become output high impedance at reset time if they are set as input port. (a) In case the ports are designated as output port (MODE·Bn=0): The output latches become valid and data flows between the output latches and the accumulator if the transfer command is executed. Also contents in the latches are set flexibly by calculation operation or logic operation command. Data which has been written in the output latches is reserved until commands which operate the Port·B next are executed or reset condition occurs. (b) In case the ports are designated as input port (MODE·Bn=1): Input latches become valid and contents which are input from external terminals and reserved in the input latches are loaded to the accumulator by the transfer command. In this case, it is possible to write data to the output latches and data transferred from the accumulator by the transfer command stored in the all output latches with no concern of the input/output designation of port. However, contents of the output latches of which bits are designated for the input ports cannot be loaded into the accumulator. Because the output buffers are high impedance, data in the output latches are not output to the external terminals. Thus, data reserved in the output latches are output to the external terminals when the bit is changed over to the output port and it can be loaded into the accumulator. Actual command execution is implemented by an 8-bit unit. In case command of Port B READ (MOV A, PB) is executed, input latch contents of port which is designated as input, and output latch contents of port which is designated as output are loaded into the accumulator. In case commands of Port B WRITE (MOV PB, A, etc.) are executed, although WRITE is executed into the output latches of both ports which are designated as input and output, contents in the output latch of port designated as input are not output to the external terminals.

<table>
<tr><th>SIGNAL NAME</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td>PC7 ~ PC0
(Port C)</td><td>I/O</td><td>These ports are a special 8-bit input and output port, and only PC0 and PC1 have 3-state function. 2 bits of PC0 and PC1 are general input and output ports and have each input and output latches. They have the same construction and function as Port·B. They become input high impedance in case they are programmed as input port and at reset time.
6 bits of PC2 ~ PC7 can function not only as input generally or as output port exclusively but also as various control signals. And the change-over is executed in a bit unit by designation of the MODE·C register. Refer to the following table for details.
<table>
<tr><th></th><th>MODE·CN=0</th><th>MODE·Cn=1</th></tr>
<tr><td>PC0</td><td>OUTPUT</td><td>INPUT</td></tr>
<tr><td>PC1</td><td>OUTPUT</td><td>INPUT</td></tr>
<tr><td>PC2</td><td>$\overline{\text{SCS}}$ INPUT</td><td>INPUT</td></tr>
<tr><td>PC3</td><td>SAK OUTPUT</td><td>OUTPUT</td></tr>
<tr><td>PC4</td><td>TO OUTPUT</td><td>OUTPUT</td></tr>
<tr><td>PC5</td><td>IO/$\overline{\text{M}}$ OUTPUT</td><td>OUTPUT</td></tr>
<tr><td>PC6</td><td>HLDA OUTPUT</td><td>OUTPUT</td></tr>
<tr><td>PC7</td><td>HOLD INPUT</td><td>INPUT</td></tr>
</table>
Contents of this port are set flexibly by calculation operation or logic operation or judge command, etc. By the transfer command, the port can exchange data with the accumulator.
In case they are chosen as control input and output, most of its function is determined by the hold control circuit and the serial port control circuit, not by commands.</td></tr>
<tr><td>$\overline{\text{WR}}$</td><td>O</td><td>This signal is a strobe signal which is output for WRITE operation of external memory or I/O mode. At external memory WRITE MACHINE CYCLE and the OUT command is executed, it becomes active (low) during the I/O WRITE MACHINE CYCLE only. Otherwise, it holds a high impedance condition. It becomes output high impedance at halt or hold or reset time.</td></tr>
<tr><td>$\overline{\text{RD}}$</td><td>O</td><td>This strobe signal is output for READ operation of external memory or I/O mode. Signal becomes active (low when external memory command is executed, IN command is executed at external memory read machine cycle and during I/O read machine cycle. Otherwise, signal becomes high impedance. It also becomes output high impedance at hat or hold or reset time.</td></tr>
<tr><td>SAK (PC3)</td><td></td><td>Multiprocessor system with serial input and output can be designed easily by utilizing this signal. It becomes low after completion of serial data transfer and it becomes high when it receives data from the serial register (S/P) or it sets transfer data to the serial register. It can be utilized as interrupt request signal to the main CPU.</td></tr>
</table>

SIGNAL NAME	I/O	DESCRIPTION
$\overline{SCS}$ (PC2)		Multiprocessor system with serial input and output can be designed easily by utilizing this signal. When signal at low is input, the $\overline{SCK}$ signal becomes valid and it causes serial data transfer through the SI and SO. When signal at high is input, output of the SO becomes high impedance and the $\overline{SCK}$ will be refused. In case the PC2 is programmed as general input (MC2=1), the SI, SO and $\overline{SCK}$ terminals are always valid.
TO (PC4)	O	This signal is set by the STM command and output of timer flip-flop which is reset by the borrow generated by countdown of the timer is output through this terminal.
IO/$\overline{M}$ (PC5)	O	Signal at low is output when it accesses memory, otherwise it holds high level itself. The signal is not necessary if memory is connected externally without connecting an I/O.
HLDA (PC6)	O	When the HOLD REQUEST is accepted, it becomes high and hold high level during the hold cycle, then it becomes low when the hold condition is released.
HOLD (PC7)	I	This terminal is for the hold request signal and it is checked every machine cycle. The CPU goes into the hold cycle (Th) without shifting to the next machine cycle if the signal is hgih. Then it causes the address bus (PE15-0), the data bus (DB7 ~ 0), the $\overline{RD}$ and the $\overline{WR}$ to become high impedance. The HLDA signal becomes high at this time. The hold condition continues as long as the HOLD signal is high. HLDA signal becomes low when the signal becomes low and various buses and control signals will be released, then the CPU shifts to the next machine cycle.
DB7 ~ DB0	I/O	These terminals are an 8-bit bidirectional bus which is used when data is exchanged between external memory and the accumulator or I/O and the accumulator. It becomes output high impedance at the input mode or halt or hold or reset period.
PE15 ~ PE0	O	These terminals are a 16-bit output/input port and can be programmed as address bus also. It can be programmed in the following three ways. (a) 16-bit address bus: In case up to 60Kbytes memory is connected externally, these terminals are programmed as a 16-bit address bus. This is possible by the PER command or the RESET signal. When external memory reference command is executed, the reference address is output through the terminals only during the external memory reference machine cycle of the command cycle. Otherwise, all bits from PE15 to PE0 are high impedance. In this mode, all bits become high impedance when halt or hold or reset condition occurs.

SIGNAL NAME	I/O	DESCRIPTION
		(b) 4 bits for output port and 12 bits for address bus: In case up to 4Kbytes memory is to be connected, address buses from PE11 ~ PE0 are used as address bus and PE15 ~ PE12 are used as outputs of higher 4 bits (B7 ~ B4) of the B register. When the external memory reference command is executed, lower 12 bits from PE11 ~ PE0 of reference address are output only during the external memory reference machine cycle of the command cycle. Otherwise, 12 bits from PE11 ~ PE0 are high impedance. Because higher 4 bits of the reference are neglected, 4 bits can be programmed as an external memory address. In this mode, lower 12 bits from PE11 to PE0 of the Port E become high impedance at halt or hold period. However, the higher 4 bits from PE15 to PE12 are not affected. (c) 16-bit output port: If connected to no memory externally, the terminals are programmed as 16-bit general output port. Contents of the B register are output through the higher 8 bits from PE15 to PE8 and contents of the C register are output through the lower 8 bits from PE7 to PE0 respectively by the PEX command. This mode is programmed automatically when the PEX command is executed. Note: The PEN command should not be executed if the PEX condition has been programmed previously. When the need occurs, first execute the PER instruction, then the PEN instruction follows.
M1	O	This is an output signal to inform first machine cycle of each command to the outside. High level from T1 to T3 of the 10th code fetch cycle are output. It is also used as a one step operation or break operation of a command.
$\overline{WAIT}$	I	If access time of an externally connected memory is slow, read/write timing can be extended by inputting a low level signal into this terminal. $\overline{WAIT}$ signal is checked at the end of T2. The CPU will get into wait state (Tw) if it is low and Tw will be repeated until the $\overline{WAIT}$ signal becomes high.
INT0, INT1, INT2	I	INT0 is set as level interrupt. INT1 is set as rising edge interrupt, and INT2 is set as rising/falling edge interrupt respectively by the interrupt request input. The priority order is as follows. INTT and INTS are internal interrupt. INT0 > INTT > INT1 > INT2 > INTS (a) INT0: This is a high level active signal of the level interrupt input.

SIGNAL NAME	I/O	DESCRIPTION
		(b) INT1: This is a rising edge interrupt signal and becomes active when the INT1 input varies from low to high. Therefore, after the interrupt was once accepted, it is necessary to set the INT1 high from the low period in order for the next interrupt to be accepted. (c) INT2: This is an interrupt input which can cause the rising edge or falling edge to be valid and selection (rising edge or falling edge) depends upon the ES bit of the MASK register. The register content is reset or set by command and the rising edge interrupt is set if the ES bit is 1 or the falling edge is set if the ES bit is 0. Because the 3 interrupt inputs are sampled by 2 microseconds cycle internal clock to prevent mis-operation caused by noise, and if the cycle is less than 2 microseconds the noise will be removed from the interrupt input. Therefore, the interrupt input requires more than 4 microseconds of active period of the interrupt request signal.
X2, X1	—	Two terminals are for the crystal connecting terminals. External clock can be input from the X1 terminal.
ϕ OUT	O	This terminal outputs demultiplied oscillation of the crystal (1/2). It is used to synchronize external devices as the necessity arises.
$\overline{SCK}$	I/O	This clock controls serial input and output. It outputs contents of the serial register (S/P) with the MSB in forefront to the SO terminal at the falling edge of the $\overline{SCK}$ signal, and it loads data on the SI terminal into the serial register at the rising edge of the $\overline{SCK}$ signal.
SI	I	This terminal is for serial input port and it outputs data in the serial register to the SO terminal at the falling edge of the $\overline{SCK}$ signal. The forefront will be the MSB.
$\overline{RESET}$	I	When more than 4 microseconds of low level signal is input into this terminal, the system reset occurs and it creates the following conditions. • Reset interrupt admission flag and cause interrupt prohibit condition. • Reset interrupt request flag and terminate reservation interrupt. • Set all mask bits of the interrupt mask register. All interrupts become mask condition. The ES bit is reset and the INT2 becomes falling edge mode. • Reset the HALT flip-flop and release the halt condition. • Set contents of the register MODE·B and all Port Bs become input mode (output high impedance).

SIGNAL NAME	I/O	DESCRIPTION
		• Set contents of MODE·C register in FF (16), then the PC0 and PC1 become input mode (output high impedance), the PC2 ~ PC7 become input or output port mode and the low level signal is output to the output port. • All Port A outputs become low level. • Reset (0) all flags. • Set the COUNT register of the timer in FFF (16) and reset the timer flip-flop. • Set the SAK flip-flop. • Reset the HLDA flip-flop. • Reset contents of the PC in 0000 (16). • Cause the address bus (PE15 ~ PE0), the data bus (DB7 ~ DB0), $\overline{RD}$ and $\overline{WR}$ signals to become high impedance. To prevent mis-operation caused by noise, the $\overline{RESET}$ input does not accept level variation if it is less than a 2 microseconds cycle. When the $\overline{RESET}$ input becomes high, start program from 0000 (16) address.
SO	O	This terminal is for serial output port and it outputs data in the serial register to the SO terminal at the falling edge of the $\overline{SCK}$ signal. The forefront will be the MSB.

THE REGISTERS IN μPD7801G

The following figure shows the configuration of the registers in μPD7801G sub CPU.
It consists of 16 8-bit registers and 2 16-bit registers.

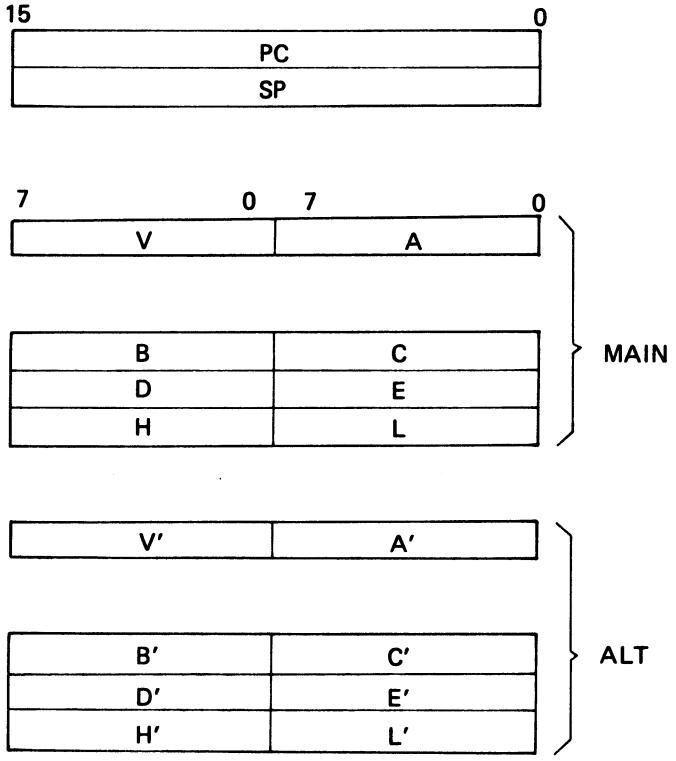


Fig. 5-7 REGISTER CONFIGURATION

1) General registers (B, C, D, E, H, L):
There are 2 sets (MAIN: B, C, D, E, H, L ALT: B', C', D', E', H', L') of general registers in this sub CPU.
Its functions are not only as supplement register to the accumulator but also data pointer as pair register (BC, DE, HL; B'C', D'E', H'L').
By using 2 sets of the registers, the contents of the register at the right before interruption need not be saved in memory and it can be saved in one of the other registers, instead so that the interrupt service can be executed. Also the other register can be utilized as an expand register.
There is an addressing mode of auto increment/decrement for the pair registers of DE, HL, D'E' and H'L' and it shortens the access time. Pair registers of BC, DE and HL can be exchanged with the ALT registers simultaneously by the EXX instruction.

2) Working register · Vector register (V):
When program working area is in the memory, the higher 8 bits of the memory are selected by this V register and the lower 8 bits are addressed by immediate data of the command. In this way, the memory area designated by the V register can be utilized as a working register of 256W x 8 configuration.
To designate the working register, one byte of address field is used and it can save the program when it is used as a work area for flag or parameter or counter of software.
The vector register is exchanged with the ALT register pairing with the accumulator.

3) Accumulator (A) :
All data processes are executed with the accumulator as the principal.
The accumulator register is exchanged with the ALT register pairing with the vector register (V).

4) Program counter (PC) :
This is a 16-bit register and it saves address information of the next program to be executed. Generally, it is automatically incremented in accordance with the byte number of command to fetch, but when executing command with branch steps, immediate data or contents of register is loaded into this register. 0000 (16) is set in the register when the reset occurs.

5) Stack pointer (SP) :
This is a 16-bit register and it saves the forefront address information of the memory stack area (LIFO) method.
Contents in the register decrement when CALL or PUSH instruction is executed or an interrupt occurs, and it increments when RETURN or POP instruction is executed.

Arithmetic Logic Unit (ALU) . . . 8 bits

This unit processes various operations such as binary addition/subtraction, decimal correction, logic operation, operation process such as comparison, shift, rotation and digit rotation.

Memory Inside The μPD7801G

This chip is able to address up to 64 Kbytes of memory. If the ROM area (0-4095th) is removed in the chip, there is no distinction between the program area and the data memory area, and both can be treated as the same. It can make powerful addressing possible.
There are reset start addresses, interrupt start addresses and call tables in the internal ROM area.
External memory area and internal RAM area are utilized freely as data memory or program memory or working register.
Access timing for internal and external memories is set the same which causes high speed process.

1) Interrupt start address:

   INT0 . . . 4th address
   INTT . . . 8th address
   INT1 . . . 16th address
   INT2 . . . 32th address
   INTS . . . 64th address

   It is necessary to set pre-process of interrupt service program properly because interval between interrupt addresses is not equal.

2) Call address table:
   Call address of one byte call instruction (CALT) is stored in 64 call addresses in the 128 bytes area from the address 128th to 255th.

3) Built-in program memory area:
   There is a built-in mask programmable ROM at address 0 ~ 4095th in this chip.
   Reset address, interrupt address and call table should be considered when programming address 2048 ~ 4095th is addressed directly by 2-byte call instruction (CALF).

4) Built-in data memory area:
   In address 65408 ~ 65535th, 128 bytes of RAM is set (built-in).

5) External expand memory area:
   Externally, up to 60 Kbytes (address 4096 to 65407th) of data memory of program memory are expandable by using address bus (PE15 ~ PE0) and data bus (DB7 ~ DB0).

6) Working register area:
   256 bytes of working register can be programmed freely in the memory (with V register designation).

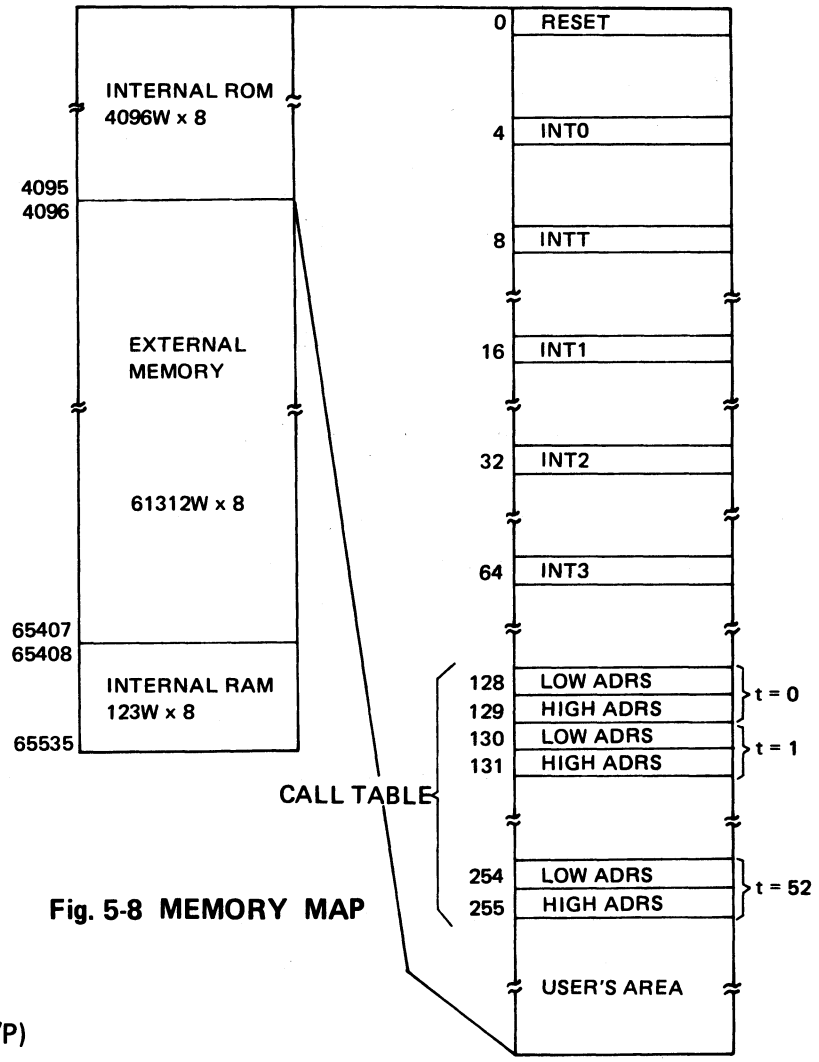


Fig. 5-8 MEMORY MAP

Serial register (S/P)

This is an 8-bit register. Serial clock becomes valid when the $\overline{SCS}$ input is low and data input from the serial input (SI) and data output from the serial output (SO) are possible. When 8 pulses of the serial clock is generated (end of 8-bit data transmission/reception), carry (T8; INTS) generated in octal counter causes internal interrupt to generate and acknowledge output (SAK) to become low. MOV S, A instruction causes 8-bit data to be set in the serial register and MOV A, S instruction causes serial instruction contents to be read. At that time the SAK signal becomes high.
The octal counter is cleared and internal clock is triggered by the SIO instruction. Then transmission and reception begin.

Timer

This is a programmable 12-bit interval timer. It consists of TIMER·REG0 (8 bits), TIMER·REG 1 (4 bits), PRESCALER and 12-bit counter.
Its count ranges from 4 microseconds to 16 milliseconds.
First of all, program count value at the TIMER·REG (MOV TM0, A; MOV TM1, A) and TIMER REG content at down counter. After the program is completed, it starts counting time. It counts down every 4 microseconds and generates interval interrupt (INTT) when borrow is generated. Simultaneously TIMER·REG content is set at down count again and it starts counting down.

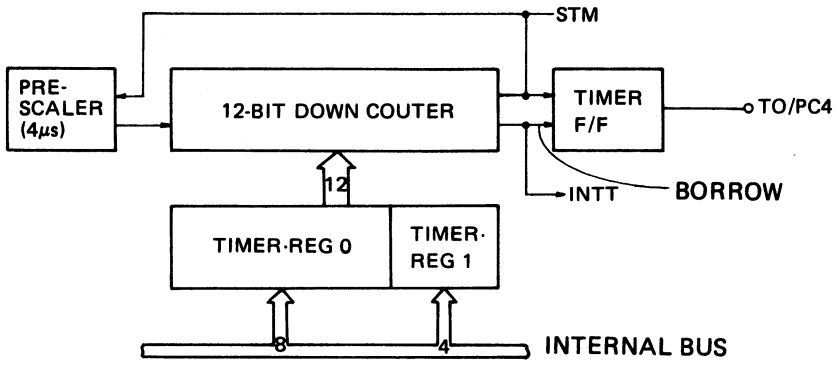


Fig. 5-9 TIMER BLOCK DIAGRAM

Accordingly, interrupt is repeatedly generated in interval of time programmed at the TIMER·REG. TIMER flip-flop is set by STA instruction and reset by borrow on down counter. It is output to TO (PC4) if MC4=0 and utilized for various external controls.

Mode · B

This register is an 8-bit register and designates input/output mode of Port B. It also sets contents of the accumulator (MOV MB, A) and determines data.
Input/output designation is programmed in a bit unit base.

MBn = 0 : PBn = OUTPUT MODE
MBn = 1 : PBn = INPUT MODE (n = 0 ~ 7)

Mode · C

This register is an 8-bit register and designates input/output mode of Port C.
It also sets content of the accumulator (MOV MC, A) and determines data. Mode designation is programmed in a bit unit base. It designates external clock or internal clock to be used as serial clock.

	MCn=0	MCn=1
n=0	PC0: OUTPUT	PC0: INPUT
1	PC1: OUTPUT	PC1: INPUT
2	PC2: $\overline{SCS}$ INPUT	PC2: INPUT
3	PC3: SAK OUTPUT	PC3: OUTPUT
4	PC4: TO OUTPUT	PC4: OUTPUT
5	PC5: IO/$\overline{M}$ OUTPUT	PC5: OUTPUT
6	PC6: HLDA OUTPUT; PC7: HOLD INPUT	PC6: OUTPUT; PC7: INPUT
7	INTERNAL CLOCK	EXTERNAL CLOCK

Program status word (PSW)

The word consists of 6 different kinds of flags to be set or reset by the result of instruction execution. Two kinds of flags among the rest are instruction and they can be checked. Content of the PSW is saved automatically in the stack when interrupt is generated (external, internal, SOFT 1 instruction) and it is resumed by RETI instruction.
$\overline{\text{RESET}}$ input set all to 0.

D7	D6	D5	D4	D3	D2	D1	D0	
	Z	SK	HC	L1	L0		CY	PSW

1) Z (zero):
Z is set on 1 when the result of operation is zero and it is set on 0 when the result of operation is other than 0. It can be checked by instruction.

2) SK (skip):
SK is set on 1 when the skip condition is met and it is set on 0 if it is not.

3) HC (half carry):
In result of operation, HC is set on 1 when carry is brought about from bit 3. Otherwise it is set on 0.

4) L1:
When stack in length by the stack instruction MVI A, byte is brought about, it is set on 0. Otherwise it is reset to 0.

5) L0:
When the stack by MVI L, byte; LXI H, word instructions are brought about, it is set on 1. Otherwise it is reset to 0.

6) CY (carry) :
In operation result, it is set on 1 when carry from bit 7 is brought about and it is reset to 0 otherwise. It can be checked by instruction.

7) Affection by Flags:
Various flags in the following table are affected by the execution of 18 ALU instructions, shift, rotation and carry instructions. The results are as follows.

Operation						D6	D5	D4	D3	D2	D0
reg. memory			immediate		skip	Z	SK	HC	L1	L0	CY
ADD ADC SUB SBB	ADDW ADCW SUBW SBBW	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			↕	0	↕	0	0	↕
ANA ORA XRA	ANAW ORAW XRAW	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		↕	0	●	0	0	●
ADDNC SUBNB GTA LTA	ADDNCW SUBNBW GTAW LTAW	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	 GTIW LTIW		↕	↕	↕	0	0	↕
ONA OFFA	ONAW OFFAW	ONAX OFFAX	ONI OFFI	ONIW OFFIW		↕	↕	●	0	0	●
NEA EQA	NEAW EQAW	NEAX EQAX	NEI EQI	NEIW EQIW		↕	↕	↕	0	0	↕
INR DCR	INRW DCRW					↕	↕	↕	0	0	●
DAA						↕	0	↕	0	0	↕
RLL, RLR SLL, SLR						●	0	●	0	0	↕
RLD, RRD						●	0	●	0	0	●
STC						●	0	●	0	0	1
CLC						●	0	●	0	0	0
			MVI A, byte			●	0	●	1	0	●
			MVI L, byte LXI H, word			●	0	●	0	1	●
					BIT SK SKN SKIT SKNIT	●	↕	●	0	0	●
					RETS	●	1	●	0	0	●
All other instructions						●	0	●	0	0	●

↕: affected
1: set
0: reset
●: not affected

Interrupt control block

There are 3 external interrupts and 2 internal interrupts. Both interrupts are vectored interrupt.

	INTERRUPT TYPE	INTERRUPT ADDRESS	PRIORITY
EXTERNAL	INT0 (LEVEL)	4	1
	INT1 (RISING EDGE)	16	3
	INT2 (RISING/FALLING EDGE)	32	4
INTERNAL	INTT (TIMER OVERFLOW)	8	2
	INTS (SERIAL BUFFER FULL/EMPTY)	64	5

The block consists of INTERRUPT REQUEST register, MASK register, PRIORITY CONTROL, TEST CONTROL and INTERRUPT ENABLE flip-flop.

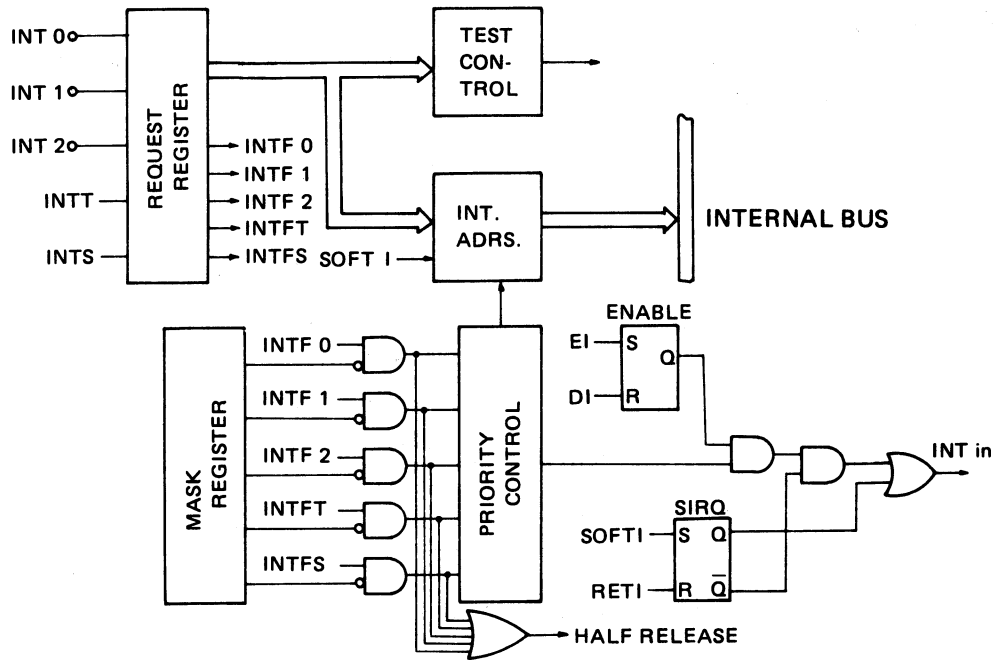


Fig. 5-10 INTERRUPT CONTROL BLOCK

1) INTERRUPT REQUEST register:
This register consists of 5 different kinds of interrupt request flags which is set against each interrupt. All flags are reset at time of system reset.

INTF0 – This is the flag which is set by level interrupt (INT0) from external and it is set on 1 when high level is input into INT0 input. It is reset when low level is input.

INTF1 – This flag is set on 1 by rising edge input into INT1 input.

INTF2 – This flag is set on 1 by rising edge or falling edge input into INT2 input. The rising edge or falling edge is determined by bit 5 of MASK register. (ES: Edge Select). ES=1: RISING EDGE ES=0: FALLING EDGE

INTFT – This flag is set when overflow in the TIMER occurs.

INTFS – This flag is set when the serial register ends reception of 8 bits data through SI terminal or transmission through SO terminal.

2) MASK register:

This register has a 5-bit mask flag for each interrupt and it is set and reset by instruction. It is also masked by MASK bit 1.

BIT NO.	BIT CONTENT
0	MASK INTO
1	MASK INTT
2	MASK INT1
3	MASK INT2
4	MASK INTS
5	ES
6	–
7	–

Furthermore, ES bit is able to determine rising edge and falling edge of INT2 input.

3) PRIORITY CONTROL circuit:

This circuit controls the former stated priority order. The circuit will accept interrupt with higher priority when more than two interrupts occur simultaneously.

INTO > INTT > INT1 > INT2 > INTS

4) TEST CONTROL circuit:

This circuit is used when instruction, which checks interrupt request flag, is implemented.

5) INTERRUPT ENABLE flip-flop:

This flip-flop is set by EI instruction and reset by DI instruction. Once it accepts one of the two instructions, it is reset. Interrupt is admitted if the flip-flop is set and the interrupt is prohibited if it is reset.

It is reset by the system reset.

6) SIRQ flip-flop:

This flip-flop is set by SOFTI instruction and prohibits all other interrupts (INTF0 ~ 2, INTFT and INTFS) no matter what the EI/DI condition may be, and it requests interrupt by SOFTI instruction. It is reset by RETI instruction and releases the prohibit condition.

Interrupt operation

When interrupt is accepted, the following operation are implemented.

1) It resets the ENABLE flip-flop and causes prohibition condition.
2) It saves contents in the PSW and the PC into the stack register.
3) It generates interrupt start address, then jumps over to interrupt start address.
   At the same time, it resets interrupt request flag which has generated the interrupt.

INTERRUPT	START ADDRESS
INT0	4th ADDRESS
INTT	8th ADDRESS
INT1	16th ADDRESS
INT2	32nd ADDRESS
INTS	64th ADDRESS

Interrupt by SOFTI instruction

This is a instruction which generates internal interrupt in program and it causes contents in flag (PSW) and the PC to be saved into the stack when it is executed. Then it branches to the 96th address. It can be utilized effectively to monitor program and debugging.
Interrupt by SOFTI instruction is different from other interrupts and generated no matter what EI and DI conditions may be. If SOFTI instruction is executed, the other 5 interrupts are on hold until RETI instruction is newly executed.

MVI instruction

As the following 3 instructions are stacked in length, it executes the instruction once at the first. After that, it consumes numbers of the clock necessary for executing the instruction originally without performing (the same condition as NOP). However, the stack in length only among group A or group B produces the efficiency.

```
GROUP A :   MVI A, byte                      (L1 FLAG)
GROUP B :   MVI L, byte ; LXI H, word        (L0 FLAG)
```

If the stack by group A instruction occurs, L1 flag is set. L0 flag is set by group B. Interrupt is not prohibited during execution of the stack instruction because L flag is saved by interrupt but it can judge if next instruction is the instruction which produces the efficiency of the stack in length when it returns from interrupt.

```
START →      MVI   A, 0      ;  A ← 0
             MVI   A, 1      ;  NOP (7 CLOCKS),    L1=1
             MVI   A, 2      ;  NOP (7 CLOCKS),    L1=1
             MVI   L, OAH    ;  L ← OAH
             MVI   L, OBH    ;  NOP (7 CLOCKS),    L0=1
INTERRUPT →  MVI   L, OCH    ;  NOP (7 CLOCKS),    L0=1
             LXI   H, OOH    ;  NOP (10 CLOCKS),   L0=1
```

6. DISASSEMBLING / ASSEMBLING

6-1. SYSTEM UNIT

1) Turn off the power switch and unplug the power cord.
2) Place the system unit up-side-down on the work bench as shown in Fig. 6-1.
3) Remove 10 screws holding the upper and the bottom housings together.
4) Turn it over slowly and replace on the bench.
5) Slide the upper housing toward the front as shown in Fig. 6-2.
   You may have to hold the bottom housing with your the other hand.
6) Unplug 3 frame ground wires on top of the main P.C.B.
7) Remove 4 screws holding the main P.C.B.-mounting frame.
   Now, the main P.C.B.-mounting frame with the main P.C.B. can be separated.
8) To separate the main P.C.B. from the frame, unplug main-sub P.C.B. flexible connector, remove 4 screws holding two connectors on the frame and pinch in the 3 plastic snap-in holders from side to the P.C.B. side.

Be careful not to damage the flexible joiner.

9) To remove the sub P.C.B., remove I/O package compartment box by removing 4 screws first. Then unplug 2 frame ground wires and remove 12 screws on the sub P.C.B., keyboard connector and power connector respectively.

When you lift up the sub P.C.B., do it slowly and do not bend or hook any component on the P.C.B. with the bottom housing.

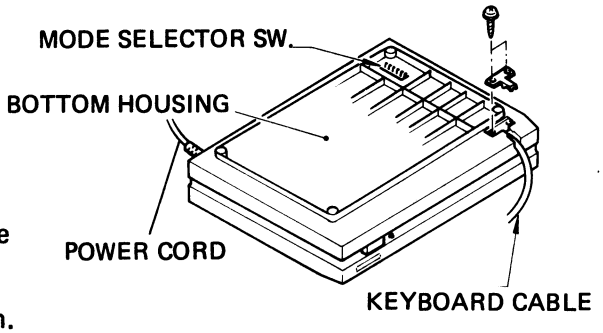


Fig. 6-1

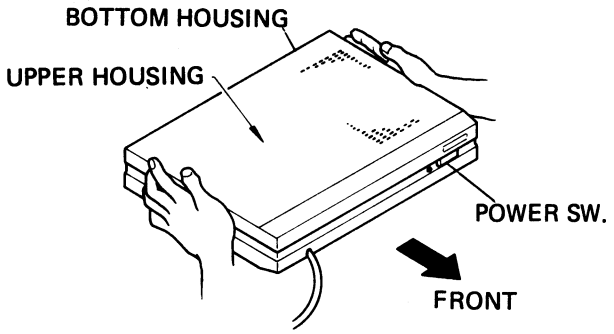


Fig. 6-2

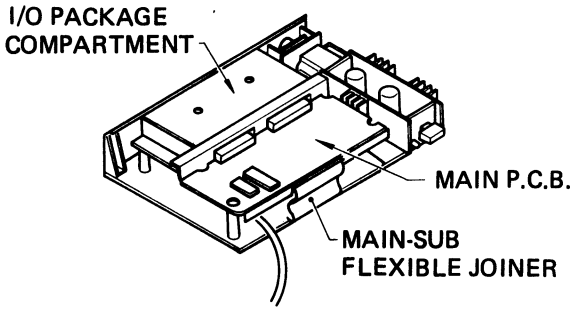


Fig. 6-3

10) To assemble, perform the above steps in reversed (from 9 to 1).

> Be careful not to bend the power-on L.E.D. when you replace the upper housing.

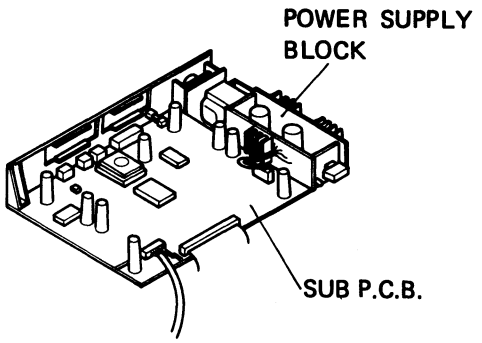


Fig. 6-4

6-2. KEYBOARD

1) Replace the keyboard unit up-side-down on the work bench as shown in Fig. 6-5.
2) Remove 6 screws holding the upper and bottom housings together.
3) To remove the key top, first remove the upper housing from the keyboard frame by removing 6 screws holding the black colored keyboard frame.
4) Pull up key top using your hand or key top remover as shown in Fig. 6-6.

> Be careful not to lose the spring when doing the above.

5) To work on pattern side of the keyboard P.C.B., remove 29 small screws, then open the P.C.B. slowly.

> Two L.E.D. located on the pattern side may be easily bent if you do not lift it up carefully.

6) To remove the key contact on key shaft, remove the key top first and relocate the key top shaft to the outside of the key shaft groove for easiness.
7) To assemble, perform the above steps in reverse (from 6 to 1).

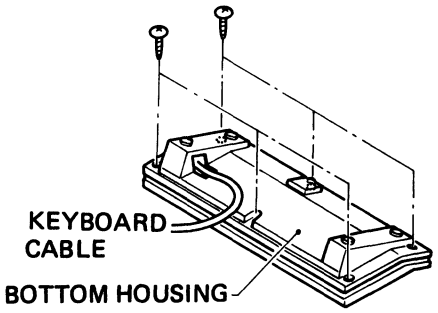


Fig. 6-5

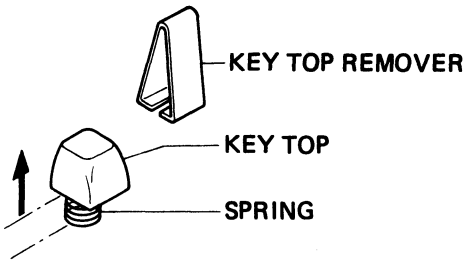


Fig. 6-6

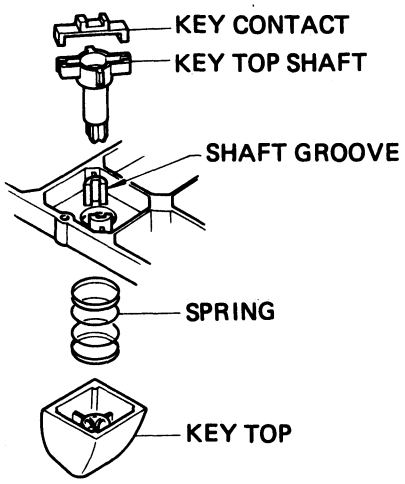


Fig. 6-7

7. COMPONENT AND CHECK PIN LOCATION MAP

7-1. MAIN P.C.B.

Note: 1) Number above each IC corresponds to the IC position number in the circuit diagram.

2) ○ marked in the following layout diagram shows test terminal.

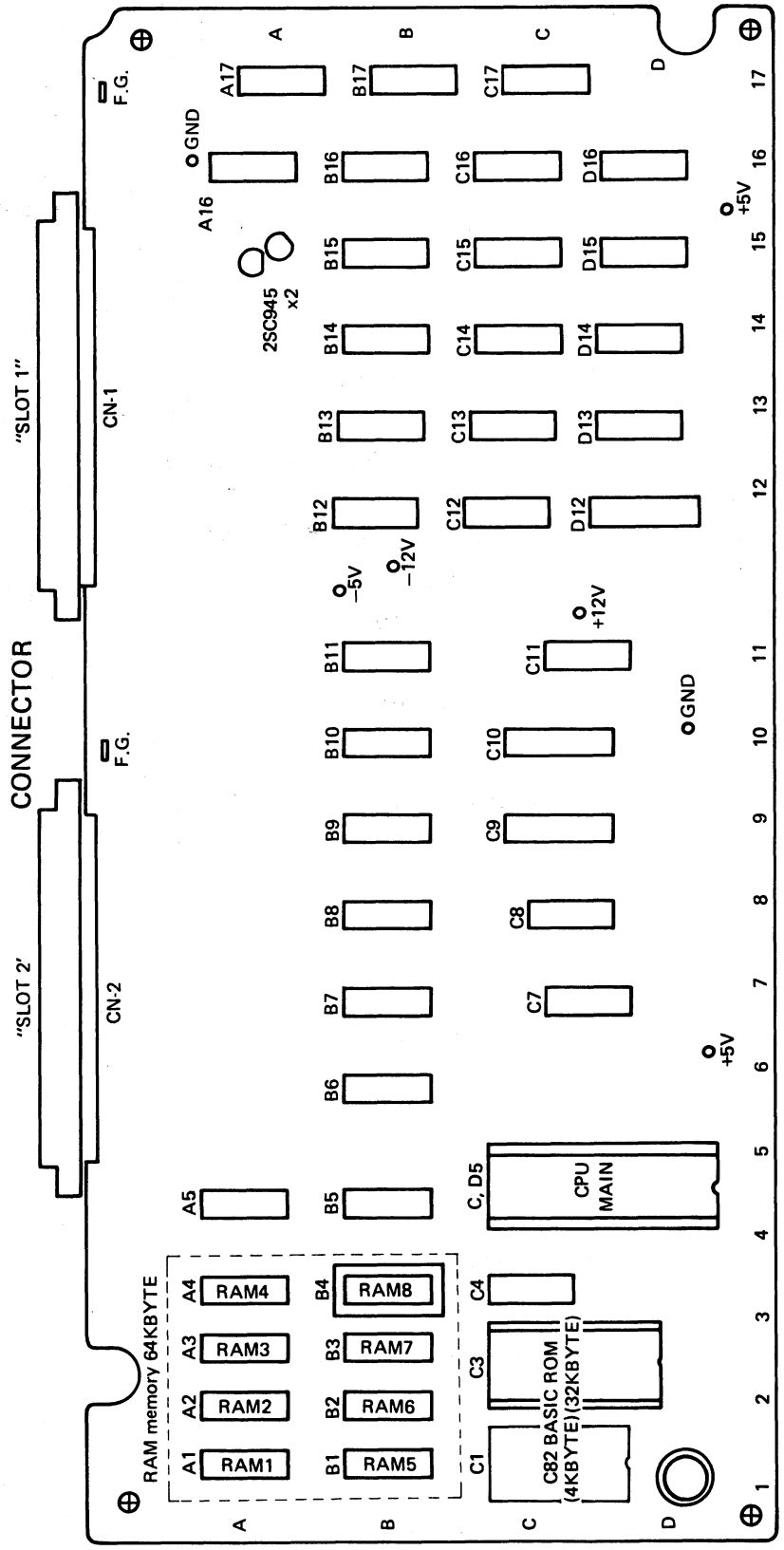


Fig. 7-1 IC LAYOUT ON THE MAIN P.C.B.

7-2. SUB P.C.B.

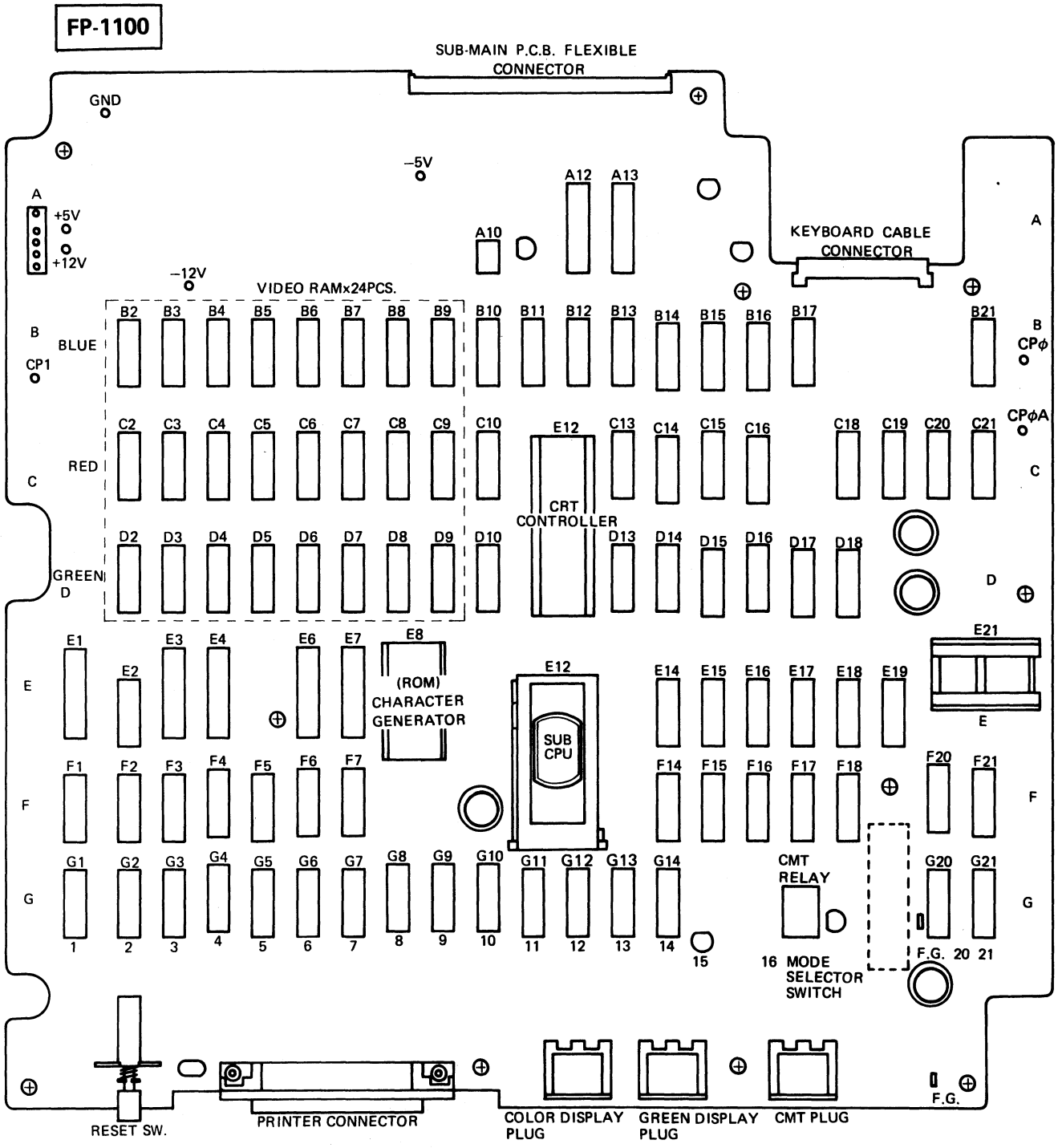


Fig. 7-2 IC LAYOUT ON THE SUB P.C.B.

8. CIRCUIT EXPLANATION

8-1. MEMORY TRANSFER

The system unit has 64KB RAM (dynamic type) for the system memory and the BASIC interpreter. As power is turned on, the block transfer which transfers the BASIC written in the ROM memory (PAGE 0) to the RAM (PAGE 1) for the BASIC language mode is executed automatically. 36KB of memory area is allocated for the BASIC in the RAM and 28KB of memory area is available for the user.

The ROM is isolated from the memory area later on and the transfer will not be executed again unless the hardware reset conditions occur such as turning on and off the power or the reset switch.

This is due to slower access time in the ROM than the access time in the CPU (4MHz). During the transfer access, read is designated for the ROM and write is designated for the RAM by the CPU respectively.

This operation is called the page change-over. After the transfer is completed, the CPU designates the RAM read and write.

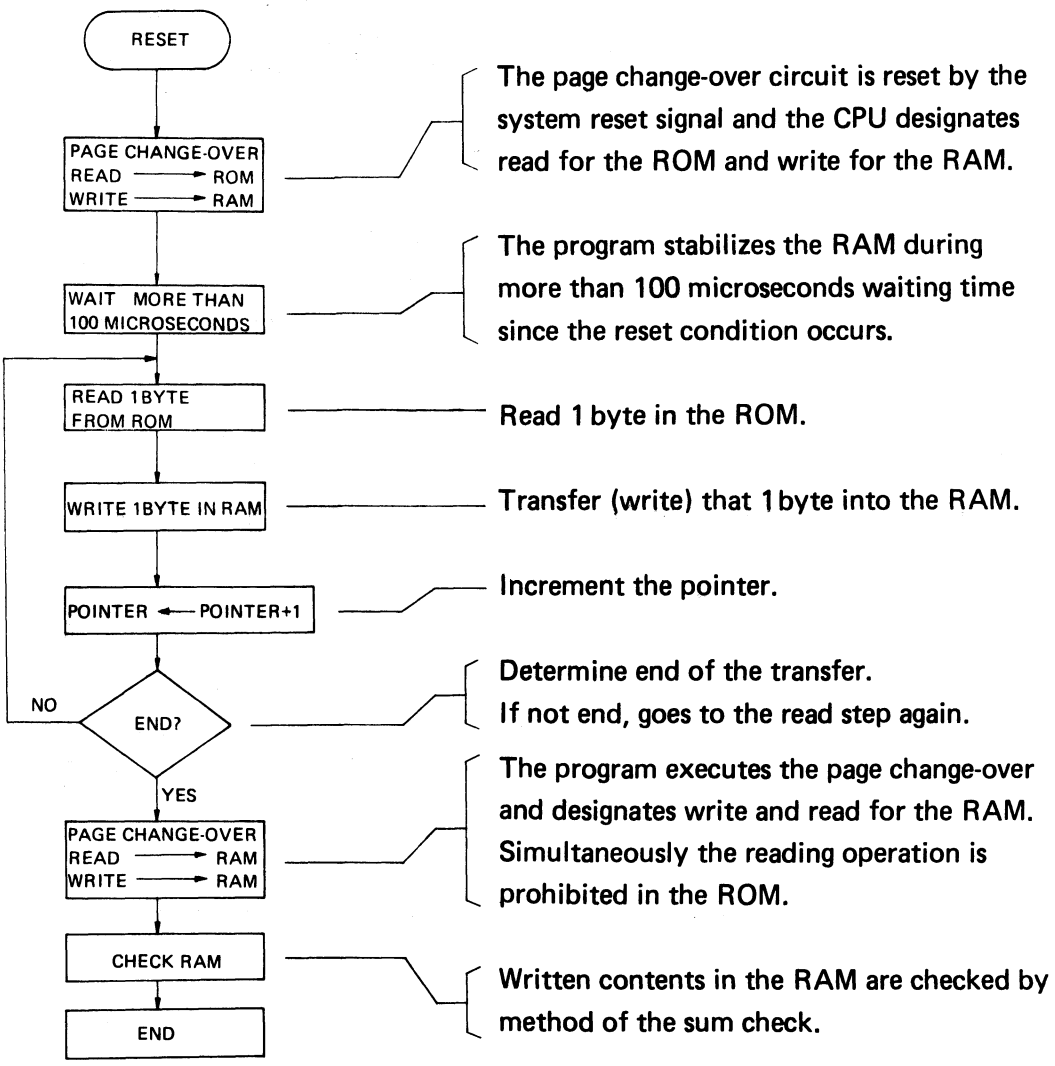


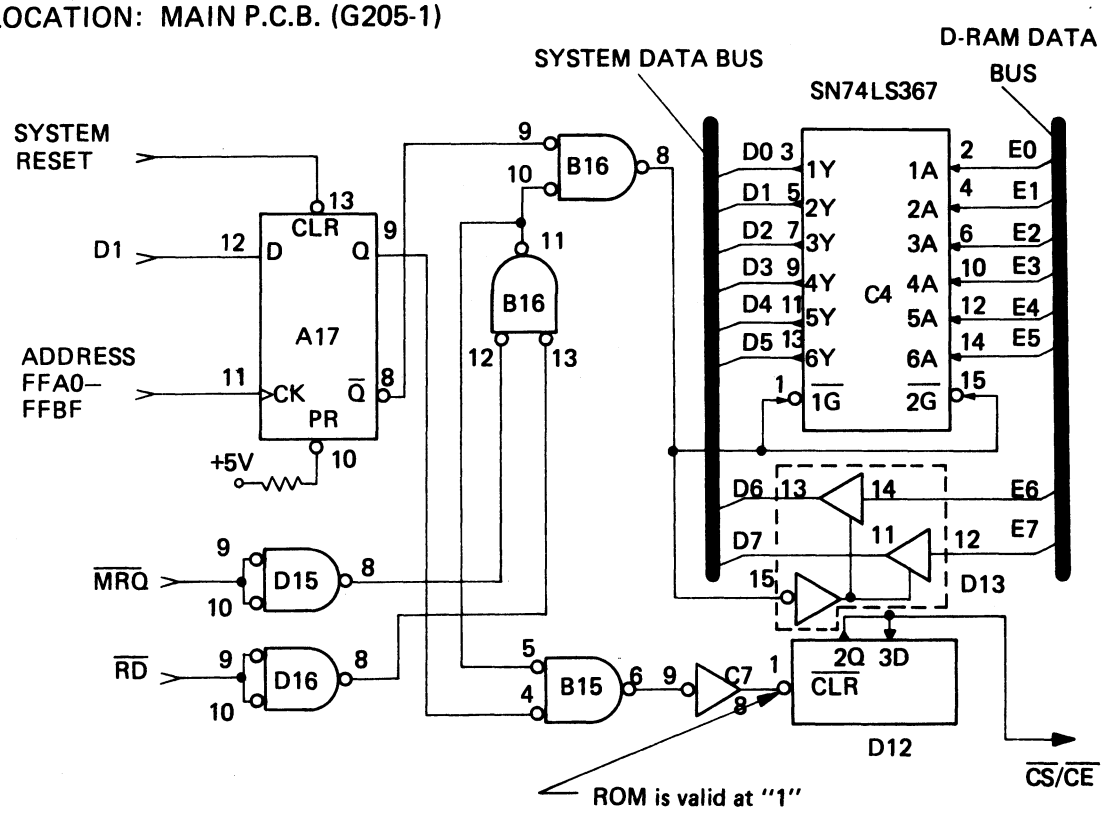
Fig. 8-1 TRANSFER FLOW CHART

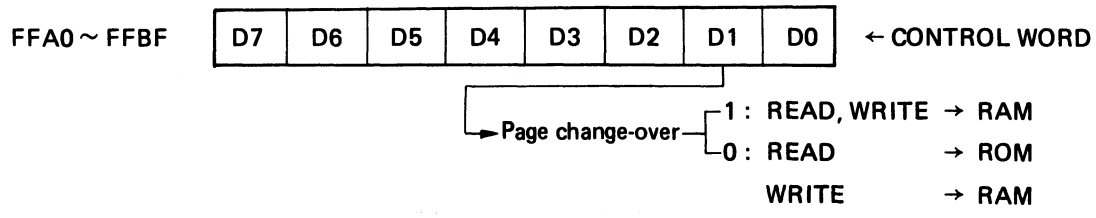
Sum check: Refers to a specific check developed when groups of digits are summed, usually without regard for overflow. Tht sum is checked against a previously computed sum to verify that no digits have been changed since the last summation.

8-2. MEMORY TRANSFER CIRCUIT:

Bank change-over is completed by writing "1" or "0" in D1 bit of the control word in I/O address space FFAOH~FFBFH. As the system is reset, such as power switch is turned on or the reset switch is pushed, flip-flop 17A in the circuit diagram is reset by the system reset, it designates the ROM for read and the RAM for write respectively.
While the flip-flop is in such condition, the C82-BASIC in the ROMs is transferred at once into RAMs. After the transfer is completed, "02" in hexadecimal will be written in the control word and the flip-flop will be set.
At this time, the ROMs are disconnected from the system flow. On the contrary, the RAMs become valid for reading and writing.

LOCATION: MAIN P.C.B. (G205-1)





8-3. WAIT CIRCUIT:

As, we have already explained, the ROMs contain the C82-BASIC long access time, a signal causes the CPU to be in wait condition which is necessary to accomplish the data transfer. The signal is known as the WAIT signal and is input into the CPU from the WAIT terminal. This condition is required each time one byte data is transferred from the ROMs into the memory.

When the active $\overline{\text{WAIT}}$ signal (active low) is input from the terminal at the falling edge of T2 state, other word is active at the falling edge of the state, Tw states are inserted between T2 and T3 states. At last Tw state, the state samples the wait condition and the condition is released if the $\overline{\text{WAIT}}$ signal is inactive at that time.

Then, one byte of data (D0 ~ D7) will be written into the memory at the falling edge of T3 state. The time required for the CPU to read-in the one byte of data is about 500 nanoseconds, but for the ROM to complete the transfer the BASIC is about 300 ~ 400 milliseconds.

LOCATION: MAIN P.C.B. (G205-1)

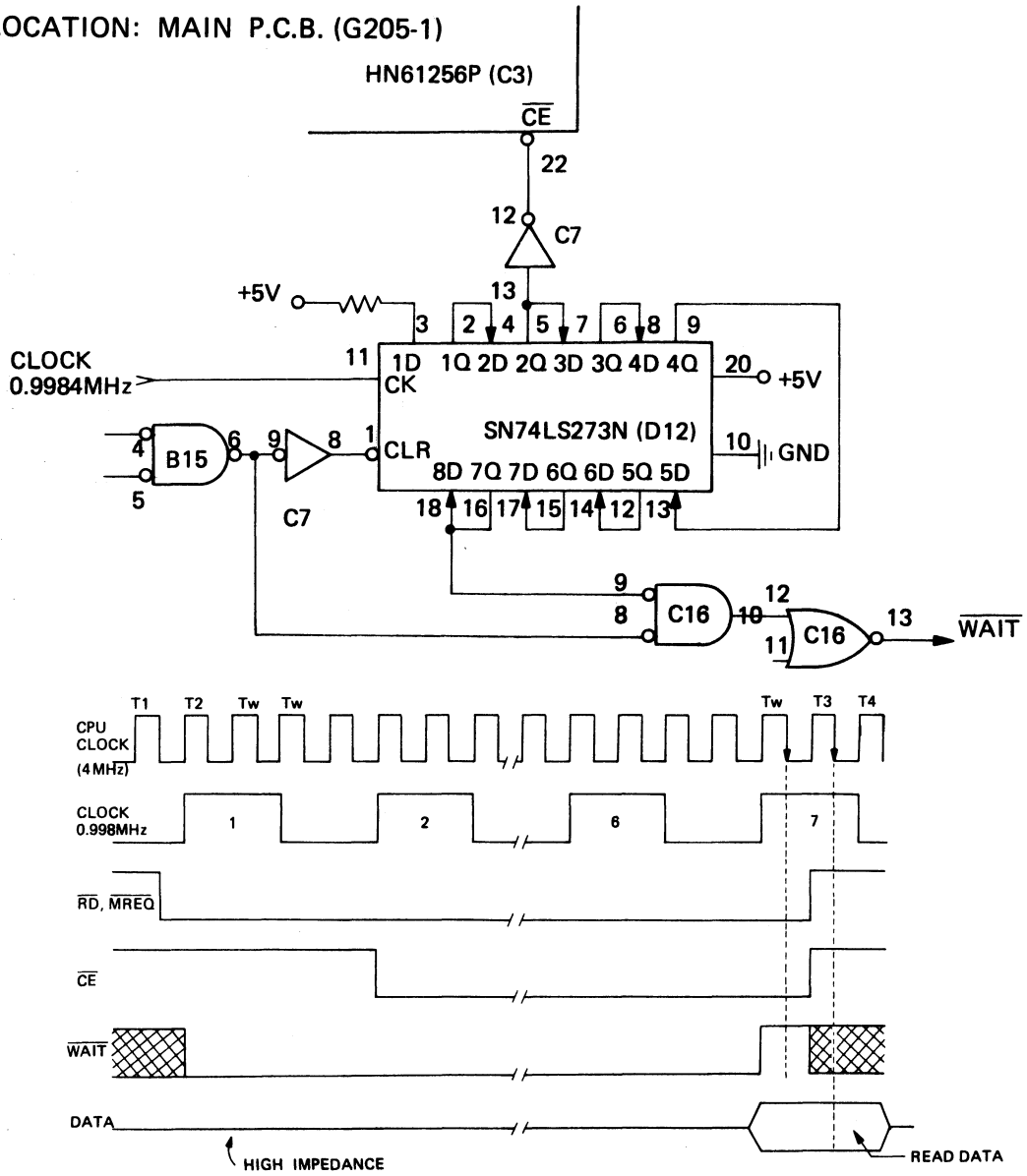


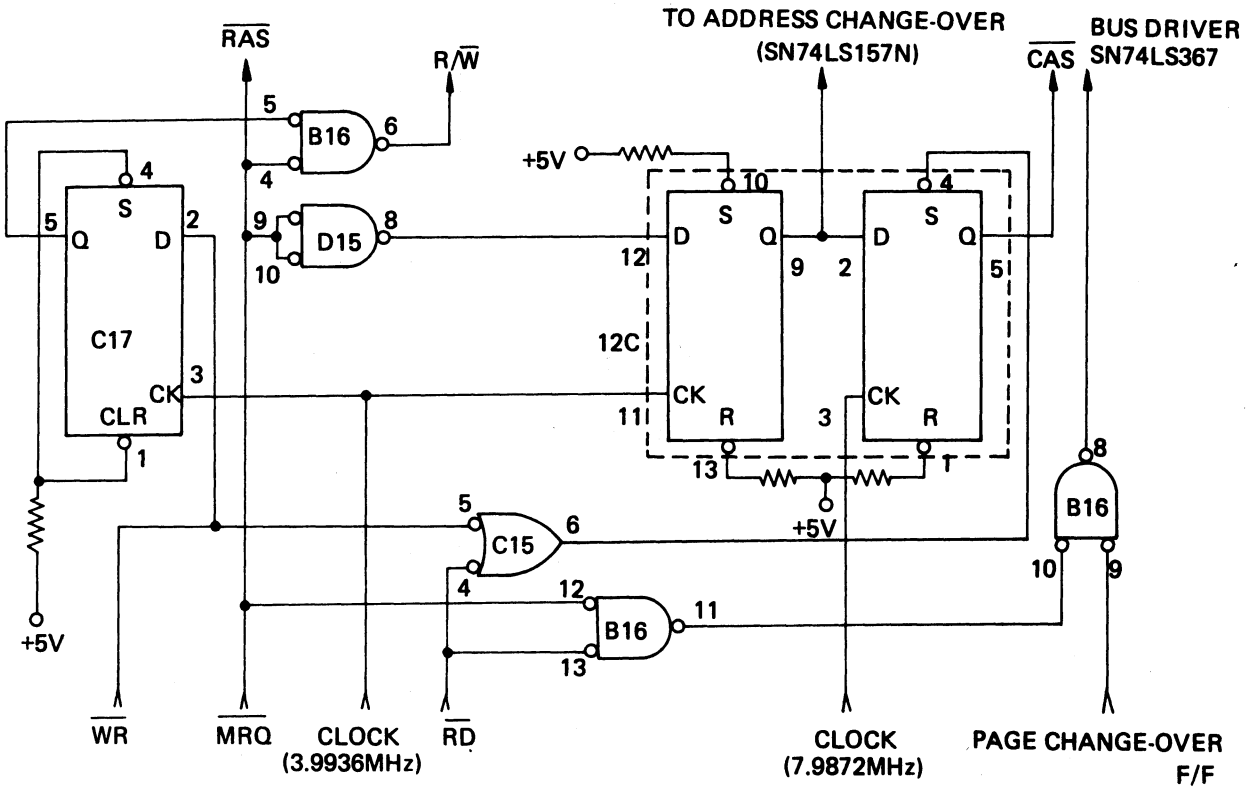
Fig. 8-2 READ CYCLE TIME CHART

8-4. RAM CONTROL SIGNAL GENERATE CIRCUIT:

RAM capacity in this unit is 64 Kbyte (8x8Kbytes) and the type is dynamic C-MOS RAM, and their addresses are designated by $\overline{RAS}$ (row address select) and $\overline{CAS}$ (column address select) signals. Both signals form $\overline{WR}$, $\overline{MQR}$ and $\overline{RD}$ signals from the main CPU and 2 clocks in the following circuit diagram.

Read and write timing of the memory are as follows.

LOCATION: MAIN P.C.B. (G205-1)



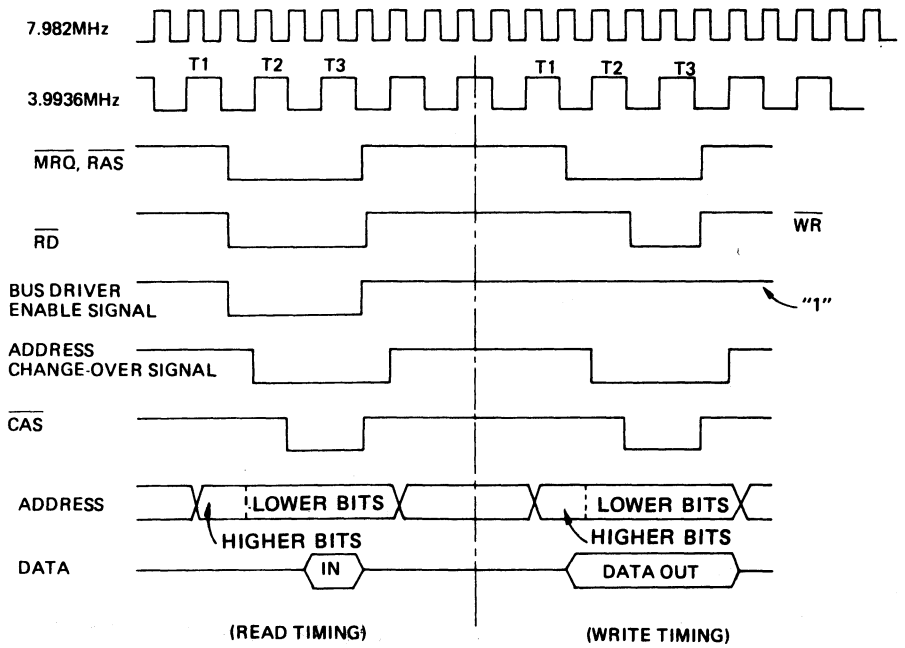
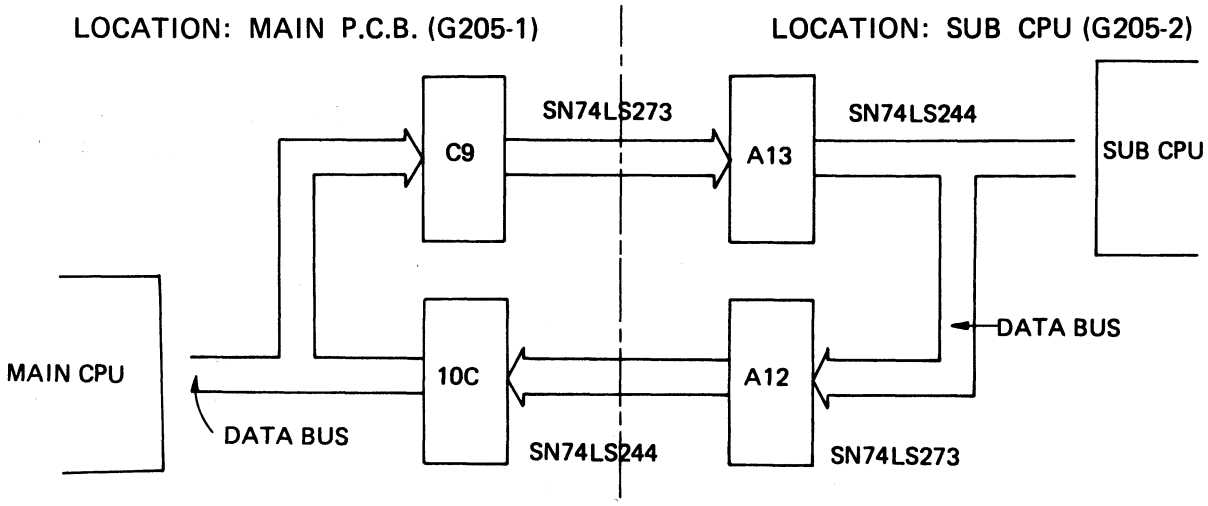


Fig. 8-3 TIMING CHART

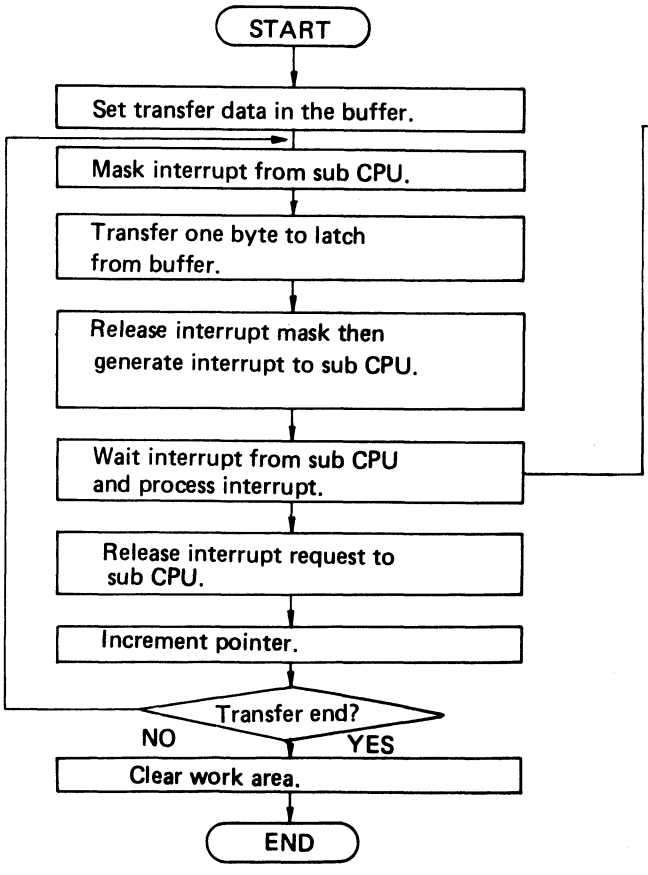
8-5. MAIN-SUB CPUs INTERFACE CIRCUIT:

The main CPU and sub CPU do not activate synchronously. Therefere, it is necessary to install an interface for the communication between the two devices.
Two 8-bit latches for the main CPU and the same two latches for the sub CPU are used for that purpose.

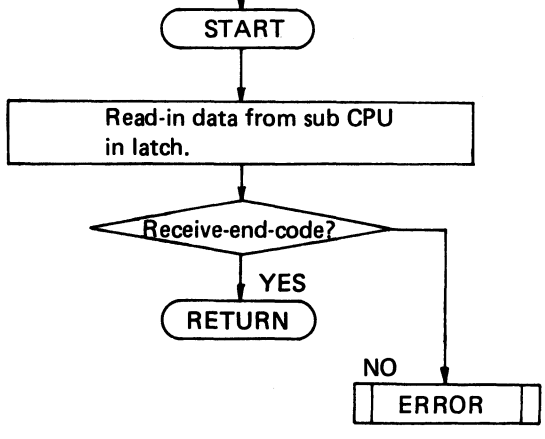


Address for read and write of the data by the main CPU to the latches are as follows.

READ:	FF80-FFFF	D7	D6	D5	D4	D3	D2	D1	D0	(SN74LS244)
WRITE:	FFC0-FFDF	D7	D6	D5	D4	D3	D2	D1	D0	(SN74LS273)



Sub CPU interrupt process flow



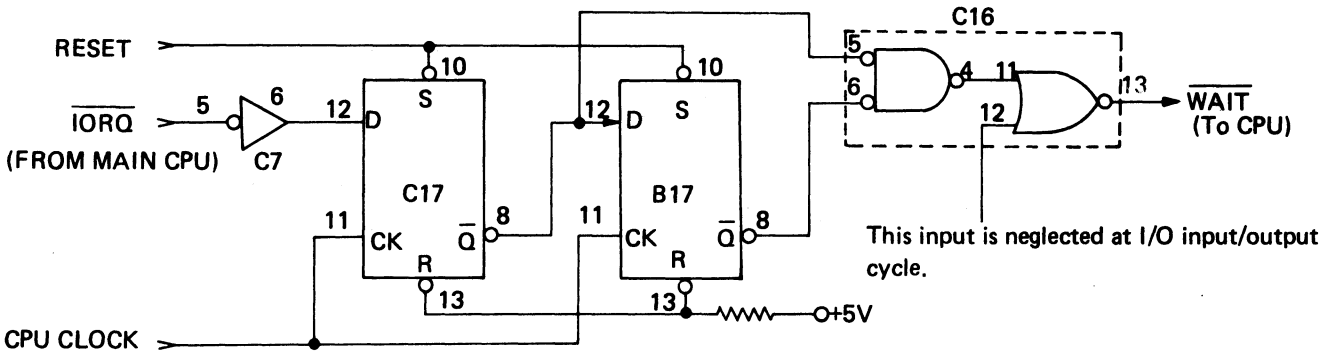
This example shows data transfer from the main CPU to sub CPU.

Fig. 8-4 DATA TRANSFER FLOW

8-6. $\overline{\text{WAIT}}$ SIGNAL GENERATE CIRCUIT:

At time of I/O input or output cycle, one $\overline{\text{WAIT}}$ pulse is generated to insert Tw pulses into the CPU clock in the following circuit when active $\overline{\text{IORQ}}$ (active low) that indicates I/O device code number is being output to address bus (other than M1 cycle duration) is input into flip-flop gate C17 through inverter gate C7. Refer to the following time chart for details of the signal formation.

LOCATION: MAIN P.C.B. (G205-1)



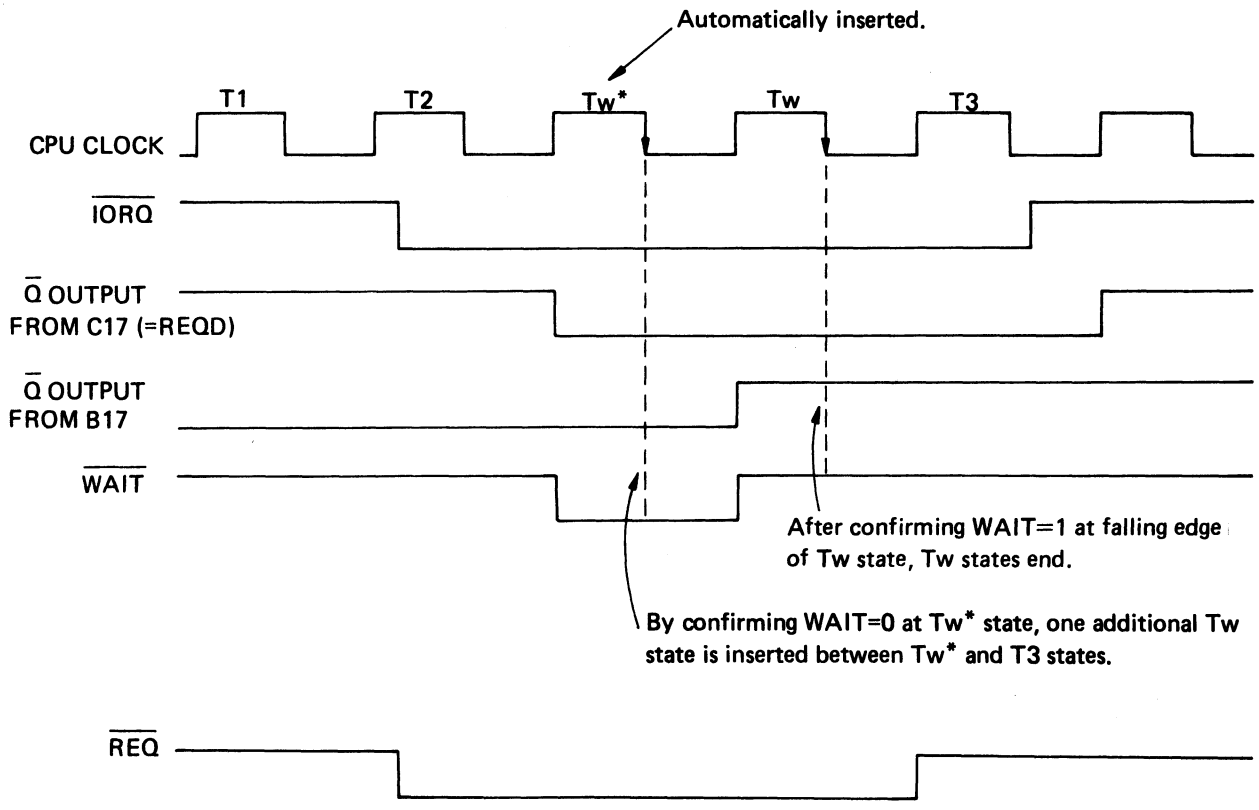
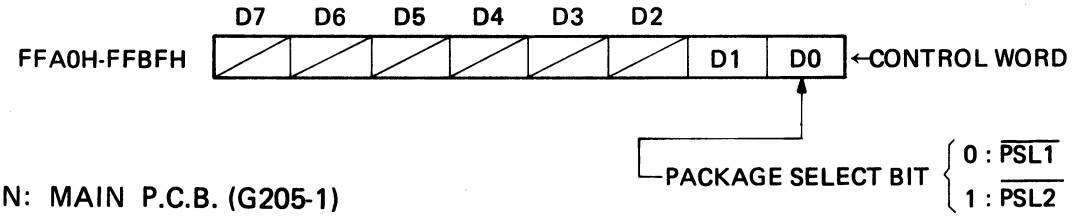


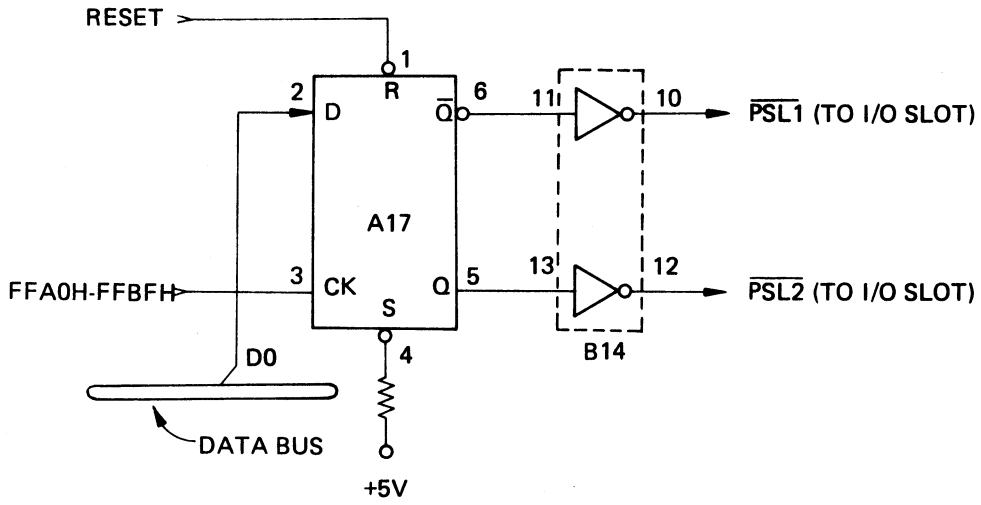
Fig. 8-5 MAJOR I/F SIGNAL TIME CHART

8-7. I/F CONTROL CIRCUIT:

This system unit has two I/O slots which connect optional memory packs such as the C-16K RAM pack and ROM pack, FDD unit, RS-232C interface pack, I/O box and so on.
These external peripheral devices are designated and controlled by $\overline{PSL1}$ and $\overline{PSL2}$ (stand for package select) that are generated in the following circuit.
Change-over of the control signals is executed by writing "1" or "0" in the first bit of the control word of I/O address space FFA0H-FFBFH. Type of device connecting to the system unit is distinguished by a reading device code number in each device by using the $\overline{CS}$ signal.



LOCATION: MAIN P.C.B. (G205-1)



SIGNAL NAME	PIN NO.	DESCRIPTION
D0 ~ D7	A13 ~ A16, B13 ~ B16	BIDIRECTIONAL DATA BUS
$\overline{A0} \sim \overline{A15}$	A17 ~ A24, B17 ~ B24	ADDRESS BUS
$\overline{RD}$	A7	READ SIGNAL
$\overline{WR}$	B7	WRITE SIGNAL
$\overline{REQ}$	A6	I/O SIGNAL RISING ONE CPU CLOCK EARLY
$\overline{REQD}$	B6	I/O SIGNAL RISING ONE CPU CLOCK DELAY
$\overline{CS}$	A8	DEVICE SELECT SIGNAL
$\overline{PSL1}$, $\overline{PSL2}$	1-A4, 2-A4	PACKAGE SELECT SIGNAL
$\overline{RST}$	B5	RESET SIGNAL
$\overline{INTA} \sim \overline{INTD}$	A11 ~ A12, B11 ~ B12	INTERRUPT REQUEST SIGNAL
$\overline{NMI}$	A10	NON MASKABLE INTERRUPT REQUEST SIGNAL
+5V, −5V	A1, 2, 26, 27, B25	POWER VOLTAGE
+12V, −12V	A3, B3, A25	POWER VOLTAGE
GND	B1, 2, 26, 27	SIGNAL GROUND
$\overline{BSL1}$, $\overline{BSL2}$	1-A5, 2-A5	I/O BOX SELECT SIGNAL

I/O INTERFACE

8-8. INTERRUPT CONTROL CIRCUIT:

There are six different kinds of interrupts to be utilized in this system and the priority order is:

INTS (or SUBINT) > INTA > INTB > INTC > INTD

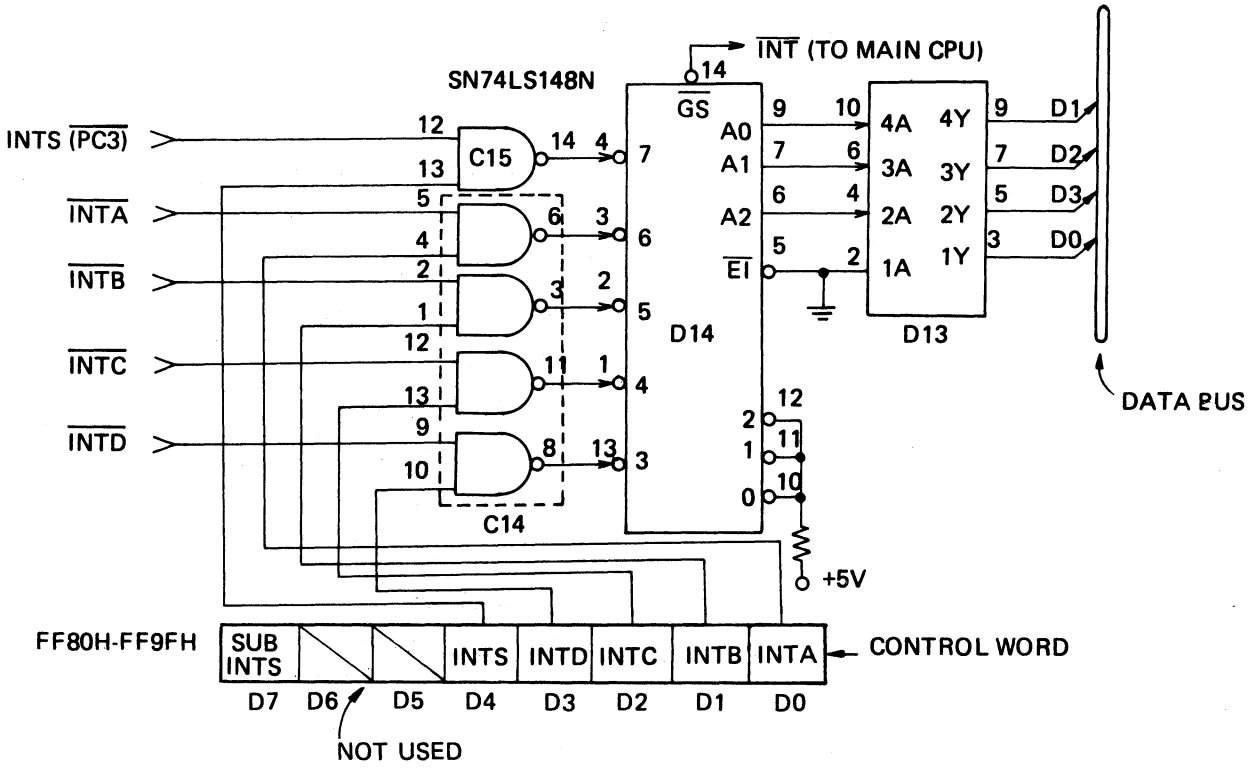
INTS is considered as the highest priority and indicates that the sub CPU has data to be transferred to the main CPU. SUBINT indicates that the main CPU has data to be transferred to the sub CPU.

Interrupts are input through NAND gates to be encoded and output each interrupt in higher priority order by the priority encoder device No. 14D when more than one interrupt is input into the device simultaneously.

The interrupt in the device is transformed in 3-bit code and the output to data bus. Highest priority order interrupt is always to be executed first, then the interrupt of which priority is second to the highest is to be executed and so on. Normally, all interrupts are executed in mode 2 in the main CPU.

This encoder features priority decoding of the inputs to ensure that only the highest-order data line is encoded. It is also capable of encoding eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry has been provided to allow octal expansion without need for external circuitry in this device. Data inputs and outputs are active at the low logic level.

LOCATION: MAIN P.C.B. (G205-1)



Interrupt: A break in the normal flow of a system or routine is such that the flow can be resumed from that point at a later time. An interrupt is usually caused by a signal from an external peripheral device.

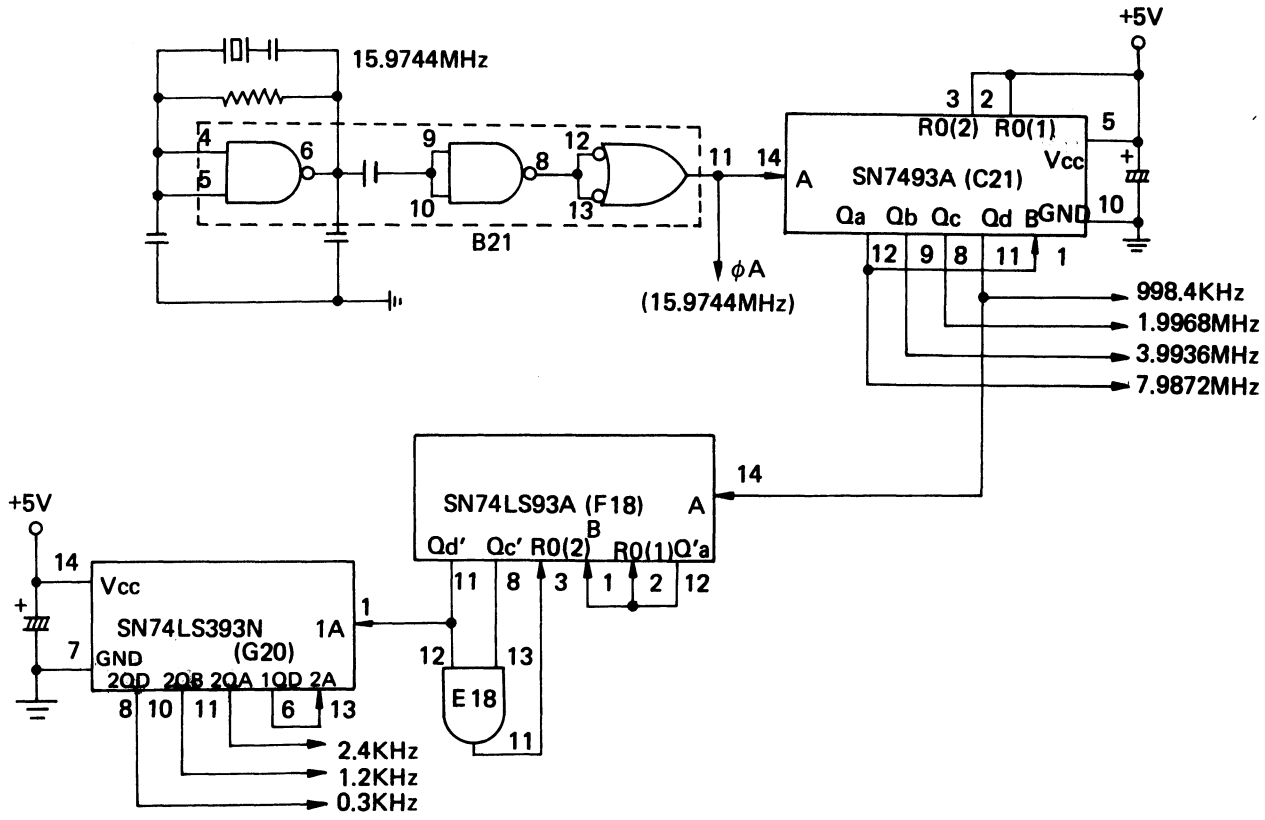
8-9. CLOCK GENERATE CIRCUIT:

Various clock pulses that synchronize device functions are generated in the following circuit. First of all, the crystal oscillator generates 15.9744MHz which becomes the master of clocks, then the frequency is demultiplexed into 8 different kinds of clock pulses in C21, F18 and G20 counters to be distributed in different cycles.

CLOCK CYCLE AND DESCRIPTION

CLOCK	DESCRIPTION
15.9744MHz	Dot clock for 80-character display mode
7.9872MHz	Dot clock for 40-character display mode
3.9936MHz	CPU clock
1.9968MHz	CRTC clock in 80-character display mode
0.9984MHz	CRTC clock in 40-character display mode
76.8KHz	Data sampling clock at load time in MT operation
2.4KHz	Data "1" (mark) clock at save time in MT operation
1.2KHz	Data "0" (space) clock at save time in MT operation and clock for 1200 baud rate
0.3KHz	Clock for 300 baud rate

LOCATION: SUB P.C.B. (G205-2)



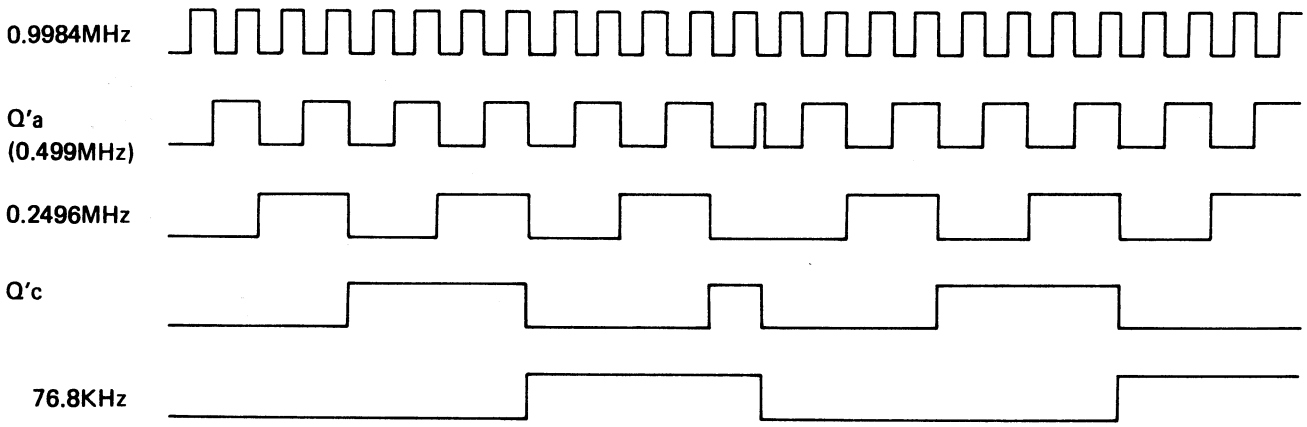


Fig. 8-6 Clock timing chart

8-10. SUB CPU PORTS:

Sub CPU μPD7801G has three different kinds of input/output port blocks that can be utilized as terminals for communications between the sub CPU and external peripheral devices.

Details of the port functions are described in the following table.

PORT	I/O	DESCRIPTION	WHEN "0"	WHEN "1"
PA0	OUT	R.G.B. video RAM display control	No green display	Green display
PA1	OUT		No red display	Red display
PA2	OUT		No blue display	Blue display
PA3	OUT	Change-over for CRT clock	80-character mode	40-character mode
PA4	OUT	Change-over for green/color	Color display	Green display
PA5	OUT	Clear video RAM	Display normally	Clear
PA6	OUT	Change-over MT baud rate	Set 1200 baud	Set 300 baud
PA7	OUT	Change-over MT clock	"LOAD" clock	"SAVE" clock
PB0	I/O	Bus terminal for "KEY IN" signals from keyboard and data signals of Centronix I/F	Output to printer	Input from keyboard
PB1	I/O			
PB2	I/O			
PB3	I/O			
PB4	I/O			
PB5	I/O			
PB6	I/O			
PB7	I/O			
PC0	I/O	Centronix I/F $\overline{\text{BUSY}}$ signal	Not busy	Busy
PC1	I/O	Centronix I/F $\overline{\text{ERROR}}$ signal	Error	Not error
PC2	IN	MT "LOAD" clock input		Read-in data
PC3	OUT	Interrupt from sub to main CPU	Active	Not active
PC4	OUT	Designate Centronix input/output	Output mode	Input mode
PC5	OUT	Remote control signal output to MT	Off	On
PC6	OUT	Centronix I/F $\overline{\text{STROBE}}$ signal output	Active	Not active
PC7	IN	Serial data input from MT		

SUB CPU PORT FUNCTION TABLE

8-11. RESET SIGNAL CIRCUIT:

There are two ways to generate a RESET signal for initializing the system.
One way is when the power switch is turned on or AC input voltage becomes extraordinarily low, the other is when the RESET switch is pushed in.

Low level of PWD signal (from power supply circuit) at base of transistor 1 causes the transistor to be opened, and +12V is applied to base of transistor 2 . Because transistor 2 is turned on +12V at the base, current between the collector and the emitter flows. Thus, the voltage drop at the collector becomes the same voltage level with GND.
Because a large number of fan-outs are required for the RESET signal, a common emitter follower circuit has been adapted to gain high amplification and consistent stability in this system.

LOCATION: SUB P.C.B. (G205-2)

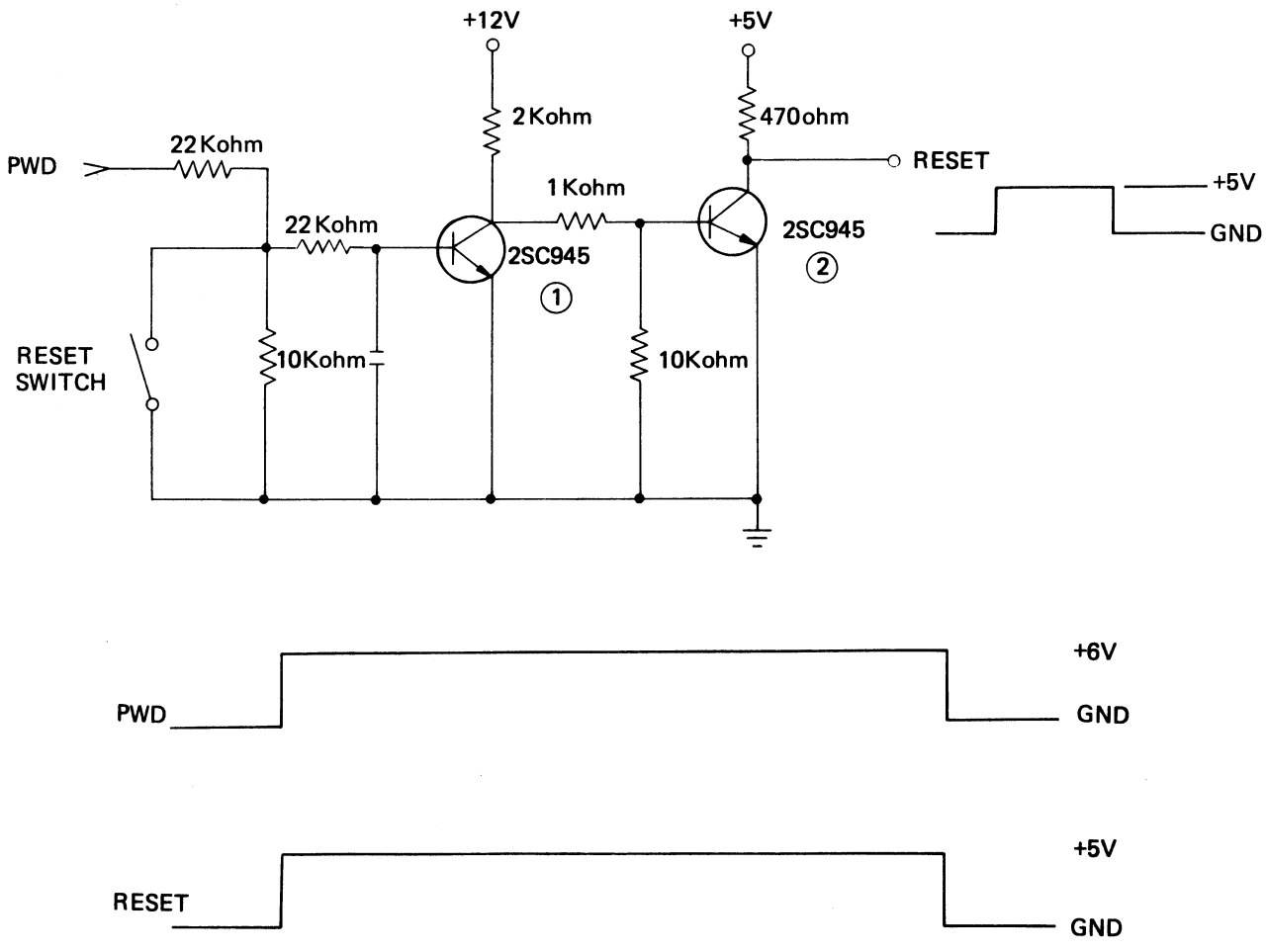
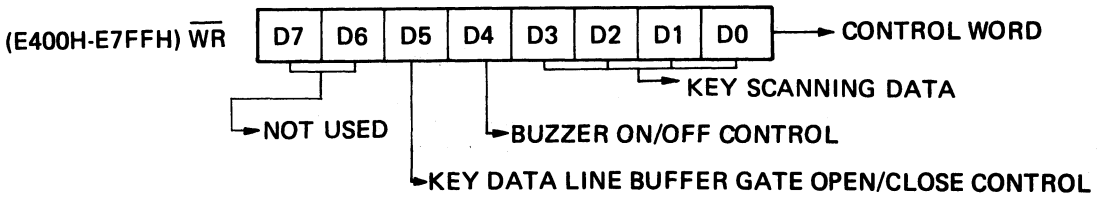


Fig. 8-7 RESET SIGNAL WAVEFORM

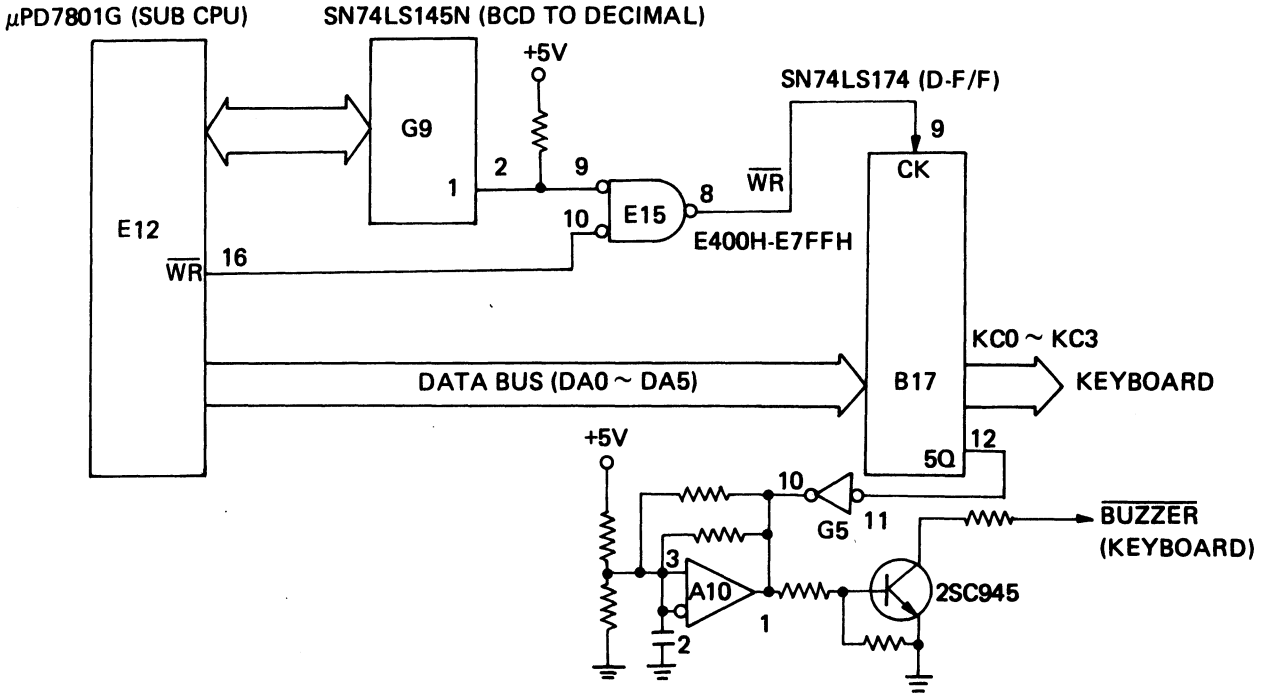
8-12. KEYBOARD CONTROL CIRCUIT:

The keyboard used in this personal computer is known as the scan method in software which enables a keyboard operator to enter input from the keyboard with two keys about the same time (2 keys roll-over) and the keyboard is in conformity with ASCII.
The sub CPU will determine what type of keyboard is connected with it right after the power switch is turned on by reading 5 bits in memory address space from E400-E7FFH.
Key scanning is executed by writing in 0 to 3rd bit in the memory address space E400-E7FFH. Also by writing in the control word, the following functions can be performed.



1) Buzzer control:
By writing "1" in the 4th bit, the buzzer will be turned on.

LOCATION: SUB P.C.B. (G205-2)

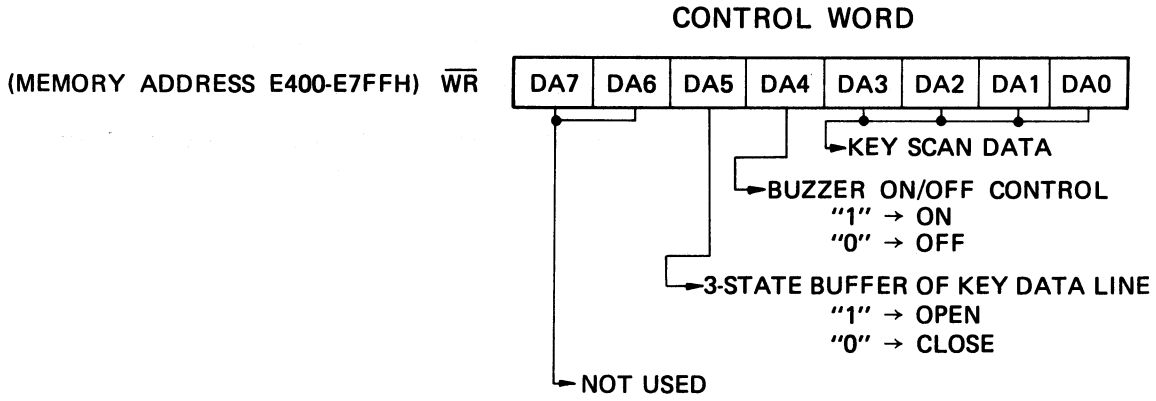


2) Buffer control:
By writing "1" in the 5th bit, input data from the keyboard can enter into Port PB0 ~ PB7 in the sub CPU.

3) L.E.D. control:

Two L.E.Ds on the keyboard are controlled by writing in DA0 ~ DA3 bits. The following table shows details.

DA3	DA2	DA1	DA0	L.E.D. CONDITION
1	1	0	1	"SHIFT LOCK" ON
1	1	1	0	"CAPS" ON
1	1	1	1	ALL L.E.Ds OFF



8-13. PRINTER INTERFACE:

The Centronix standard 8-bit parallel interface is used in this system unit. This interface transmits data and $\overline{\text{STROBE}}$ signal and other timing signals from/to the CPU synchronously.

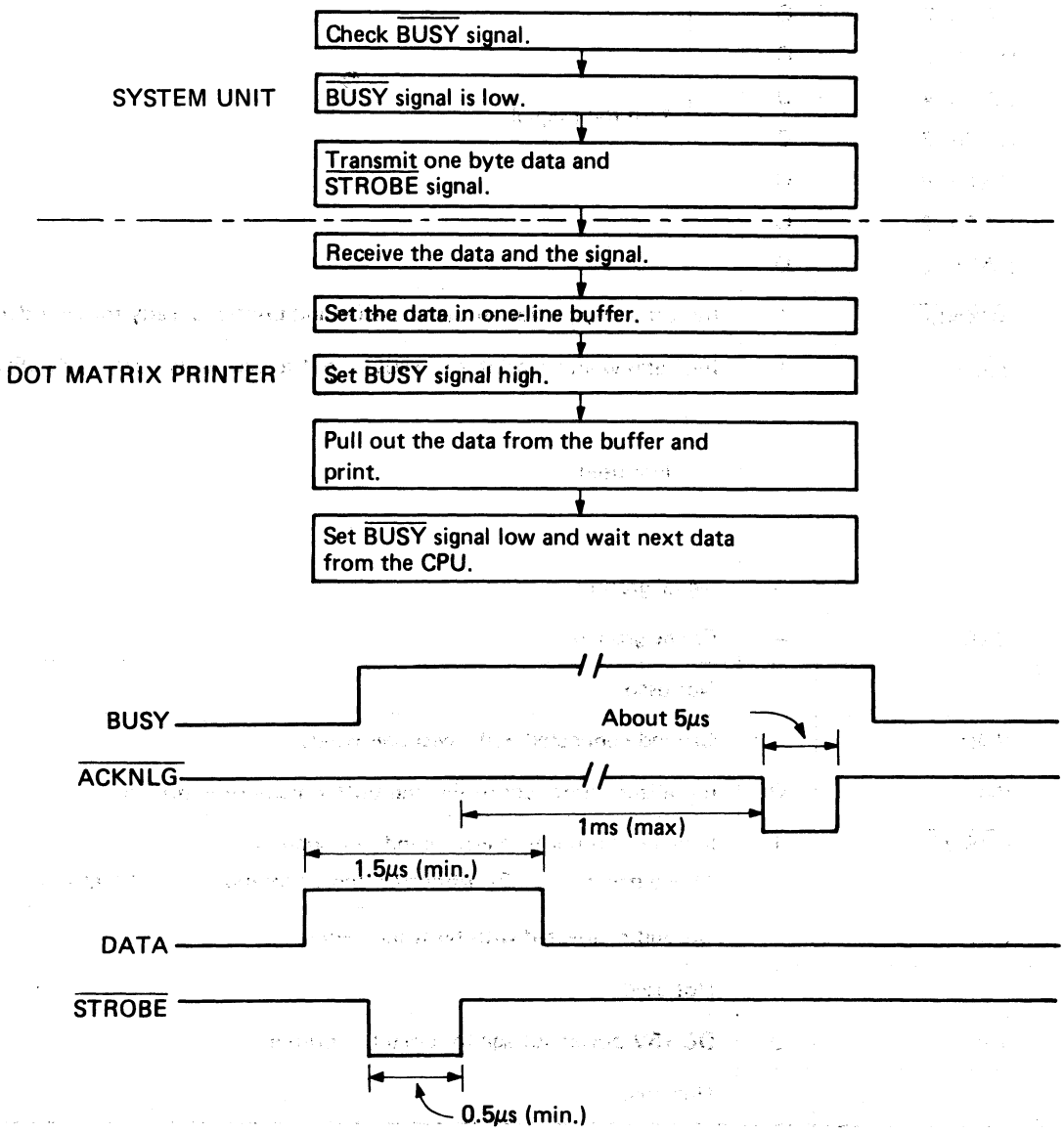


Fig. 8-8 INTERFACE TIMING CHART

PRINTER INTERFACE

PIN NO.	SIGNAL NAME	I/O	DESCRIPTION
1	$\overline{\text{STROBE}}$	I/O	Normally high. Active pulse requires more than 0.5μs.
2	DATA 1	O	8-bit data signal.
3	DATA 2	O	
4	DATA 3	O	
5	DATA 4	O	
6	DATA 5	O	
7	DATA 6	O	
8	DATA 7	O	
9	DATA 8	O	
10	$\overline{\text{ACKNLG}}$	I	Indicates completion of data transfer and printer is ready for next data.
11	$\overline{\text{BUSY}}$	I	Indicates whether printer is ready or not to accept data from sub CPU.
12			Not used.
13			
14			
15			
16	0V	–	Signal ground.
17	GND	–	Frame ground.
18			Not used.
19~30	GND	–	Ground connected with twist pair wires.
31	$\overline{\text{INIT}}$	O	Initializes printer controller and buffer memory in printer.
32	$\overline{\text{ERROR}}$	I	Indicates printer is in error condition such as: 1) No paper. 2) Abnormal motor rotation. 3) Off-line.
33	GND	–	Ground connected with twist pair wires.
34			Not used.
35	+5V	O	DC +5V power voltage for circuit in printer.
36			Not used.

Note: I/O direction is viewed from system unit side.

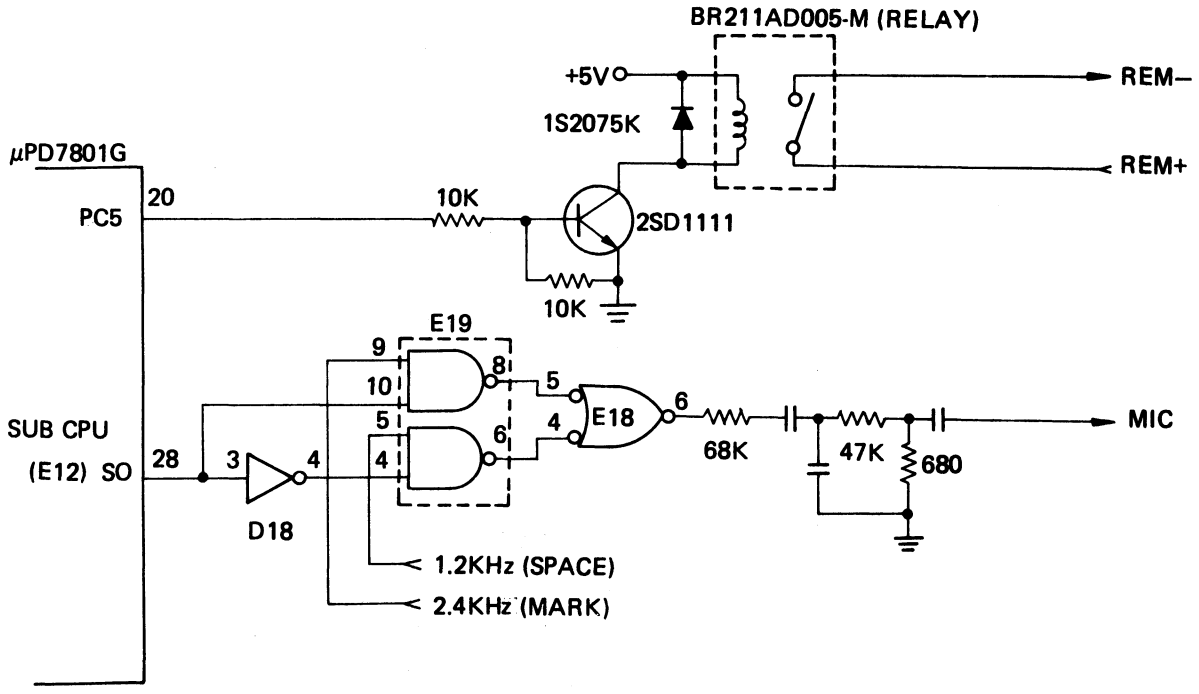
8-14. CMT CONTROL CIRCUIT:

This system unit has a built-in interface for CMT (cassette magnetic tape) which can be utilized as one of the external memory storage devices.
The interface does not require an additional intermediate device and can access from the sub CPU to a commercially sold cassette tape player as long as the following specifications are met:

1) MIC terminal : OUTPUT IMPEDANCE 5Kohm
   OUTPUT VOLTAGE 3mVp-p
2) EAR terminal : INPUT IMPEDANCE 10Kohm
   INPUT VOLTAGE 3 ~ 10Vp-p
3) REMOTE terminal: 24V, 1A

Data transfer speed (baud rate) can be designated in software. However, 300 baud will be automatically selected if no selection is made in the software.
Although mode selector switch No. 4 at bottom of the system unit can select the baud rate 1200 or 300 in hardware, the selection in the software has priority over the mechanical selection.

LOCATION: SUB P.C.B. (G205-2)



PIN NO.	I/O	SIGNAL NAME	DESCRIPTION
1	–	+5V	DC +5V power voltage.
2	–	GND	Signal ground.
3			Not used.
4	O	MIC	Output signal to cassette player.
5	I	EAR	Input to system unit.
6	–	REM +	Connect cassette player remote terminal with these terminals.
7	–	REM –	
8			Not used.
		FG	Frame ground.

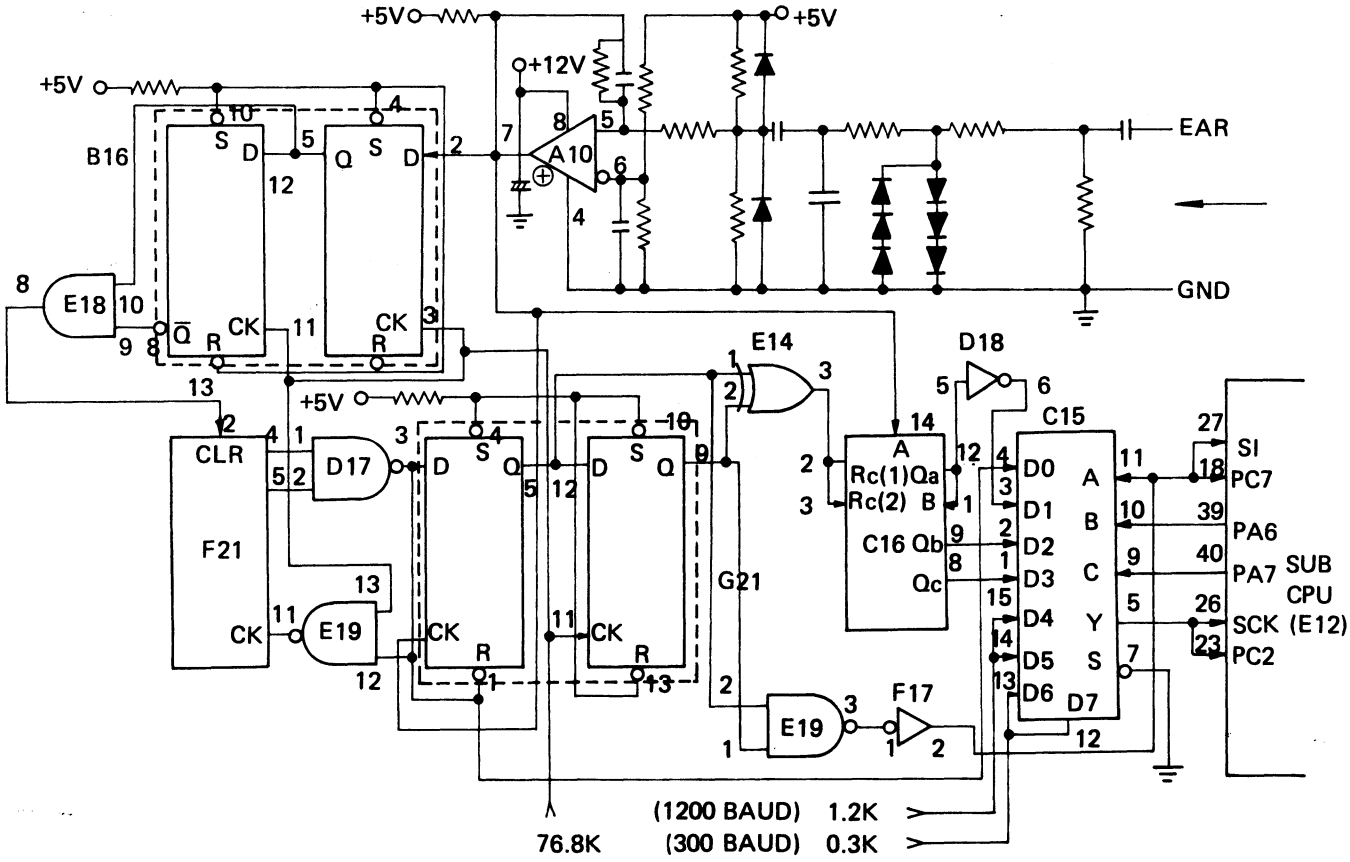
CMT INTERFACE

8-15. DATA SAMPLING CIRCUIT:

Limiter at entry stage of this circuit cuts above the 5V level of input data to meet the 5V TTL level and input that data into the data sampling circuit.

In this circuit, the data after the limiter circuit is separated from the timing pulses. ICs 16C and 15C generate serial clocks with synchronization of baud rate frequency which enables the data to enter into register possible in the sub CPU. The data can enter into serial register at the rising edge of the control clock through the SI terminal. In the sub CPU, the data is converted from serial to parallel data.

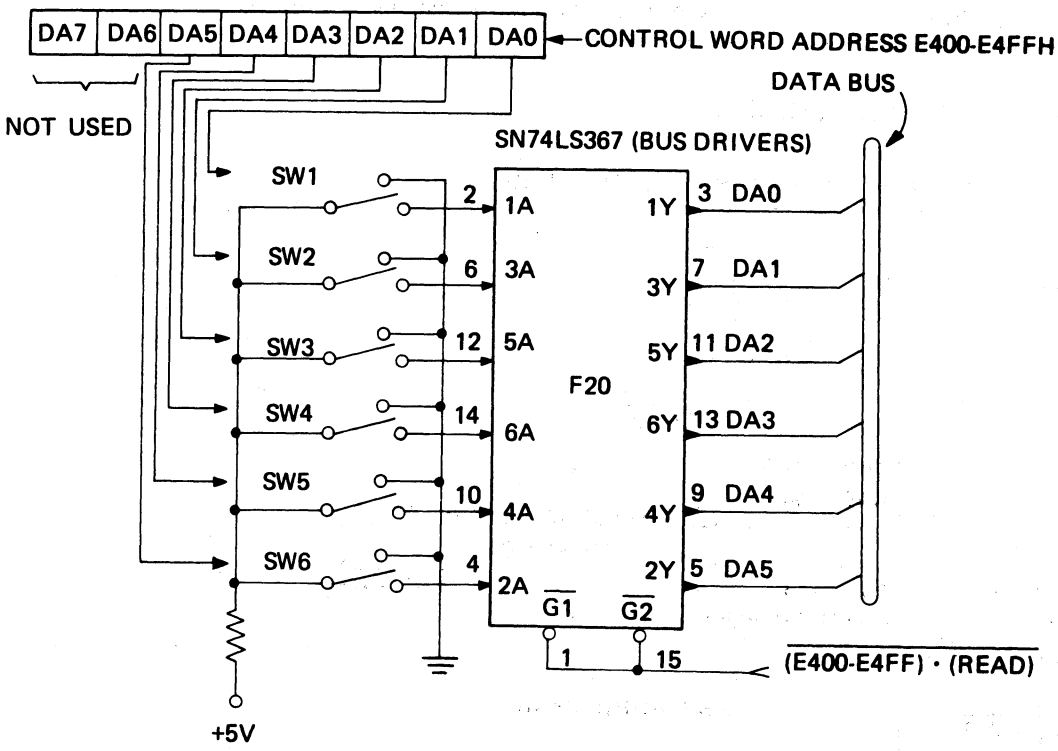
LOCATION: SUB P.C.B. (G205-2)



8-16. MODE SELECTOR SWITCH:

Six mode selector switches are located underneath the CPU box. These selector switches are utilized to select the following modes.
Right after the power switch is turned on, the sub CPU reads memory space of address E400H-E4FFH and finds condition of the switch.
However, the mode can be changed in software and the software has priority over the condition of the switch.

LOCATION: SUB P.C.B. (G205-2)



SWITCH NO.	SELECTION MODE	ON	OFF
1	Number of characters in horizontal direction on display	80-character	40-character
2	Screen mode	Screen 1	Screen 0
3	Model selection	FP-1100	FP-1000
4	CMT baud rate selection	300 baud	1200 baud
5	Printer selection	FP-1012PR	
6	Keyboard selection	Always ON	

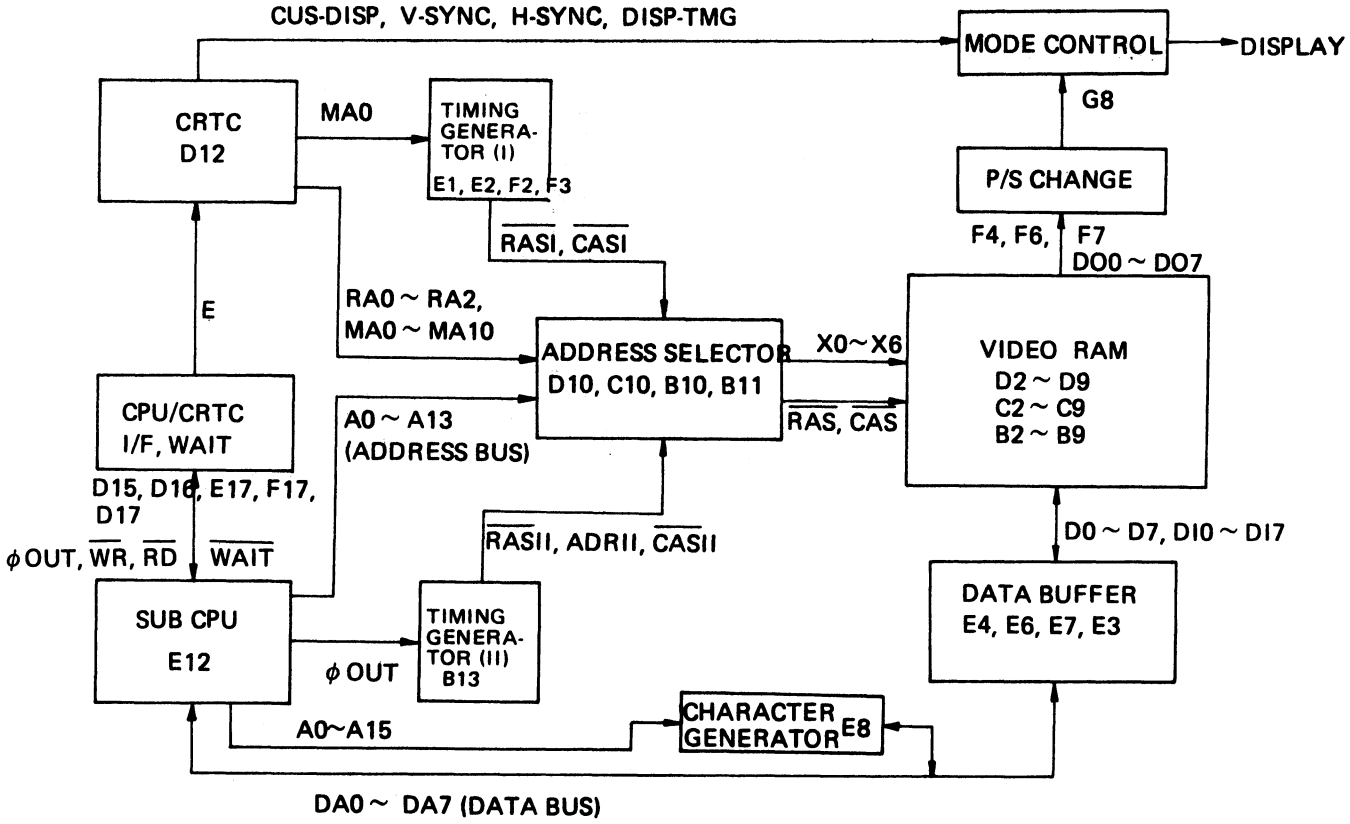
MODE SELECTION TABLE

8-17. DISPLAY CONTROL:

For the raster scan method, HD46505SP CRT controller has been adapted in this system unit. 48Kbytes of video RAM for FP-1100 (color) and 16Kbytes for FP-1000 (green) are utilized for video signal memory respectively.

	INTERLACE MODE		NORMAL MODE	
NUMBER OF HORIZONTAL DISPLAY CHARACTERS	40	80	40	80
NUMBER OF VERTICAL DISPLAY CHARACTERS	25	25	25	25
DOT NUMBER	320x400	640x400	320x200	640x200

LOCATION: SUB P.C.B. (G205-2)



- Dot number in a character composition { 8 (H) x 8 (V) dots
  8 (H) x 16 (V) dots for interlace mode.

- Video signal : R.G.B. for FP-1100
  Composite for FP-1000

The video control circuit consists of the following blocks:

1) Timing generator (I), (II)
   This block generates $\overline{RAS}$ (row address selector) and $\overline{CAS}$ (column address selector) for video RAMs.
2) Video RAM address selector
   This block designates video RAM address by changing over between address (MA0 ~ 10) from CRT controller and address (A0 ~ A13) from the sub CPU.
3) Data buffer
   These buffers are utilized for the data bus between the sub CPU and the video RAMs.
4) P/S (parallel and serial) change-over
   Video data (signal) to be transferred to the display unit is converted from parallel data to serial data in this block.
5) Mode control
   This block controls screen mode on the display unit. The selection menus are interlaced or normal, and color or green.
6) I/F and WAIT signal circuit for CPU/CRT controller
   This block generates enable signal for CRT controller and WAIT signal for the sub CPU.

Display theory :

To indicate characters on the CRT screen and hold it for a while, it is necessary to continue scanning and refresh the screen continuously.
In the refresh memory, display data written in cannot be displayed as is. This is because the data in the memory is written with ASC II code.
The character code thus must be converted into the character pattern mode.
The device used to perform this operation is called a character generator. It may be a sort of ROMs that can generate a character pattern with address which consists of a character code and raster line number.
Normally, because one dot of a character time is less than 10 nanoseconds, the theory, that reads character dots by row or column in parallel to generate the character pattern and then converts it into serial for display signal, is adapted.
For alphabetical and numerical display, a 5x7 or 7x9 dot matrix composition is widely used.

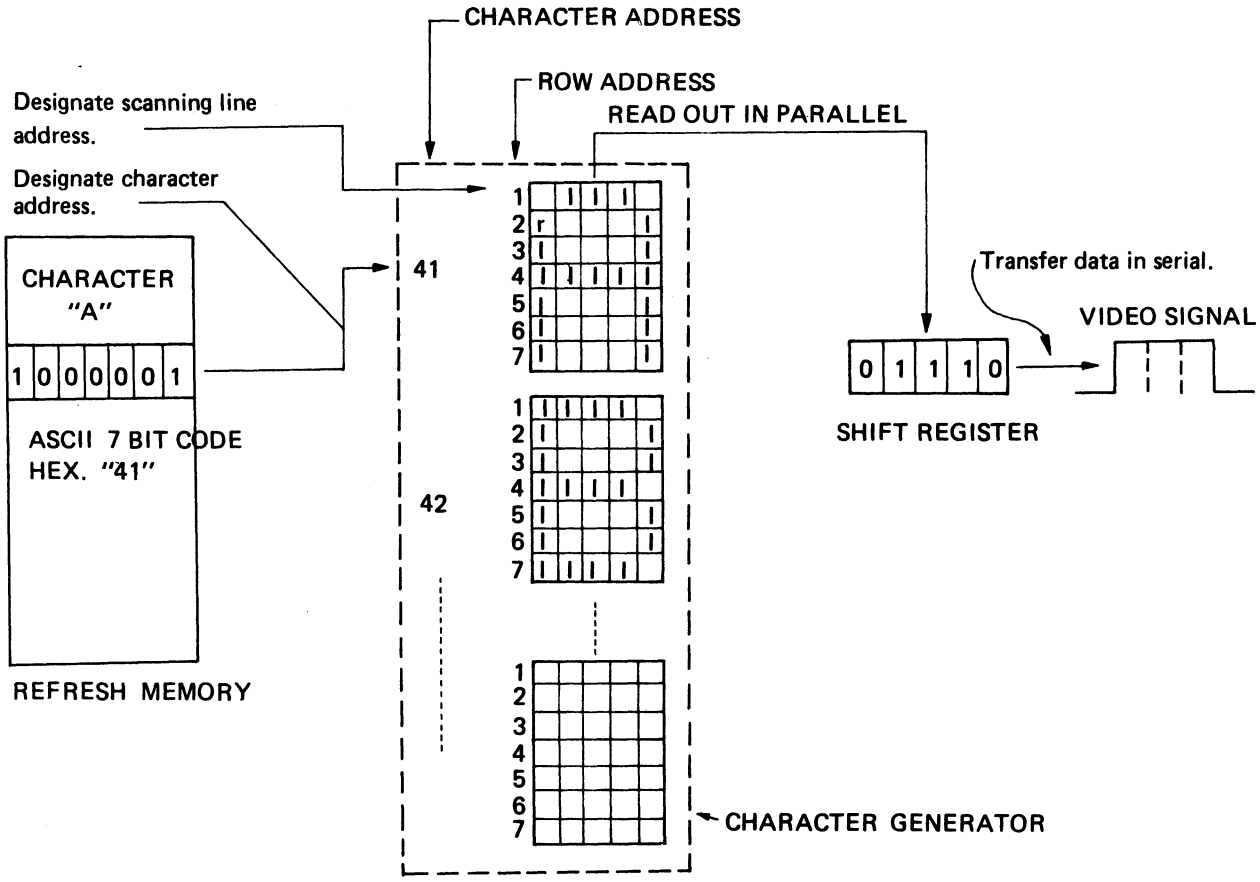
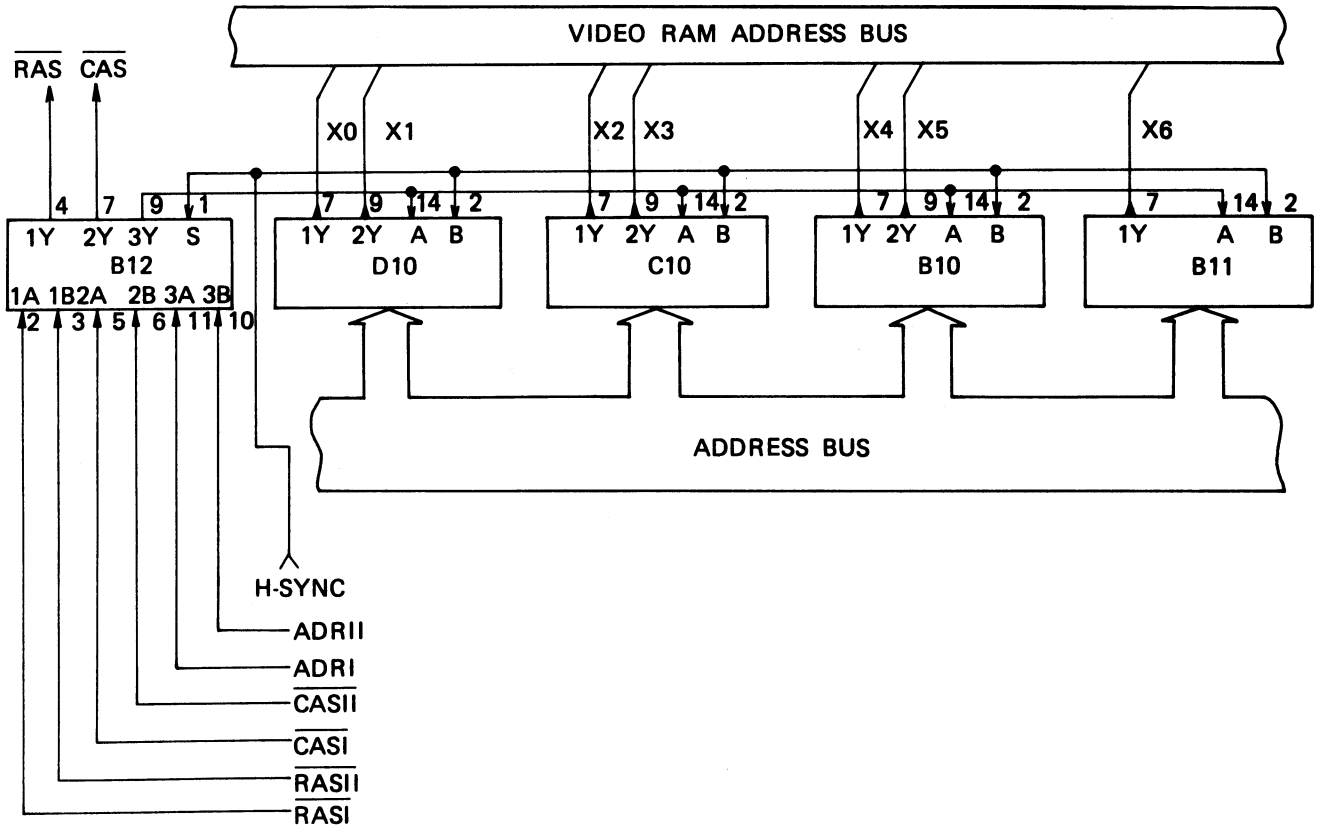


Fig. 8-9 CHARACTER GENERATION THEORY

8-18. VIDEO RAM ADDRESS SELECTOR:

The following circuit is an address selector for the video RAMs. It changes over RAM address when access to the video RAMs is made by either the CRT controller or the sub CPU. Refer to the following ADDRESS CORRESPONDENCE table for details:

LOCATION: SUB P.C.B. (G205-2)



		X6	X5	X4	X3	X2	X1	X0
CRTC ADDRESS	HIGHER BIT	MA10	MA9	MA8	MA7	MA6	MA5	MA4
	LOWER BIT	MA3	MA2	MA1	MA0	RA2	RA1	RA0
CPU ADDRESS	HIGHER BIT	$\overline{A13}$	A12	A11	A10	A9	A8	A7
	LOWER BIT	S6	A5	A4	A3	A2	A1	A0

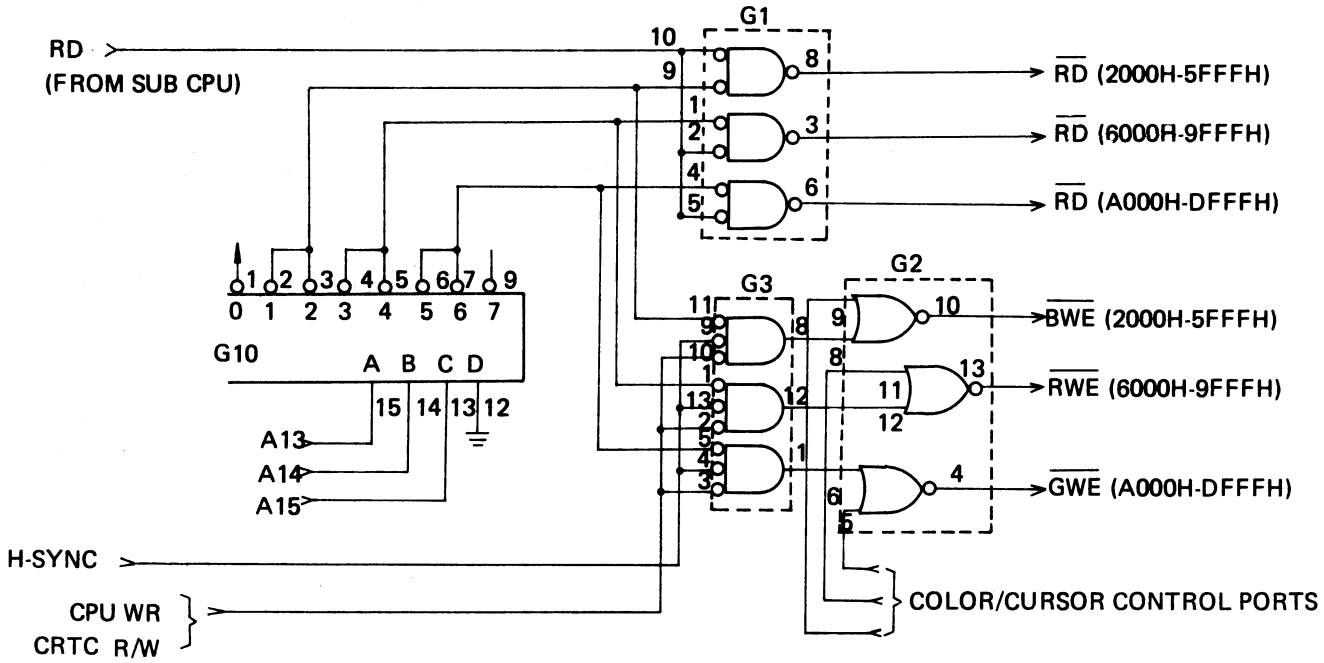
ADDRESS CORRESPONDENCE TABLE

RAM: This type of memory is random because it provides immediate access to any storage location point in the memory by means of vertical and horizontal coordinates. Information may be "written in" or "read out" in the same fast procedure.

8-19. VIDEO RAM $\overline{CS}$ & R/$\overline{W}$ SIGNAL GENRATE CIRCUIT:

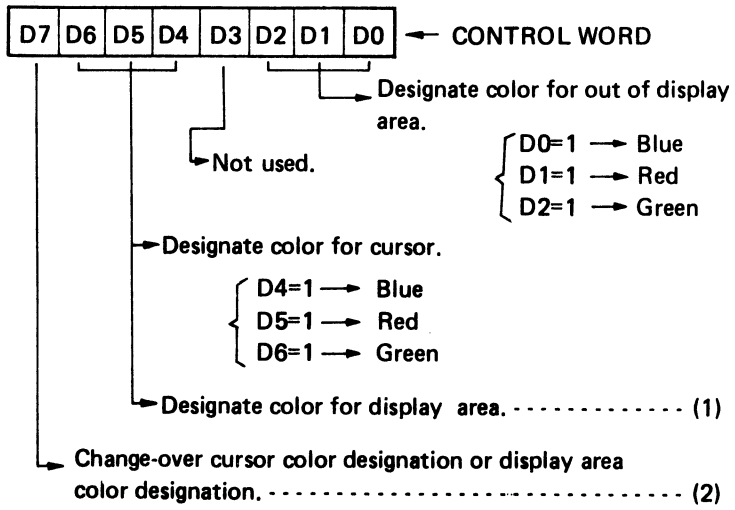
This circuit generates the $\overline{CS}$ (chip select) signal which allows reading and writing data in the RAMs and R/$\overline{W}$ signal which designates read or write execution.
High level of R/$\overline{W}$ signal designates reading function and low level designates writing function respectively.
Accessing the RAMs by the sub CPU is executed during the horizontal fly-back period.

LOCATION: SUB P.C.B. (G205-2)



COLOR/CURSOR CONTROL description is as follows:

	D0	D1	D2
	D4	D5	D6
BLACK	0	0	0
BLUE	1	0	0
RED	0	1	0
MAGENTA	1	1	0
GREEN	0	0	1
CYAN	1	0	1
YELLOW	0	1	1
WHITE	1	1	1

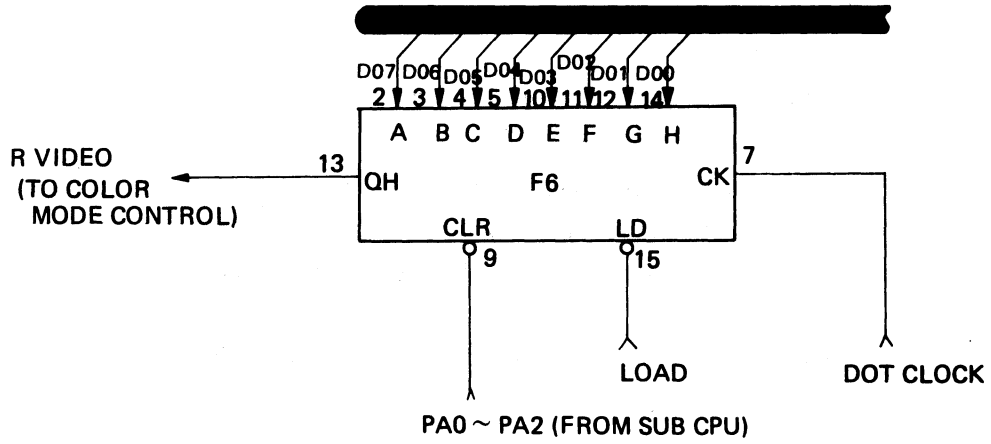


Note: (1) Color designation can be executed when D7 bit is "1".
(2) D4 ~ D6 bits designate color for cursor when D7 bit is "0" and color for display area when D7 bit is "1".

8-20. P/S (parallel to serial) CONVERSION CIRCUIT:

This circuit converts data in parallel from video RAMs to serial data synchronizing with the dot clock (7.9872MHz or 15.9744MHz).
Then it inputs the data into a color mode control device G8. The data output to CRT can be implemented with a horizontal display period (when DISPTMG from the CRT controller is "1"). The data can also be turned off by PA0 ~ PA2 port port signals from the sub CPU.

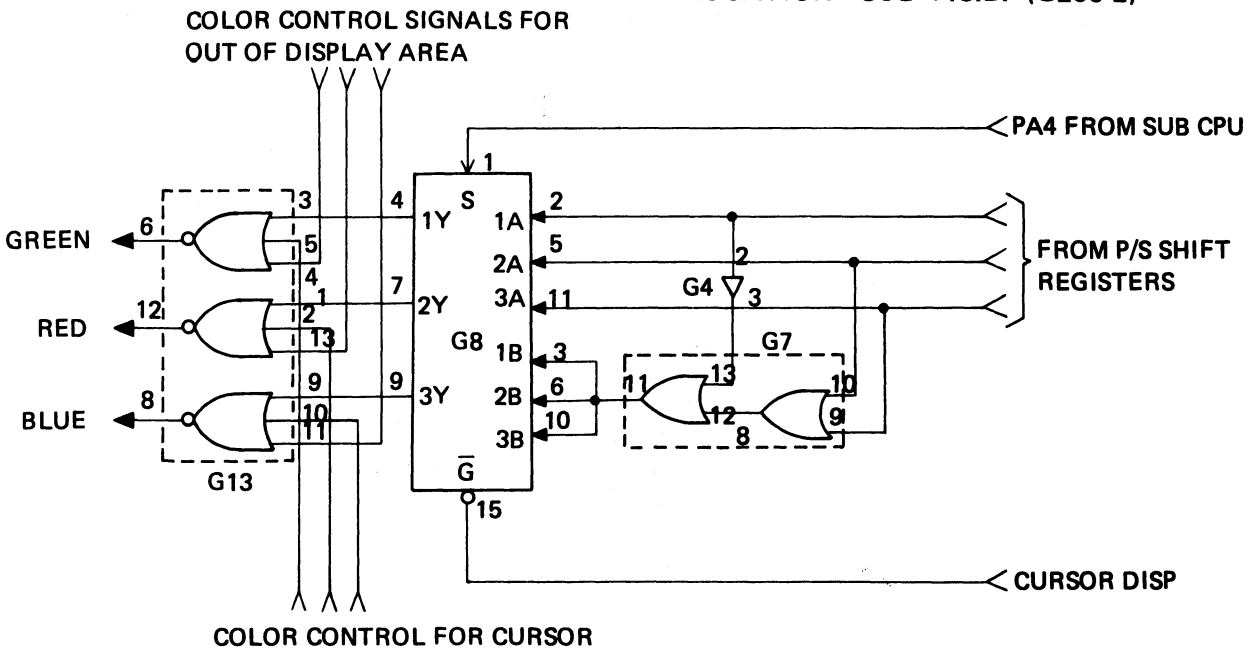
LOCATION: SUB P.C.B. (G205-2)

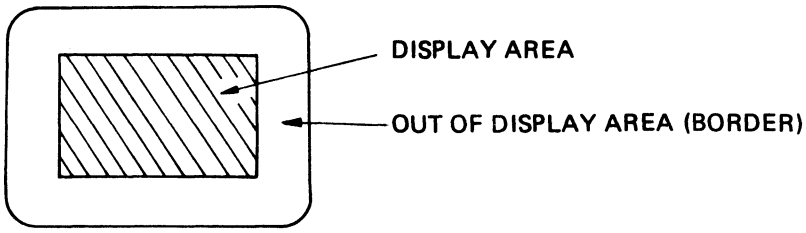


COLOR MODE CONTROL CIRCUIT:

The following circuit is to control color for the display area, out of the display area and the cursor.
The converted data is NORed by color control signals for out of the display area and the cursor, then transferred to the display (CRT) unit.
PA4 signal from the sub CPU controls color mode or mono color (green) mode by presenting "0" (color) or "1" (mono color).

LOCATION: SUB P.C.B. (G205-2)



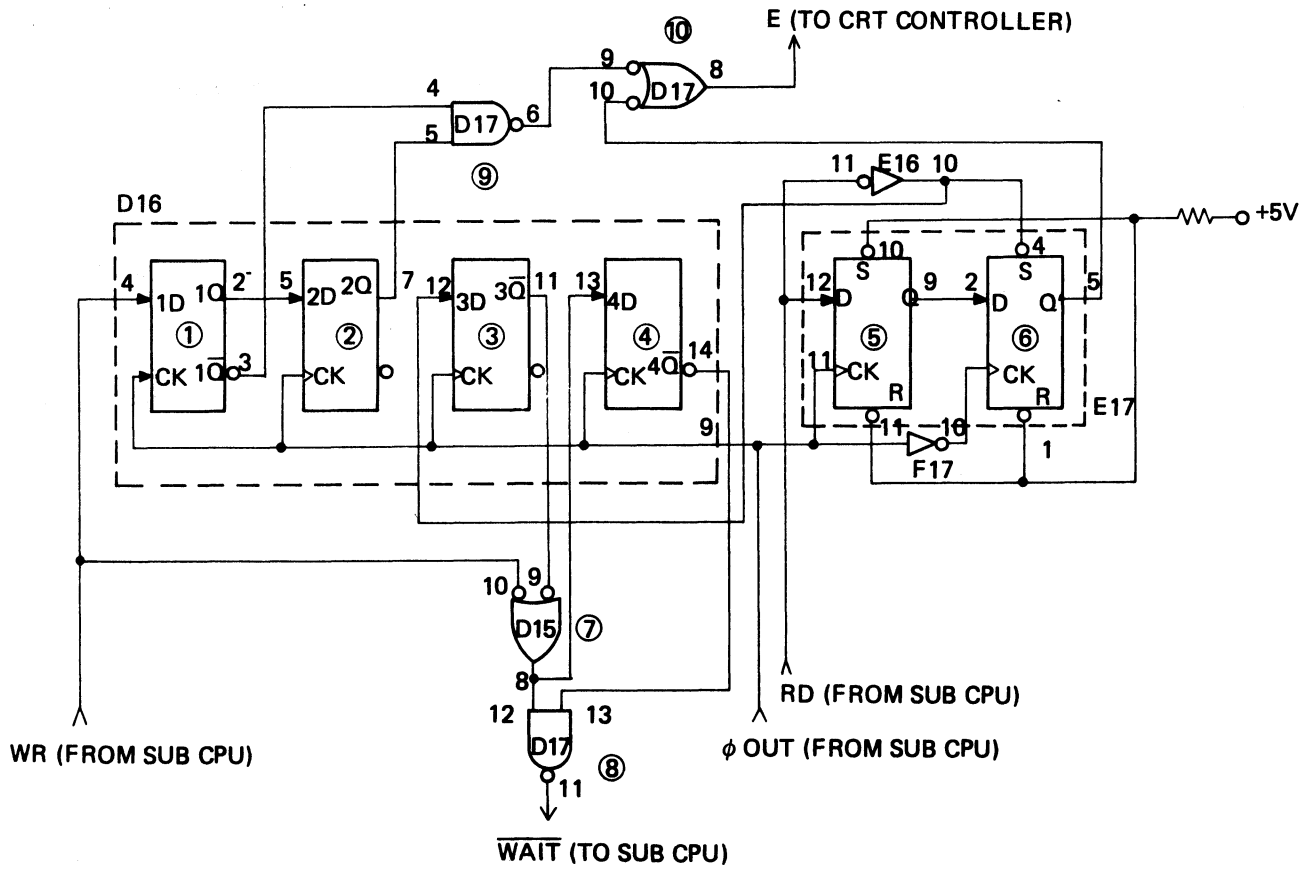


NOR gate: one of logic gates having multiple inputs and one output that is energized only if all inputs are zero.

8-21. I/F & WAIT SIGNALS GENERATE CIRCUIT:

③, ④, ⑦ and ⑧ in the followjng circuit generate a $\overline{\text{WAIT}}$ signal which can be used to delay ϕ OUT clock for one cycle at reading and writing by the sub CPU. ①, ② and ⑨ generate E (enable) signal provided to the CRT controller at access from the sub CPU to the CRT controller.
⑤ and ⑥ flip-flops generate E (enable) signal provided to the CRT controller at access from the CRT controller to the sub CPU.

LOCATION: SUB P.C.B. (G205-2)



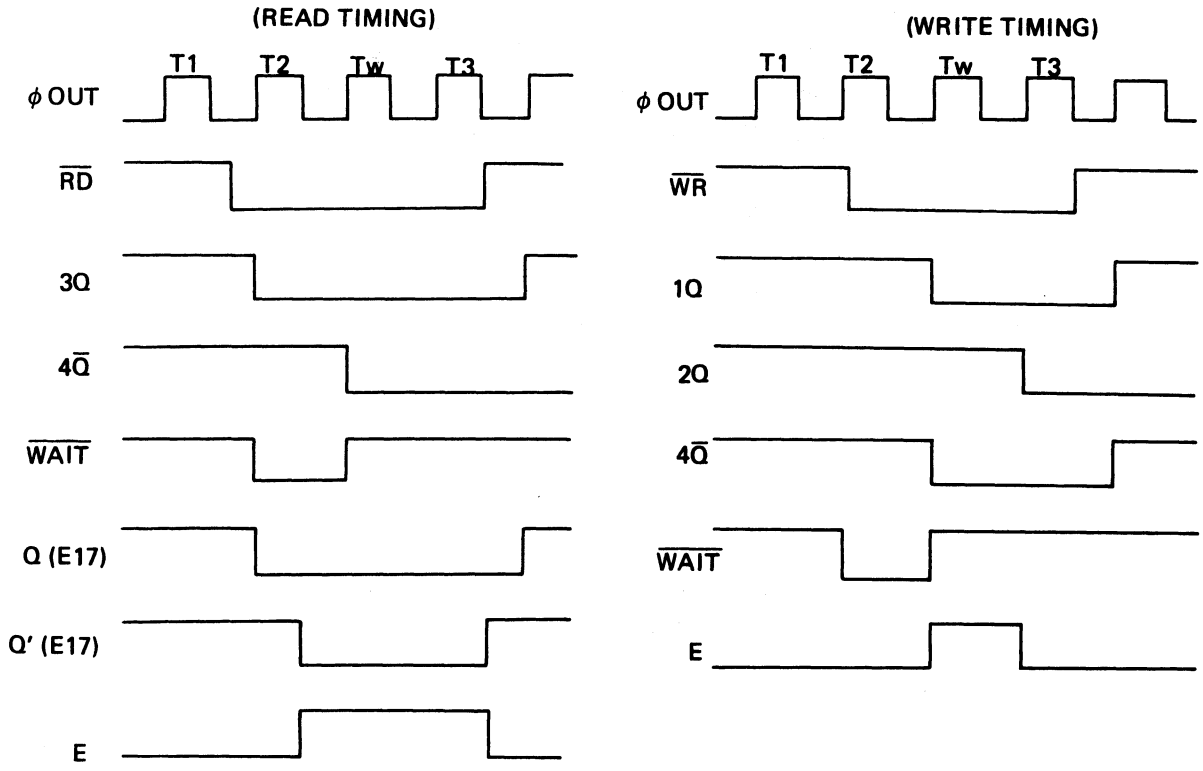


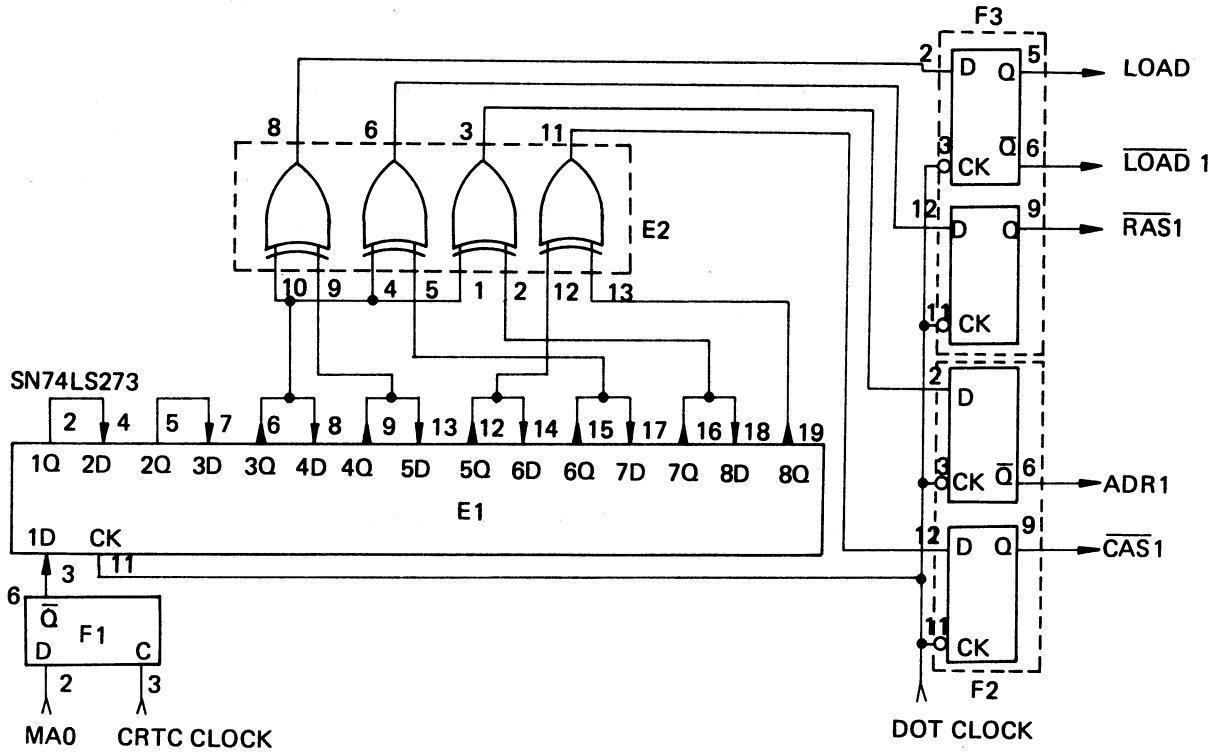
Fig. 8-10 READ/WRITE TIME CHART

8-22. TIMING GENERATE CIRCUIT (I) :

The following circuit genrates video RAM access signals $\overline{RASI}$ and $\overline{CASI}$, $\overline{LOAD}$ signal for P/S change-over shift register and selects signal for the address selector based on the address signal (MA0) from the CRT controller D12.

LOCATION: SUB P.C.B. (G205-2)

40 CHARACTER MODE : CRTC CLOCK-998.4KHz, DOT CLOCK-7.9872MHz
80 CHARACTER MODE : CRTC CLOCK-1.9968MHz, DOT CLOCK-15.9744MHz



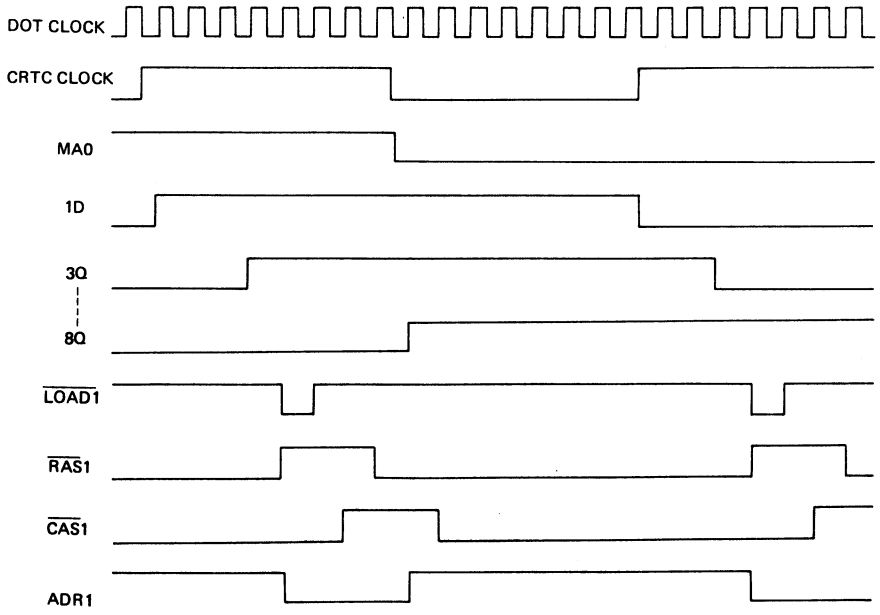
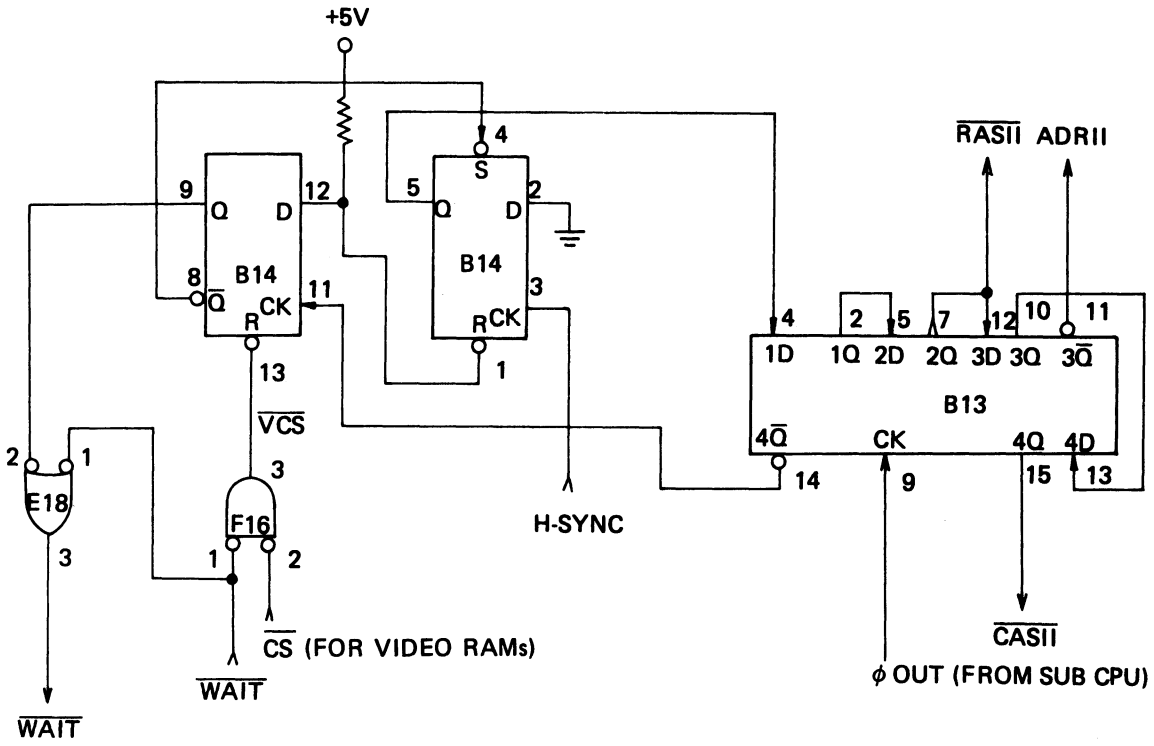


Fig. 8-11 TIMING GENERATE CIRCUIT (I)

8-23. TIMING GENERATE CIRCUIT (II) :

The following circuit generates timing signals which are necessary for the sub CPU to read or write data in the video RAMs.
The circuit has two main functions. One is to cause the sub CPU to become in wait condition until the horizontal synchronizing period comes, and the other is to generate access signals for the RAMs such as $\overline{\text{RASII}}$, ADRII and $\overline{\text{CASII}}$.

LOCATION: SUB P.C.B. (G205-2)



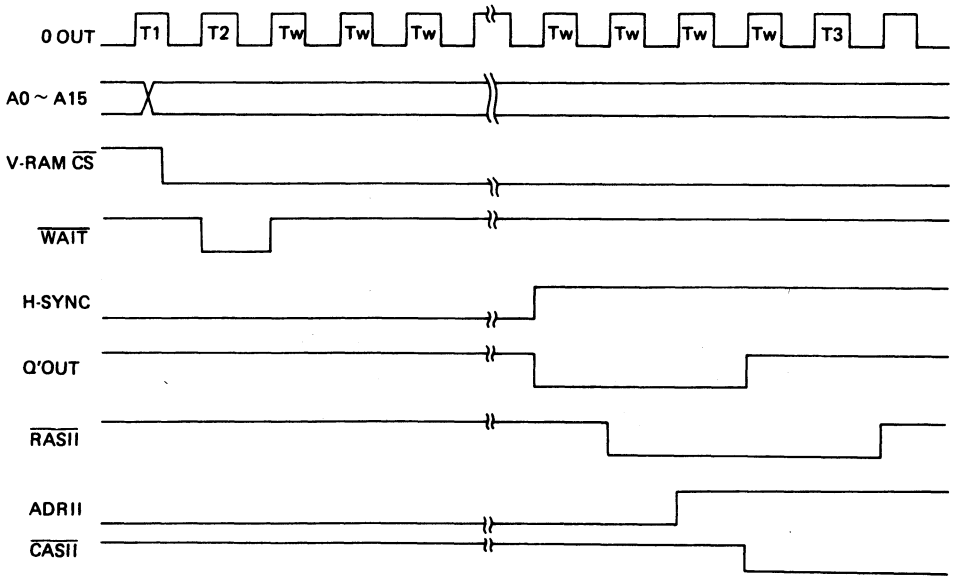


Fig. 8-12 TIMING CHART

8-24. DISPLAY (CRT) SYNCHRONIZING SIGNALS :

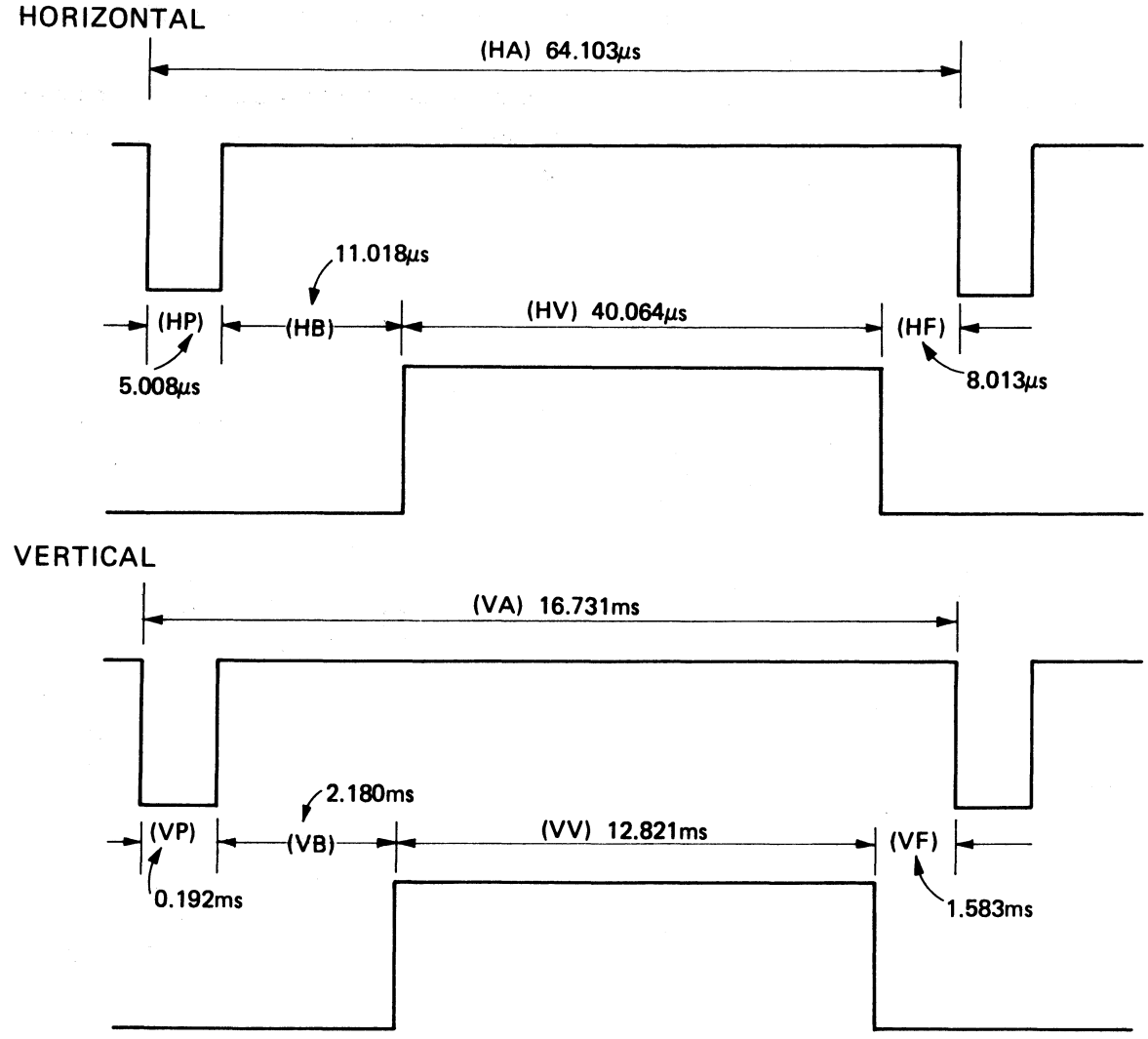


Fig. 8-13 DISPLAY SYNCHRONIZING SIGNAL

Abbreviation:
- HA – HORIZONTAL SCAN PERIOD
- HV – HORIZONTAL DISPLAY PERIOD
- HP – HORIZONTAL SYNCHRONIZING PULSE WIDTH
- HF – HORIZONTAL FRONT PORCH PERIOD
- HB – HORIZONTAL BACK PORCH PERIOD

- VA – VERTICAL SCAN PERIOD
- VV – VERTICAL DISPLAY PERIOD
- VP – VERTICAL SYNCHRONIZING PULSE WIDTH
- VF – VERTICAL FRONT PORCH PERIOD
- VB – VERTICAL BACK PORCH PERIOD

8-25. POWER SUPPLY CIRCUIT :

The power supply block consists of three small circuit boards (S1, S2 and S3) and power transformer.

These blocks produce +5V, +12V and −12V DC power voltages necessary to turn on devices in this system unit and PWD signal. AC input voltage can be selected from 100 to 240V by setting the AC voltage selector switch.

(In some units, the AC voltage selector may not be installed depending on country destination.)

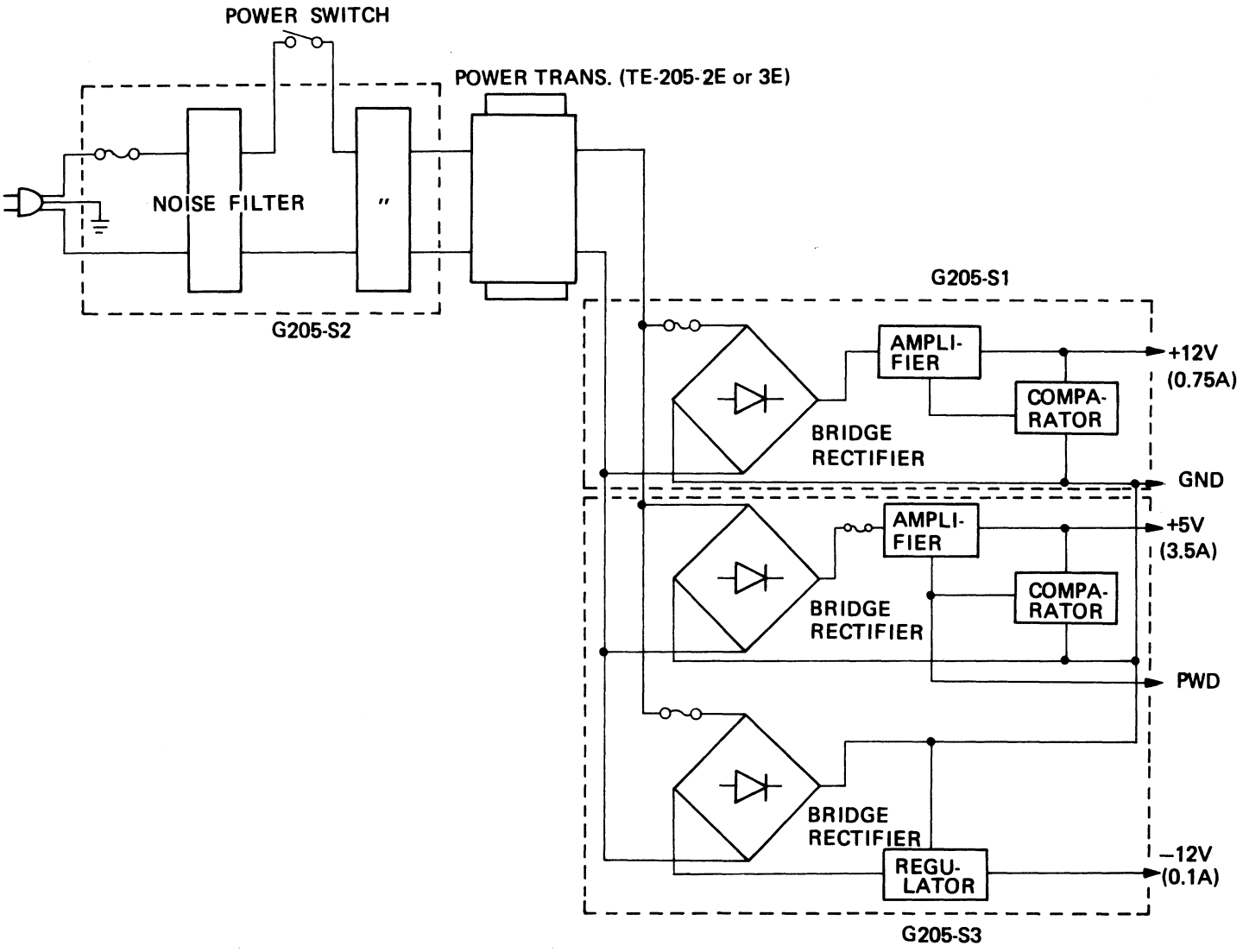
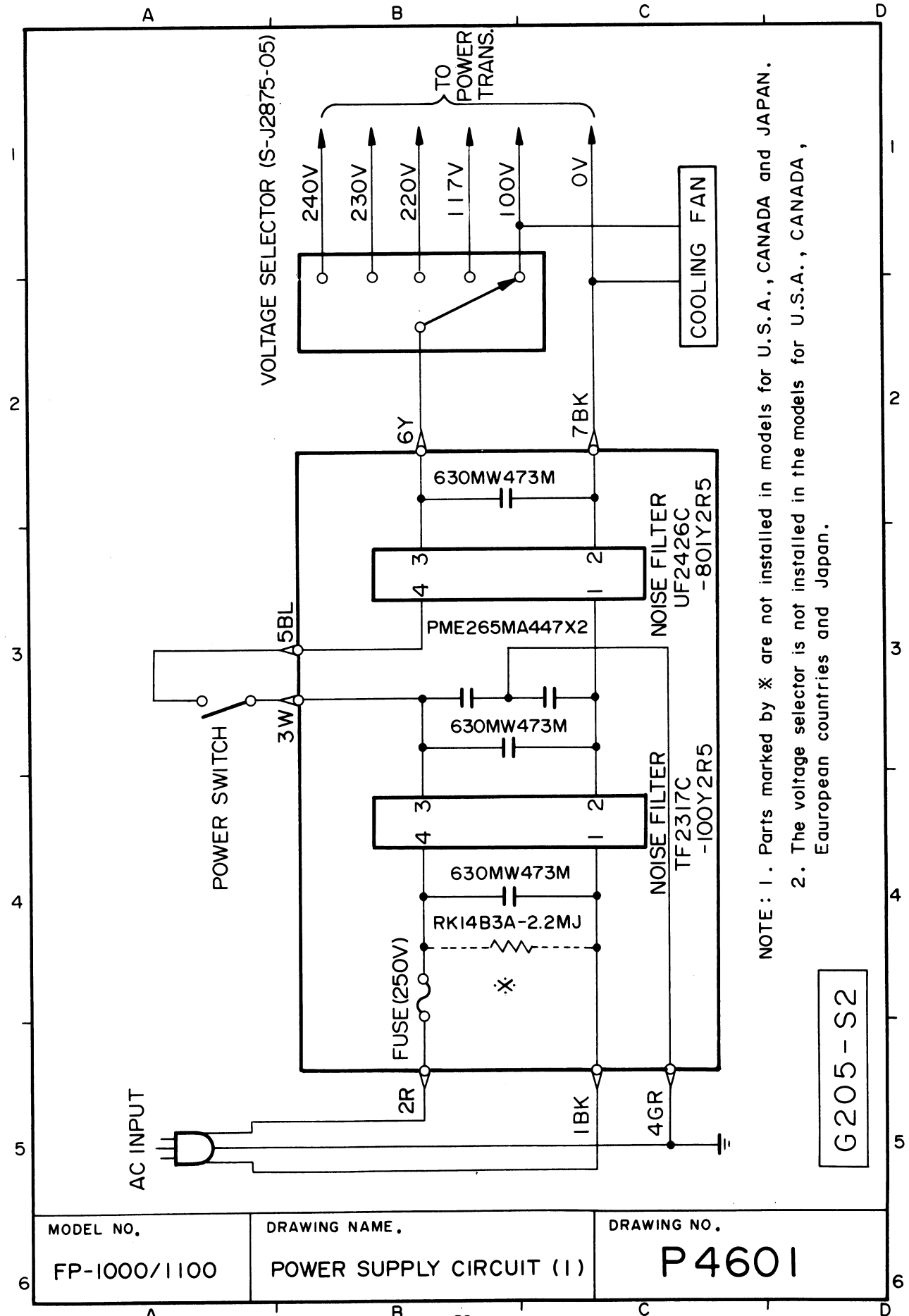


Fig. 8-14 POWER SUPPLY BLOCK DIAGRAM

POWER VOLTAGE ADJUSTMENT

POWER VOLTAGE	ADJUSTING V.R.	CHECK PIN LOCATION	READ VALUE
+12V	+12V	MAIN P.C.B.	+11.4 ~ +12.6V
+ 5V	+ 5V	MAIN P.C.B.	+4.75 ~ +5.25V
−12V	−	G205-S3	−10.8 ~ −13.2V

9. CIRCUIT DIAGRAM



COLOR VIDEO SIGNALS

GREEN VIDEO SIGNAL

TO KEY BOARD

FROM POWER SUPPLY

TO/FROM KEY BOARD

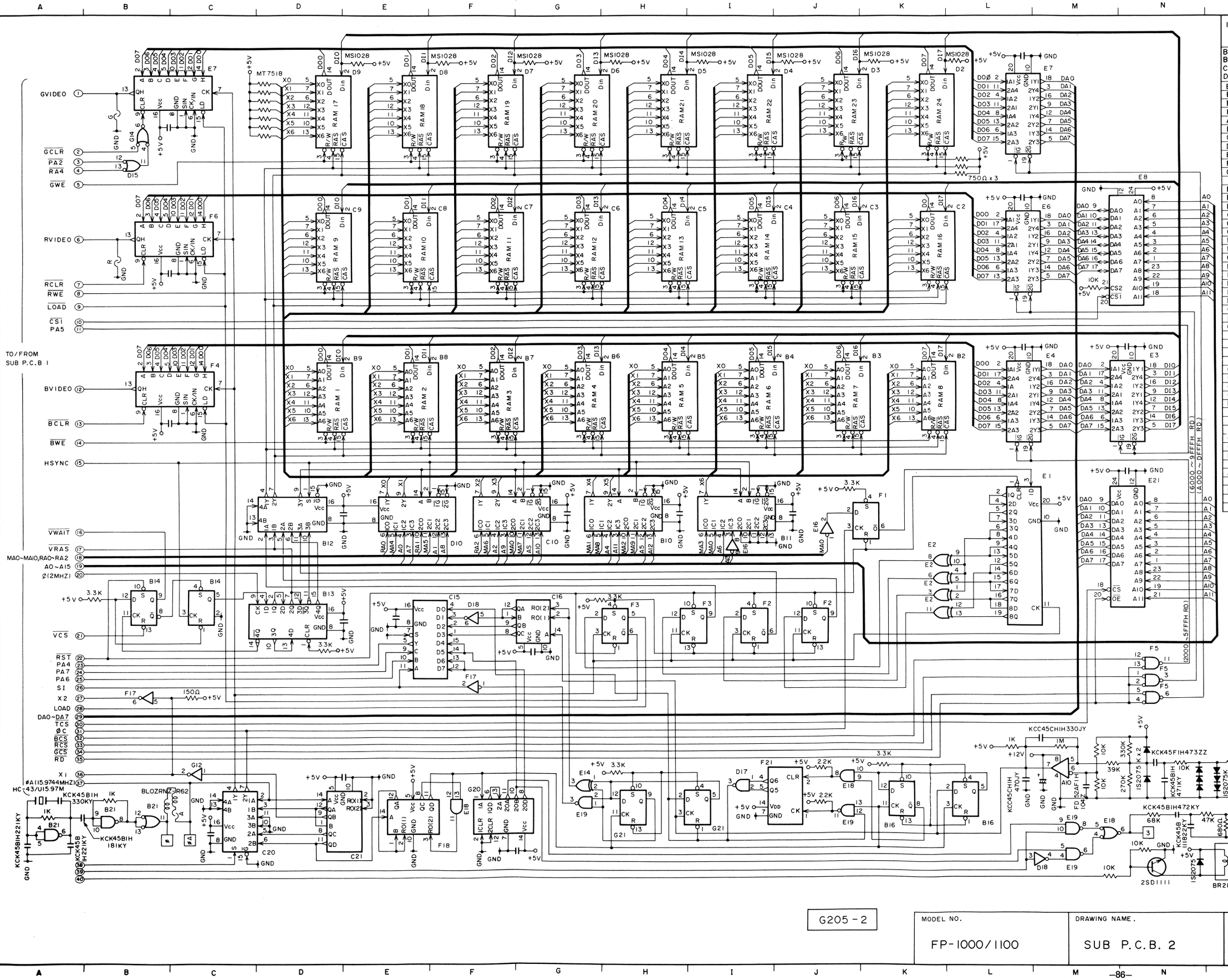
TO/FROM PRINTER

TO/FROM SUB P.C.B. 2

TO/FROM MAIN P.C.B.

MODEL NO.	DRAWING NAME.	DRAWING NO.
FP-1000/1100	SUB P.C.B. 1	P1125 ⑥

G205 - 2



IC POSITION IC	INTEGRATED CIRCUIT IC
B2,B3,B4,B5,B6,B7 B8,B9,C2,C3,C4,C5 C6,C7,C8,C9,D2,D3 D4,D5,D6,D7,D8,D9	HM4716AP-2
E8	HN46332PA40
E21	HN462732
E12	μPD7801G-101
F21	TC4024BP
A10	LM393P
B21.D15.D17.E19	SN74LS00N
G2	SN74LS02N
D18, E16, F17	SN74LS04N
E18, G1, G14, F14	SN74LS08N
F15	SN74LS11N
G12	SN7416N
F1, F2, F3	SN74S74N
B14.B16.G21.C14.F17	SN74LS74AN
E2.E14	SN74LS86N
C16.F18	SN74LS93AN
C21	SN7493AN
C15	SN74LS151
B10.B11.C10.D10	SN74LS153N
B12	SN74LS157N
C20	SN74157N
F4. F6. F7	SN74LS166AN
B13	SN74LS175N
E3	SN74LS240N
E4. E6. E7.	SN74LS244N
E1	SN74LS273N
G20	SN74LS393N
D12	HD46505SP
C18. C19	TC40H368BP
G11	SN74LS10N
G15	SN7416N
G5. G6	SN7417N
G3. G13	SN74LS27N
E15. F5. F16 G7	SN74LS32N
G9. G10	SN74LS145N
G8	SN74LS157N
B17. C13	SN74LS174N
D13. D14. D16	SN74LS175N
A13	SN74LS244N
A12	SN74LS273N
F20. G4	SN74LS367AN

G205-2

MODEL NO.	DRAWING NAME.	DRAWING NO.
FP-1000/1100	SUB P.C.B. 2	P1126 ⑦

IC POSITION	INTEGRATED CIRCUIT
C, D5	μPD780C-1
A1, B1, A2, B2, A3 B3, A4, B4	HM4864P-2
C1	HN46332PA
C3	HN61256PA5I
C14, C15	SN74LS00N
C16	SN74LS02N
C7, B9, B10, B11 B14	SN74LS04N
B12	SN74LS30N
B15, D15, D16, B16	SN74LS32N
C12, A17, B17, C17	SN74S74AN
C13	SN74LS139N
D14	SN74LS148N
A5, B5	SN74LS157N
C10	SN74LS244N
C9, D12	SN74LS273N
C4, B6, B7, B8, B13, D13	SN74LS367AN
C8	SN74LS174N
A16	SN7417N
C11	SN7493AN

I/O SLOTS

to SP-1

TO/FROM SUB P.C.B.

G205-1

MODEL NO.	DRAWING NAME.	DRAWING NO.
FP-1000/1100	MAIN P.C.B.	P1124 ⑤

KC3
KC2
KC1
KC0
FD52AF1H 104Z
SN74159
+5V 1K x3
+5V
0V
47µF10WV
GND
5V
VCC
GND
G1
G2
KCK45B1H 103KY x3
SD161201
BUZZER
TLR-114A
SHIFT LOCK
220Ω
1K
CAPS
KI 1
KI 2
KI 3
KI 4
KI 5
KI 6
KI 7
KI 8

:	;	L	K	J	H	G	F	D	S	A	SHIFT	SHIFT
ø	9	8	7	6	5	4	3	2	1	ESC		CTRL
^	RETURN	7"	4"	5"	8"	9"	6"	3"	+"	−"		GRAPH
@	P	0	I	U	Y	T	R	E	W	Q		CAPS
{	/	·	,	M	N	B	V	C	X	Z		
¥	RUBOUT	←"	CLSHOME"	↑"	↓"	INS"	→"	DEL"	/"	X"		
−	[	]	1"	2"	ø"	SPACE	øøø"	·"	,"	ENTER"		
STOP/CONT	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0		BREAK

IS2075K x 5

+5V
FD52AF1H104Z
SN7438N
GND

PFØ

G205-E4

MODEL NO.	DRAWING NAME.	DRAWING NO.
FP-1000/1100	KEYBOARD	P2253

MODEL NO.	DRAWING NAME.	DRAWING NO.
FP-1000/1100	POWER SUPPLY CIRCUIT (2)	P3609

10. TEST PROGRAM

A function test program is available for the FP-1000/1100 system unit by installing two check ROMs, one in the sub CPU P.C.B. and the other in the EP-ROM pack (FP-1031). This program enables a diagnosis of all the functions of the system unit except the power supply circuit, and other functions in the various peripheral devices.

Features are;
- 10-1, INTERRUPT AND SUM CHECK
- 10-2, VIDEO RAM AND DISPLAY CIRCUIT CHECK
- 10-3, VIDEO BIT REVERSE CHECK
- 10-4, MODE SELECTOR SWITCH CHECK
- 10-5, KEY ENTRY CHECK
- 10-6, LED CHECK
- 10-7, BUZZER CHECK
- 10-8, RS-232C INTERFACE CHECK
- 10-9, EP-ROM PACK CHECK
- 10-10, CMOS-RAM PACK CHECK
- 10-11, D-RAM CHECK
- 10-12, I/O INTERFACE CHECK
- 10-13, PRINTER INTERFACE CHECK
- 10-14, FDD CHECK

Before starting the program . . .

1) Remove the ROM in socket A of the EP-ROM pack (FP-1031) and install one of the two test ROMs (No. M1.6) in the socket as shown in Fig. 10-1.
It is not necessary to change the pad conditions of "A" and "B" on the circuit P.C.B. if pad "A" is short and pad "B" is open. If not, set these pads to A-short and B-open condition. Also, it is not necessary to remove the other three ROMs in socket B, C, and D.

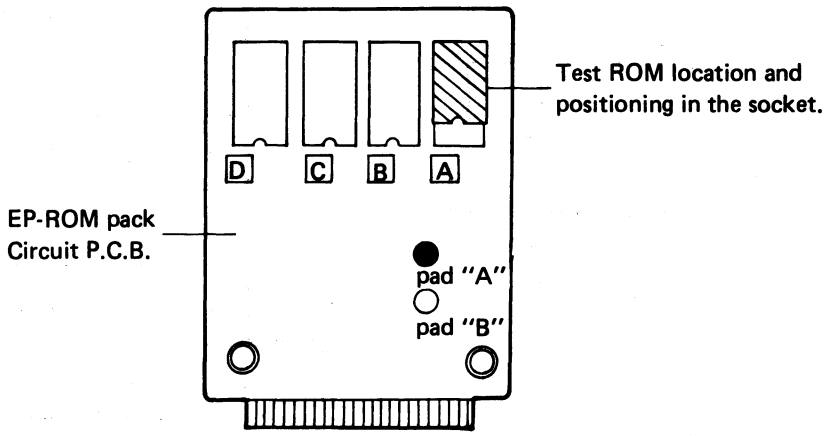


Fig. 10-1 EP-ROM PACK CIRCUIT BOARD

2) Remove the upper housing of the system unit so that the IC socket showing "HN462732G" can be located on the left side of the sub CPU P.C.B. as shown in Fig. 10-2.

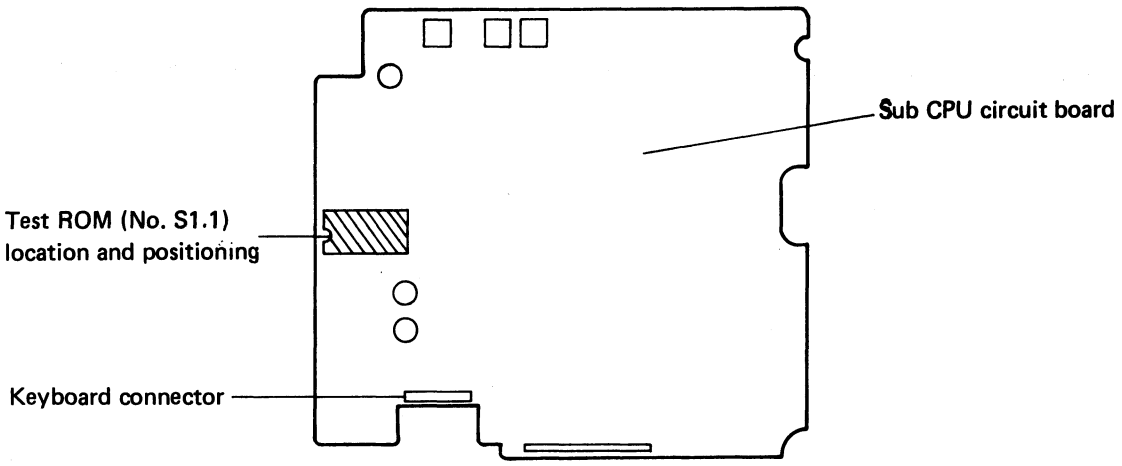


Fig. 10-2 SUB CPU P.C.B.

3) Remove the ROM from that socket and install the other test ROM (No. S1.1) in it. It is not necessary to make conditional change of any pads on the sub CPU P.C.B. nor on the main CPU P.C.B.
   Be sure to install the ROM in the right direction as shown in Fig. 10-2.
4) Install the EP-ROM pack in slot No. 1 of the system unit.
5) Install a peripheral device in slot No. 2 if that device is to be diagnosed.
   Otherwise no device installation is necessary in the slot.
6) Connect the color display unit (FP-1003) or the green display unit (FP-1001) to the monitor execution of the program and its diagnostic result.

Function and numeral keys

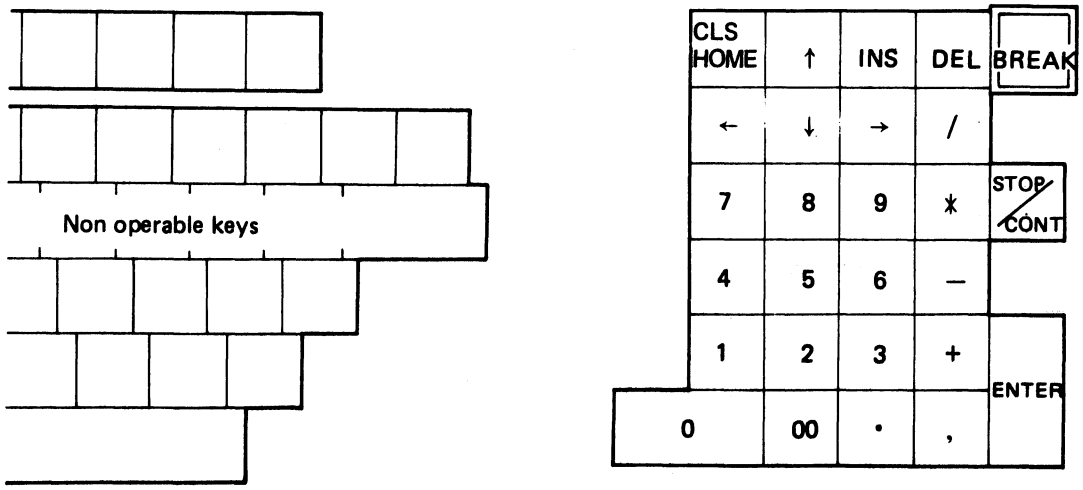


Fig. 10-3 TEST PROGRAM ENTRY KEYS

Numeral entry keys;

[0] – [9] : Used to enter numeral entry from 0 to 9.

[←] : Used to enter "A" in hexadecimal.

[↓] : Used to enter "B" in hexadecimal.

[→] : Used to enter "C" in hexadecimal.

[CLS HOME] : Used to enter "D" in hexadecimal.

[↑] : Used to enter "E" in hexadecimal.

[INS] : Used to enter "F" in hexadecimal.

Function entry keys;

[DEL] :
- Used to eliminate entry indication on the screen before depressing the "ENTER" key.
- Used to clear the screen only if the program is waiting further command in the execution of the command and the cursor is positioned on the 3rd line or below.

[BREAK] :
- Used to break execution of command.
  However, it cannot break continuation of execution in some commands.
  Refer to the "CONTROL BIT REFERENCE TABLE" for details.

[ENTER] :
- Used to start entered command
- Used to re-execute command when in command waiting condition after the previous command is completed.
- Used to continue the command after the command execution has stopped for another command to be executed in the command execution flow.
- Used to shift displayed data on the screen to a specified register when in waiting condition for new data to be entered.

[STOP/CONT] :
- Used to stop and start blinking operation of the cursor. During its stationary condition, execution of command stops if data error occurs, then waits for the "ENTER" or the "BREAK" key.

Keys other than the above-mentioned are not operable as long as the two test ROMs are installed in the system unit and the EP-ROM pack.
Removing them can release the test mode and return to normal operating mode.

MODE INDICATION REFERENCE TABLE

CODE	DESCRIPTION
CMD	Entered program command code is not used in this program.
NFR	Entered program command code is not allowed to be repeated.
NFP	Entered program command code is not allowed to be used when other command is in execution.
NFM	Entered program command code is not allowed to be entered manually.
CLS	Command control bit "S" is being closed.
CLN	Command control bit "N" is being closed.
REP	Repeat counter has no data in register.
PRG	Entered program number has not been programmed in this test program.
ADR	Entered address number is not proper.
OVP	Program has passed over valid area.
MOD	Entered mode is not used in this test program.
BKP	Program execution flow has passed through the break point in the program.
OVT	Timer has finished counting.
DVC	Entered device code is not proper to designate the device.
BKK	"BREAK" key is used to break a program execution.
PKW	A FDD write/read program command code has been entered.
PTT	Printer interface check program command code has been entered.
CPD	Result of I/O interface check.
LPA	Light pen error address.
RVM	D-RAM program command code has been entered.
PKC	CMOS-RAM pack check program command code has been entered.
RSS	Error status of RS-232C interface port.
PWD	Error write/read data after RS-232C interface check.
PKR	RS-232C interface check program command code has been entered.
BUZ	Buzzer check program command code has been entered.
LED	LED check program command code has been entered.
KEY	Key entry check program command code has been entered.
SWD	Mode selector switch check program command code has been entered.
RVD	Result of video bit reverse check.
RVV	Video bit reverse check has been entered.
CTN	The program command code to open command control bit "N" has been entered.
INT	Result of interrupt check.
SUM	Result of sum check.
RWS	Result of video RAM and display circuit check.

10-1. INTERRUPT AND SUM CHECK

As soon as the power switch of the system unit is turned on, interrupts to sub CPU and to main CPU checks and sum check of ROMs are automatically executed.
When an error occurs, result is displayed on the screen after displaying check ROM version number.

- SUB CPU INTERRUPT CHECK

This mode checks outside interrupts (to sub CPU) of INT0, INT1 and INT2, and internal interrupts of INTS and INTT. Then it indicates the results in the following manner.

ERROR DISPLAY MODE

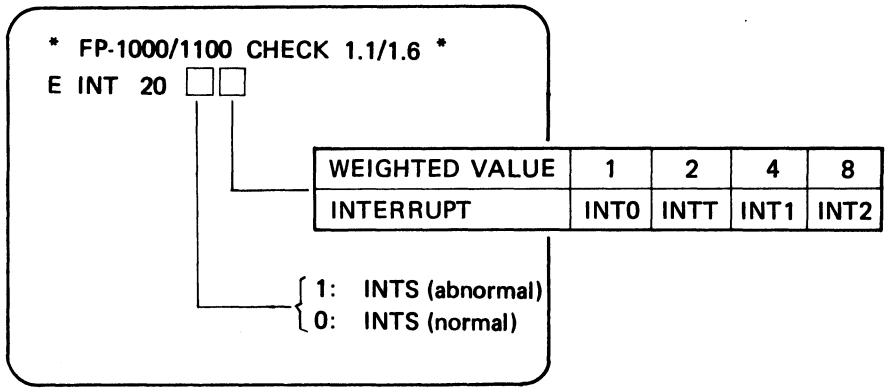


Fig. 10-4

- SUM CHECK (1)

This mode checks three ROMs on the sub P.C.B. and indicates a ROM number and sum total if its sum total differs from the sum total of the check ROM.

ERROR DISPLAY MODE

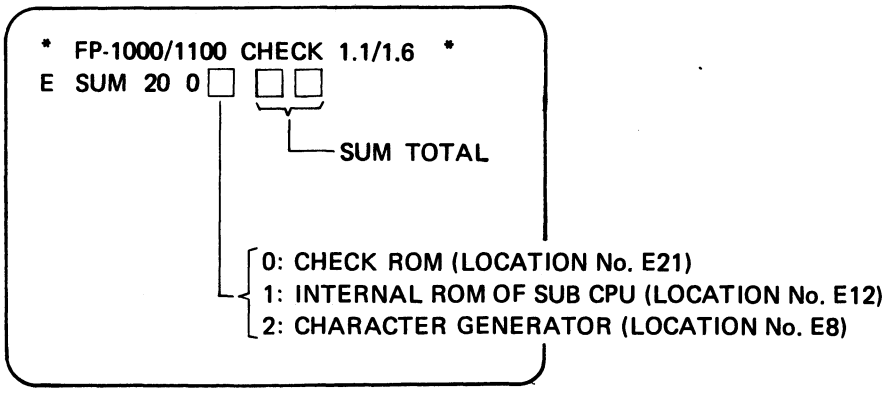


Fig. 10-5

- MAIN CPU INTERRUPT CHECK

This mode checks interrupts (to main CPU) of $\overline{\text{INTA}}$, $\overline{\text{INTB}}$, $\overline{\text{INTC}}$, $\overline{\text{INTD}}$ and $\overline{\text{PC3}}$, and input/output status of IC No. D14 (SN74LS148) on the main P.C.B.
Then it indicates the results in the following manner if an error occurs.

ERROR DISPLAY MODE

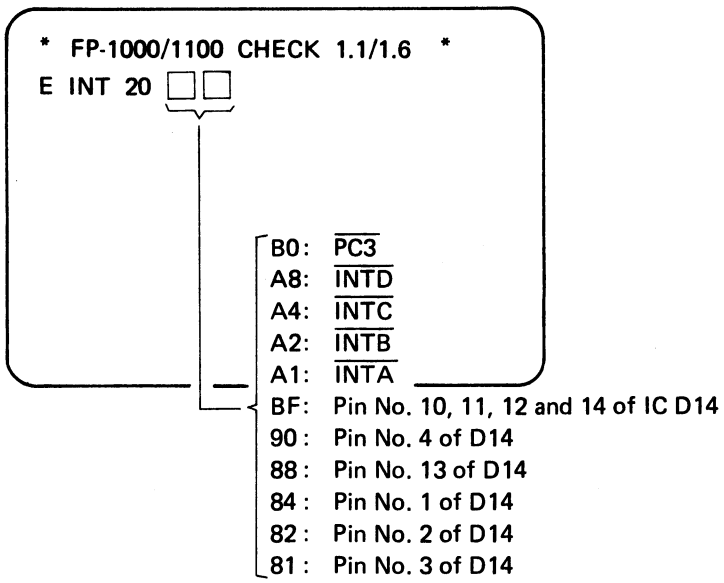


Fig. 10-6

- SUM CHECK (2)

This mode checks three ROMs on the main P.C.B. and indicates a ROM number and sum total if its sum total differs from the sum total of the check ROM.

ERROR DISPLAY MODE

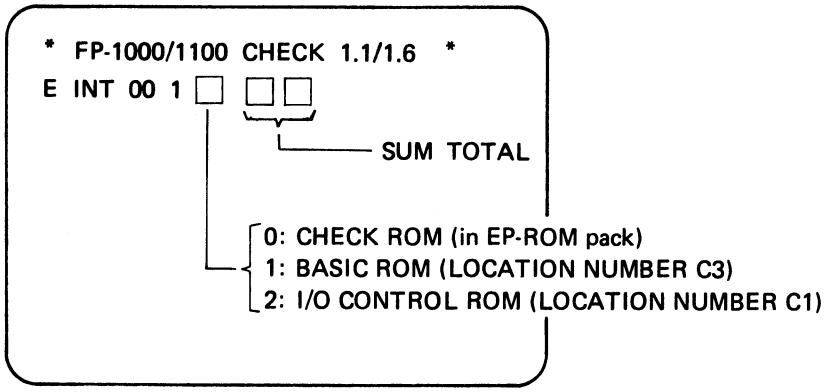


Fig. 10-7

10-2. VIDEO RAM AND DISPLAY CIRCUIT CHECK

This program operation performs video RAM and display circuit (in FP-1000 and FP-1100) checks and indicates error status which separates into blue, red and green if a hard error exists.

Enter 22 [ ] [ENTER]

- 0 For FP-1000 (green)
- 1 For FP-1100 (color)

If the video RAM ICs and the display circuit are normal, the following six display modes are consecutively indicated in the order of ①–②–③–④–⑤–⑥.

As the screen shows the display modes, note that the cursor size will be one half. If any hard error condition exists, an error status will be displayed as soon as indications of the six display modes are completed.

FP-1100

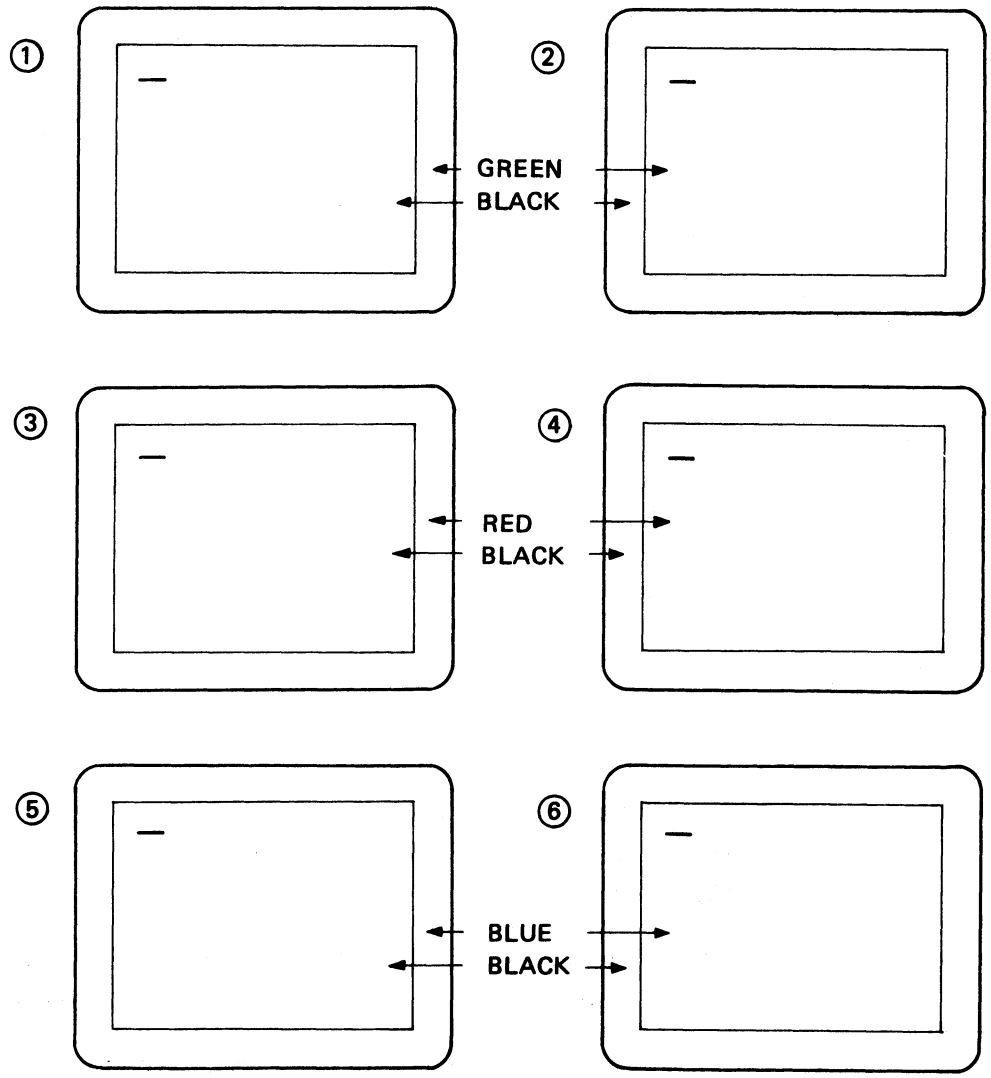


Fig. 10-8

EXPLANATION OF ERROR STATUS

Example: There is a defective video RAM IC in red video memory of FP-1100 and the screen indicates an error status as follows after completion of the six display mode indications.

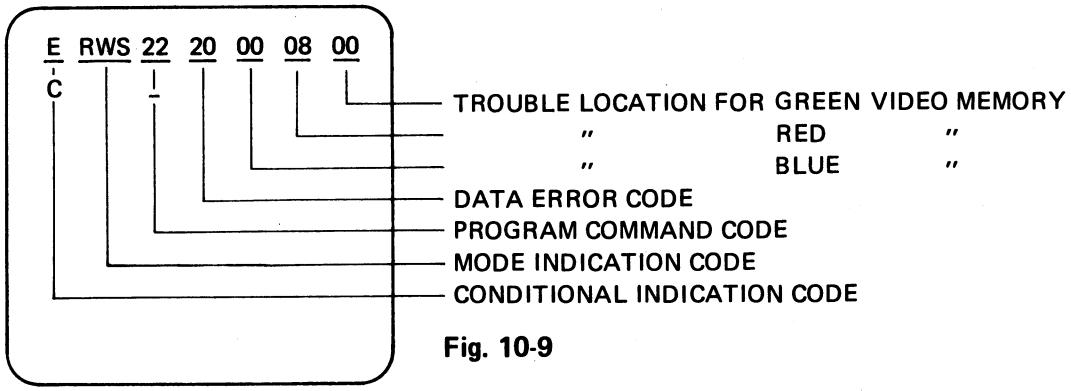
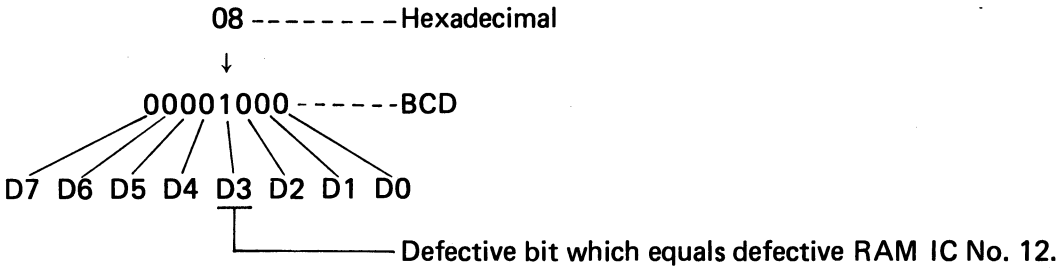


Fig. 10-9

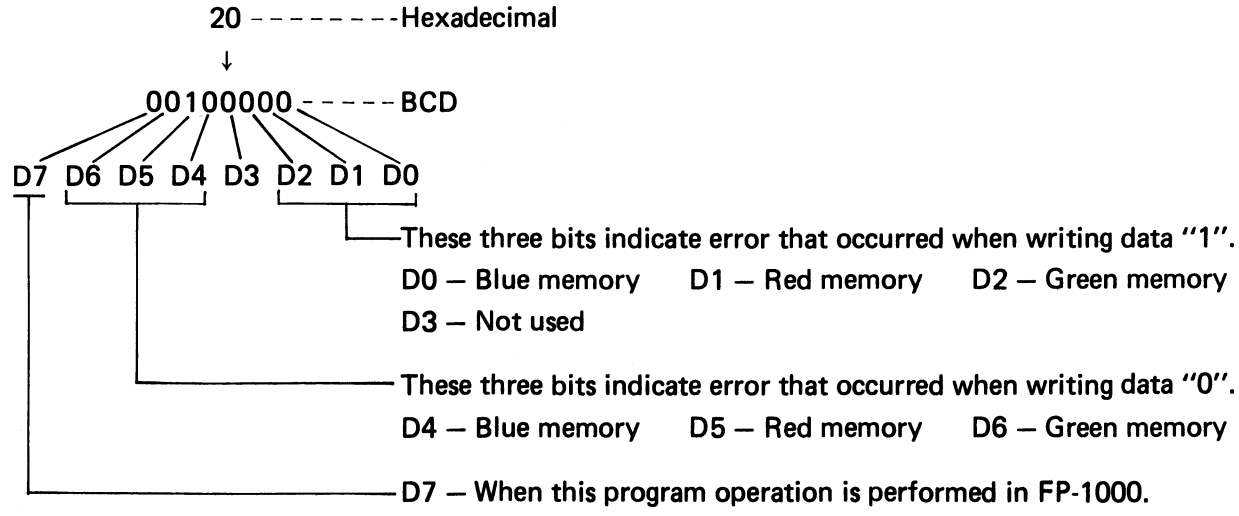
- TROUBLE LOCATION

Two digits for each video memory indicate incorrect bit(s) in hexadecimal numeral which can be converted into BCD as shown below.



- DATA ERROR CODE

These two digits can indicate if error occurred when writing data "1" or "0" in the RAMs, and in what video RAM memory such as green, red or blue.



10-3. VIDEO BIT REVERSE CHECK

This program operation performs video RAM memory check by writing data and reads that reversed data (bit). And also it can indicate address where trouble occurs and, write data and incorrect read data on the screen.

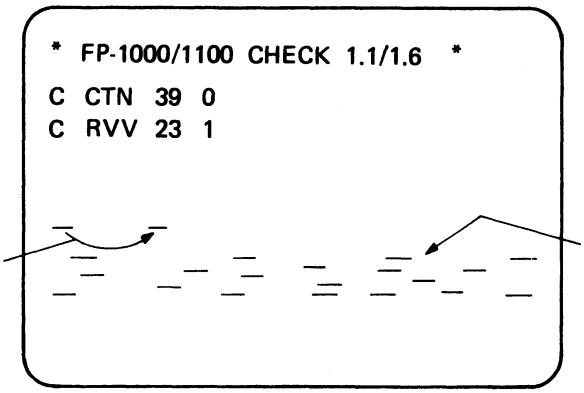
By analyzing the address and incorrect read data, the trouble location can be traced easily.

Enter 390 [ENTER]

Enter 23 [ ] [ENTER]

- 1 For FP-1100 (video RAM address 2000H-DFFFH)
- 0 For FP-1000 (video RAM address 2000H-5FFFH)

This display mode shows no error in the video RAM memory circuit.



The cursor moves here about 42 seconds later from the time when [ENTER] key is depressed.

Then an entry can be made. Otherwise, the entire memory contents of Red video are dumped (until 9FFFH).

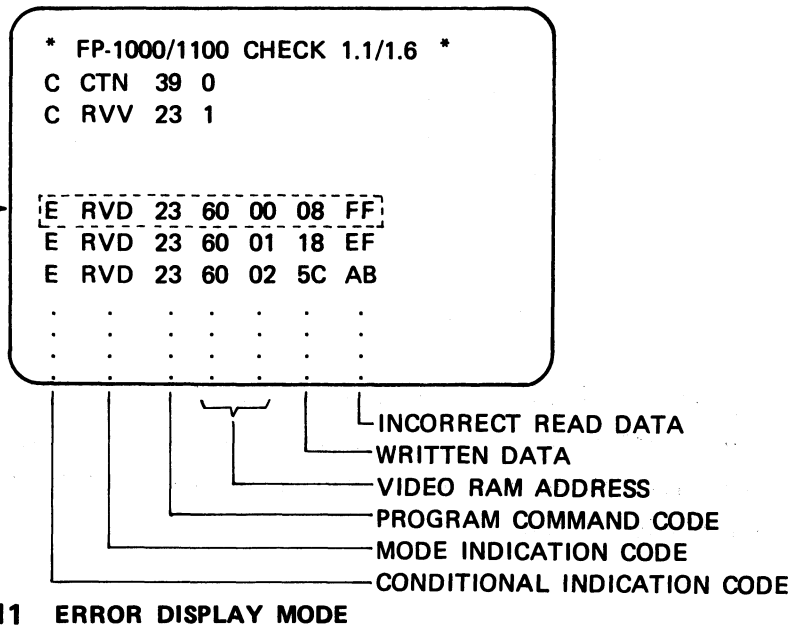
Flickering thin-short lines move down from top of the screen, then disappear.

Fig. 10-10

Example: Defective RAM IC in the video circuit (FP-1100).
(This example is made by removing RAM12 in the sub PCB.)

Enter 390 [ENTER]

Enter 231 [ENTER]



Error begins from this address. As soon as first address of an error appears on the screen, stop the memory dumping by depressing the [BREAK] key.

Fig. 10-11 ERROR DISPLAY MODE

ANALYSIS OF THE TROUBLE

Error address "E RVD 23 60 00 08 FF"

Reversed data (bit) of written data "08" is presented as follows.

① 08 ---------Hexadecimal (written data)

00001000------BCD

↓

11110111------ Reversed BCD

↓

F7---------Hexadecimal (read data)

As shown, if the RAM IC is normal, reversed data (bit) of written data "08" should be "F7" instead "FF" and indicated next to the written data on the screen.

② FF--------Hexadecimal

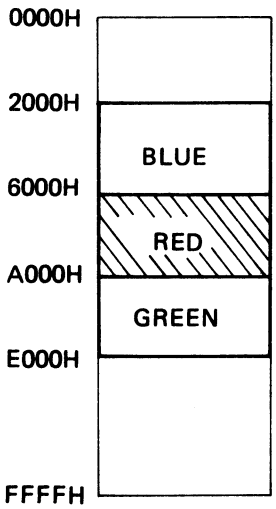
↓

1111[1]111------BCD

→This bit (D3) should be "0" instead of "1".

The next thing to be analyzed is the address "6000H" showing on the screen.
First of all, look at the memory map below and find where the address is allocated.

③



Address "6000H" can present 24 Kbyte.

$(6 \times 16^3 + 0 \times 16^2 + 0 \times 16^1 + 0 \times 16^0) \div 1024 = 24K$

By indicating in the above memory map, address "6000H" is the forefront address of Red video RAM memory. From the result of the address analysis No. 3, it is obvious that the defective RAM IC is one of the Red video RAMs (RAM9 ~ RAM 16. Refer to the circuit diagram No. P1126).

Since a bit of video data is written in each RAM IC (D0 → RAM 9, D1 → RAM 10 . . . D7 → RAM 16), in this given example D3 bit is found to be abnormal in analysis No. 2 shown in the previous page. That is, RAM12 is the cause of this trouble because D3 bit is written in RAM IC.

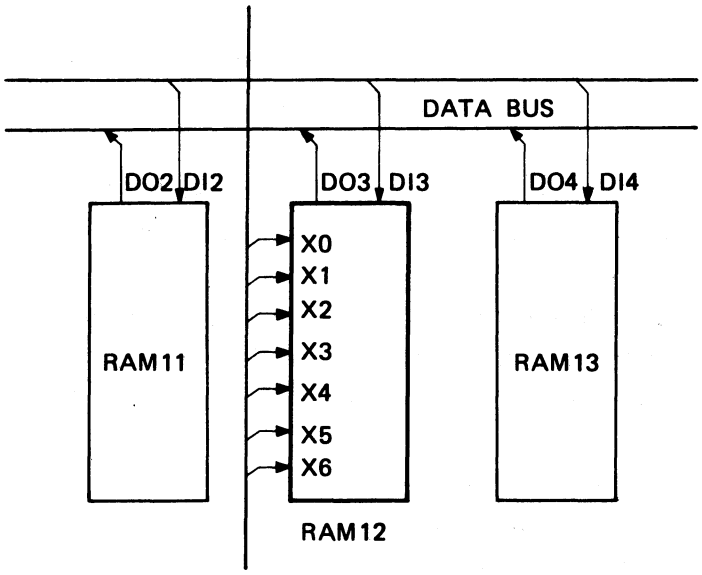


Fig. 10-12 ADDRESS BUS

10-4. MODE SELECTOR SWITCH CHECK

This program operation can indicate on-off status of the mode selector switches locating under the bottom housing in two digit hexadecimal numerals resulting from the OR adding method. The result is used to detect the functional condition for the switches and its control circuit.

Enter 34 [ENTER] (To end this mode, depress the [BREAK] key)

	ON	OFF
SW 1	01	00
SW 2	02	00
SW 3	04	00
SW 4	08	00
SW 5	10	00
SW 6	20	00

Added result is indicated here

```
* FP-1000/1100 CHECK 1.1/1.6 *
C SWD 34
C SWD 34 [ ] –
```

Fig. 10-13

Example: Suppose SW3 and SW4 switches are ON right now, the result will be "0C" on the screen.

Confirm that the result on the screen is changed when one of the six switches is turned on or turned off.

10-5. KEY ENTRY CHECK

This program operation is used to check entry of keys in JIS mode and ASCII mode.

Enter 36 [ ] [ENTER]

- 1 JIS mode (Japanese specification)
- 0 ASCII mode

Then enter [PF0] [PF1] .... ['] continuously. Each time a key entry is made, that key symbol on the key top is indicated on the screen confirming that the key entry has been performed.
However, some key entries indicate different symbols from its own as listed below.
In this program operation mode, entry of all the program entry keys become inoperative until the mode is released by depressing the [BREAK] key.

```
* FP-1000/1100 CHECK 1.1/1.6 *
C KEY 36 0
'P0' 'P1' 'P2' .................
```

Fig. 10-14

SYMBOL ON KEY TOP	ESC	CTRL	CAPS	SHIFT	RETURN	GRAPH	00
INDICATION	ES	CT	CA	SH	RE	GR	20

EXCEPTIONAL INDICATION

10-6. LED CHECK

This program operation performs on-off check for the two LEDs (CAPS and SHIFT/LOCK) on the keyboard.

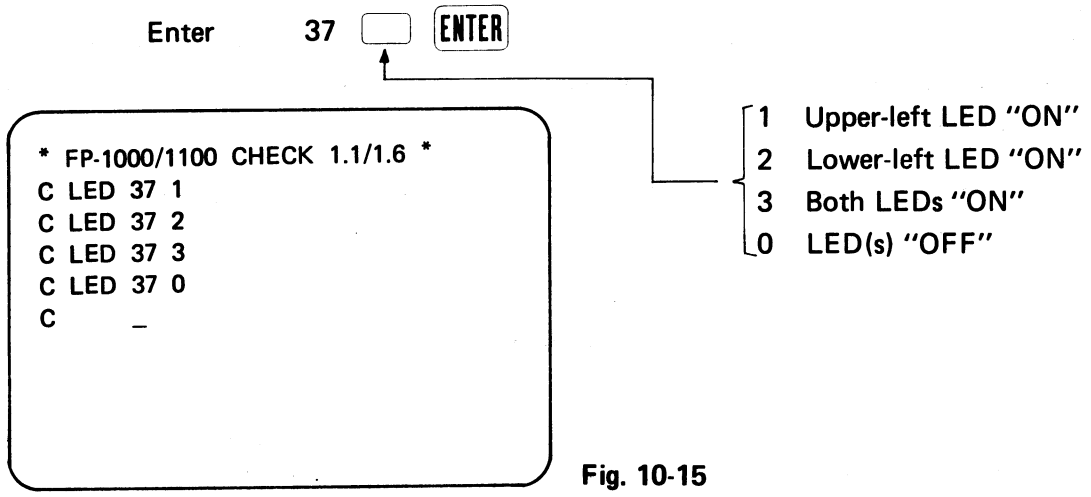
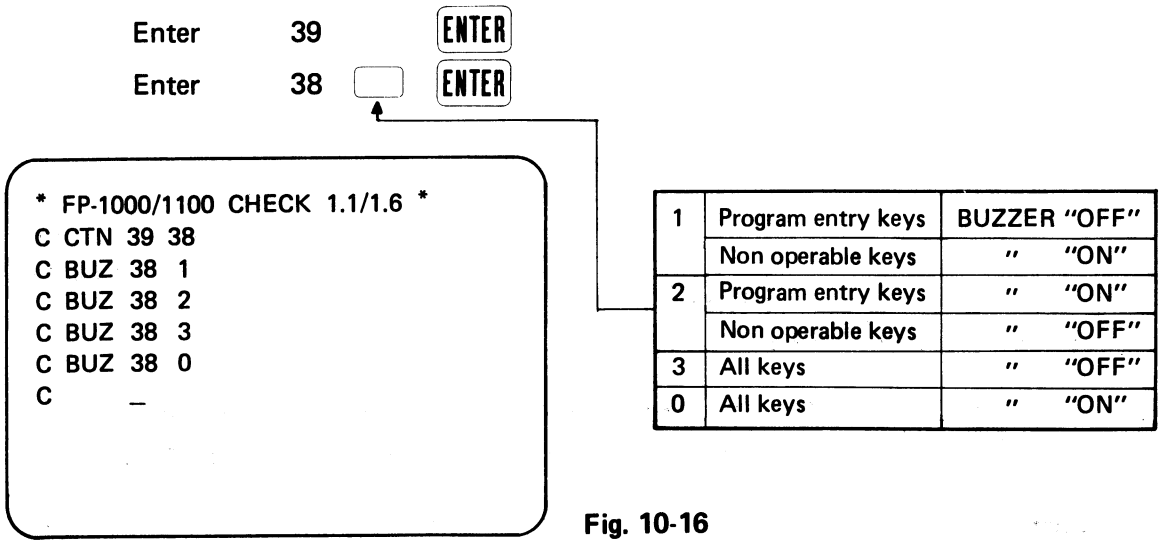


Fig. 10-15

10-7. BUZZER CHECK

This program operation performs on-off check for the buzzer (that sounds when a key entry is made) and its control circuit. It can be checked in the following four modes.



1	Program entry keys	BUZZER "OFF"
	Non operable keys	" "ON"
2	Program entry keys	" "ON"
	Non operable keys	" "OFF"
3	All keys	" "OFF"
0	All keys	" "ON"

Fig. 10-16

After a mode selection is made, make sure whether the buzzer sounds or not in accordance with the mode specification when depressing each key in the group of the program entry keys or the non operable keys.

Note: Program entry keys – "1", "2", "3", "4", "5", "6", "7", "8", "9", "0" "←", "→", " ↑ ", " ↓ ", "CLS/HOME", "INS", "DEL", "STOP/CONT" and "ENTER" keys.

Non operable keys – All other keys except the above.

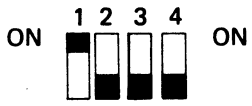
10-8. RS-232C INTERFACE CHECK

This program operation checks RS-232C interface function including the FP-1035RS pack.

- RS-232C INTERFACE CHECK

In this check mode, data generated by the ROMs is transmitted to read data buffer in the controller. Then the data sent through port "TxD" and returned from "RxD" is compared with the original data.

1) Set dip switches of the FP-1035RS pack as follows (this is to be repeated in the following checks).



2) Install the RS-232C function check connector on the output connector of the pack.
3) Install that pack in slot No. 2 (this is to be repeated in the following checks).
4) Enter 1211 ENTER

ERROR DISPLAY MODE

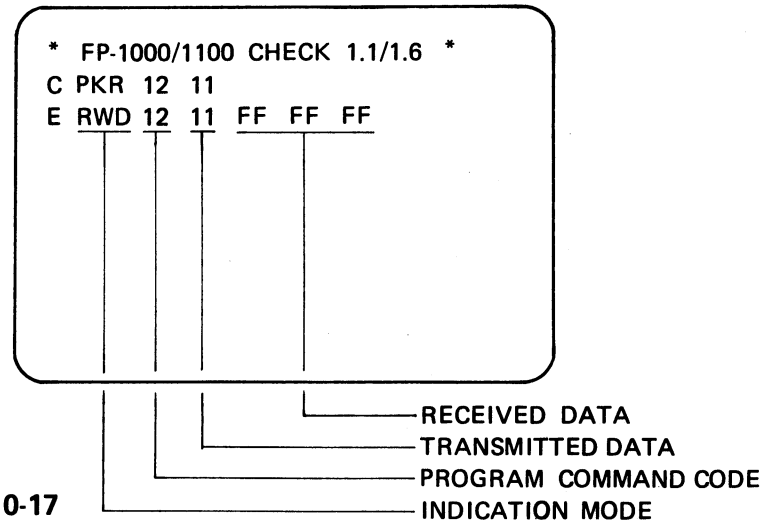


Fig. 10-17

- RS-232C INTERFACE SELF CHECK

1) Disconnect the RS-232C function check connector from the connector.
2) Enter 1218 ENTER (To end the execution, press the BREAK key.)

NORMAL DISPLAY MODE

Make sure that the display shows error indication and the data is as shown on the right.

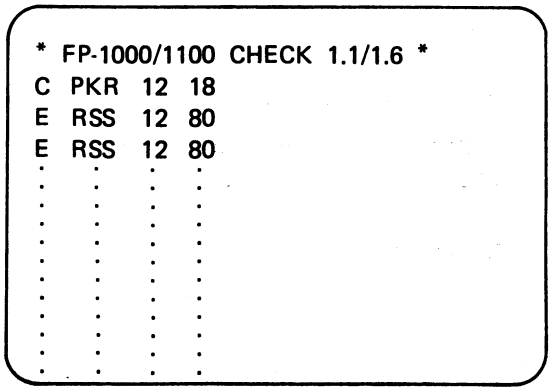


Fig. 10-18

- RS-232C INTERFACE PORT CHECK

This mode checks RS-232C connector port status and indicates its results in the following error mode if the port(s) is abnormal.

1) Install the RS-232C function check connector on the output connector of the pack.
2) Enter 121C ENTER

ERROR DISPLAY MODE

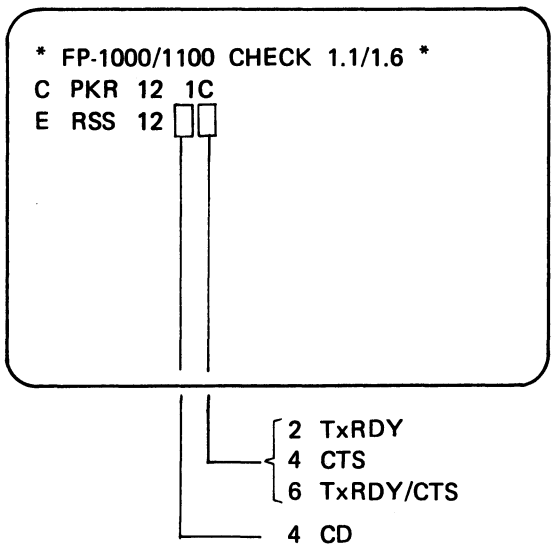


Fig. 10-19

- RS-232C DIP SWITCH CHECK

This mode indicates dip switch status by reading its on/off position.

1) Install the RS-232C function check connector on the output connector of the pack (without the function check connector, the program mode cannot read the dip switch status).
2) Enter 121B ENTER

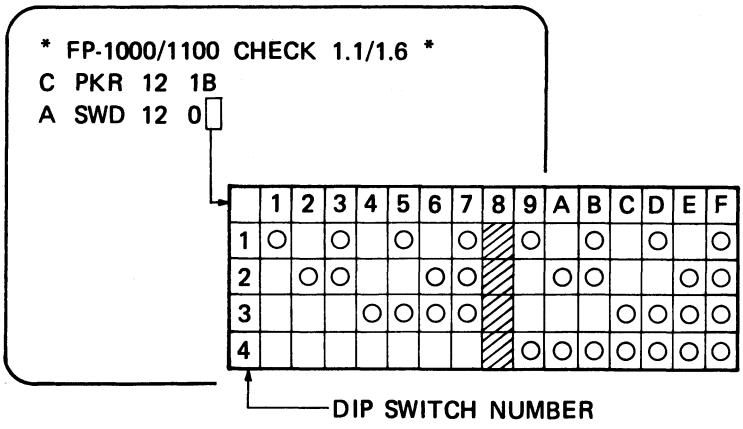


Fig. 10-20

10-9. EP-ROM PACK CHECK

This program operation checks EP-ROMs and its circuit in the EP-ROM pack (FP-1031) by reading sum total with each ROM. That result, only if the sum total differs from the sum total in the BASIC ROM, is indicated with its sum total.

1) Install an EP-ROM pack (FP-1031) in slot No. 2
2) Enter 1010 ENTER

ERROR DISPLAY MODE

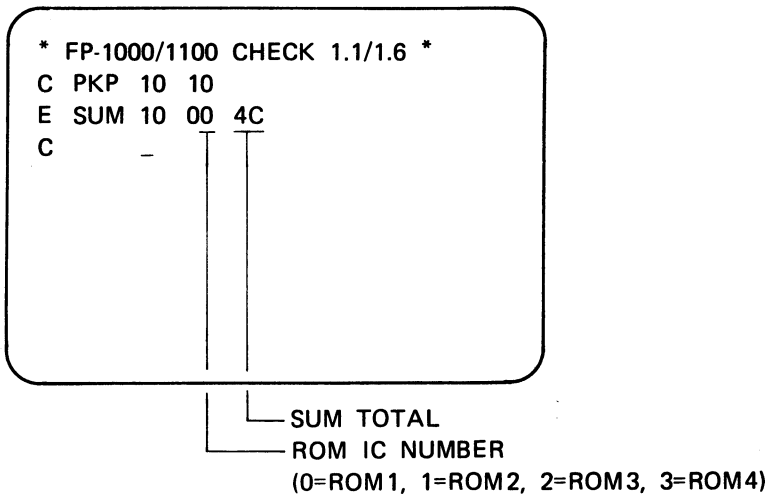


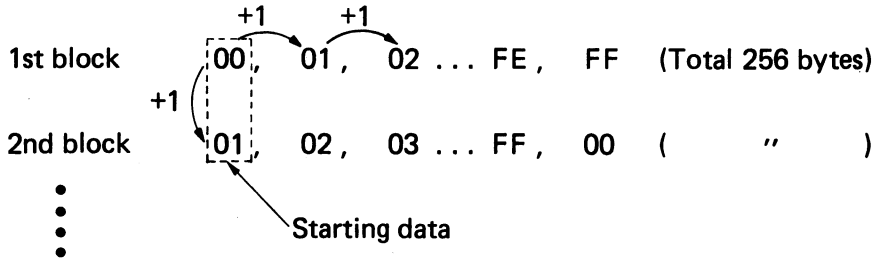
Fig. 10-21

10-10. CMOS-RAM PACK CHECK

This program operation checks CMOS-RAMs, its circuit and battery back-up function in the CMOS-RAM pack (FP-1030) by writing and read data in two different patterns. Result of the check can also be indicated in two modes only if an error occurs. This program also provides 14 modes and various executions are available by changing it. Refer to "FUNCTION TABLE" for detail of the mode.

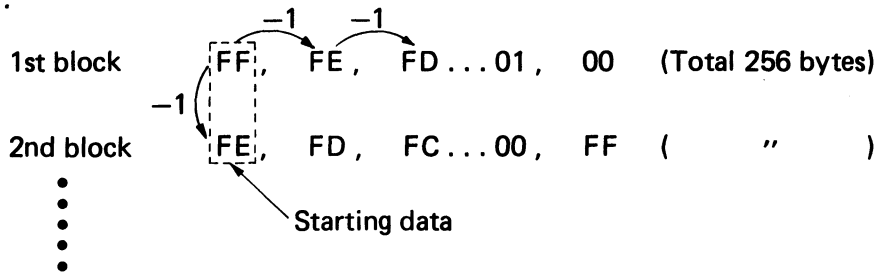
- DATA PATTERN (WT1)

As the address in one block of 256 bytes is incremented, the data is also incremented. After one block of data is written, the next block of starting data is automatically incremented.



- DATA PATTERN (WT2)

  As the address in one block of 256 bytes of data is incremented, the data is decremented on the contrary.



- READ PATTERN (RD1)

  This read pattern mode reads data in the RAMs which is written by mode WT1 and compares the data with the original data. Therefore, an error occurs when this mode reads the other data which is written by mode WT2.

- READ PATTERN (RD2)

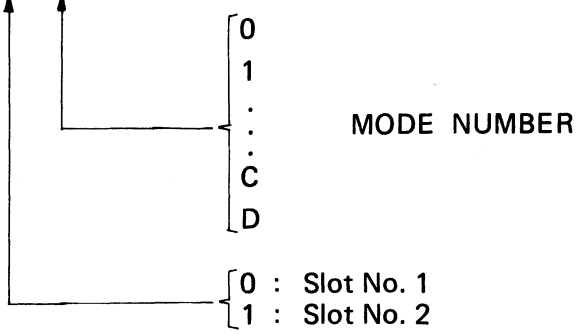
  This read pattern mode reads data in the RAMs which is written by mode WT2 and compares the data with the original data. Therefore, an error occurs when this mode reads the other data which is written by mode WT1.

SELECTION MODE	EXECUTION CYCLE				INDICATION MODE	
	WT1	RD1	WT2	RD2	RWS	RWD
0	●	●	●	●	●	
1		●	●	●	●	
2			●	●	●	
3				●	●	
4	●					
5		●			●	
6			●			
7				●	●	
8	●	●	●	●		●
9		●	●	●		●
A			●	●		●
B				●		●
C	●					
D		●				●

FUNCTION TABLE

1) Install a CMOS-RAM pack (FP-1030) in slot No. 2.

2) Enter 11 1 [ ] [ENTER]




```
* FP-1000/1100 CHECK 1.1/1.6 *
C PKC 11 11
E RWS 11 00 FF
E RWS 11 01 FF
E RWS 11 02 FF
E RWS 11 03 FF
E RWS 11 04 FF
E RWS 11 05 FF
E RWS 11 06 FF
E RWS 11 07 FF
C
```

NORMAL DISPLAY MODE

This display mode shows that selection mode No. 1 is selected. Because RD1 reads data which is written by write mode WT2, an error occurs.

READ OUT DATA
RAM IC NUMBER (0=RAM8, 1=RAM7, . . . 7=RAM1)
READ PATTERN MODE (0=RD1, 1=RD2)
PROGRAM COMMAND CODE
INDICATION MODE

Fig. 10-22

- RWS (read/write status)

  This indication mode shows only error status and the data by RAM IC.

- RWD (read/write data)

  This indication mode shows error address, the original data and read out data respectively. Read out data is indicated three times on one line.

To break the program execution, depress the [BREAK] key

```
* FP-1000/1100 CHECK 1.1/1.6 *
C PKC 11 19
E RWD 11 00 00 00 FF FF FF
E RWD 11 00 01 01 FE FE FE
E RWD 11 00 02 02 FD FD FD
```

READ OUT DATA
ORIGINAL DATA
ERROR ADDRESS

Fig. 10-23

MEMORY BACK-UP CHECK

To check memory back-up with the installed battery in the pack, execute the following three steps consecutively.

1) Enter 1116 ENTER
2) Turn off the power switch of the system unit and wait for about 3~4 hours. Then turn on it.
3) Enter 1117 ENTER

As soon as the executions are completed, the following display mode should be indicated if the memory back-up function is operating normally.

NORMAL DISPLAY MODE

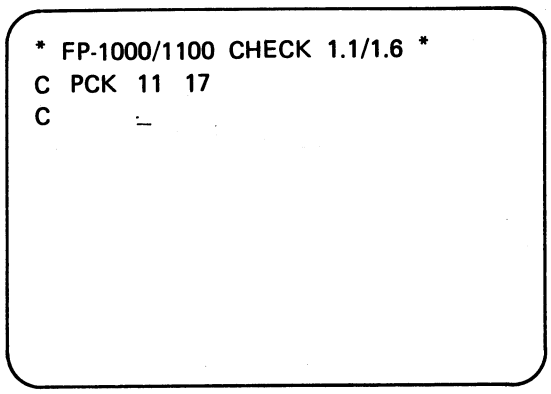


Fig. 10-24

10-11. D-RAM CHECK

This program operation checks D-RAMs (RAM1~RAM8) in the main P.C.B. by writing reversed fixed data and then reading out that data.

Enter 01 ENTER

NORMAL DISPLAY MODE

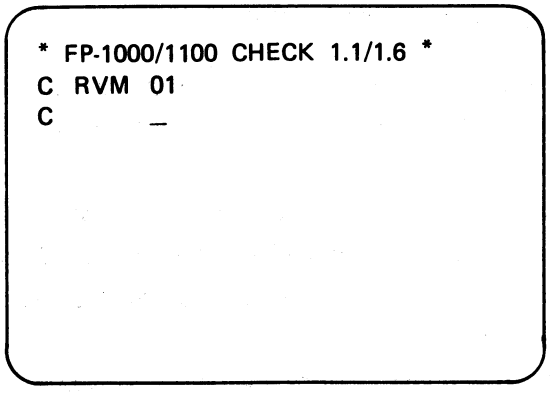


Fig. 10-25

EXPLANATION OF ERROR STATUS

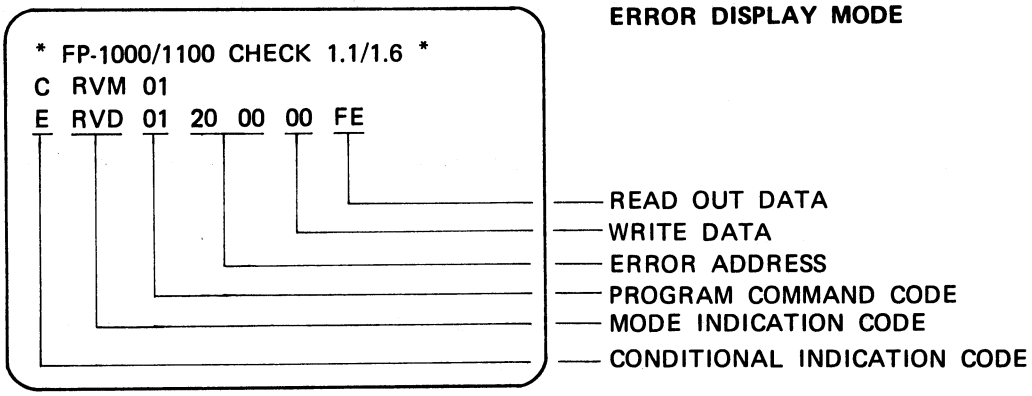
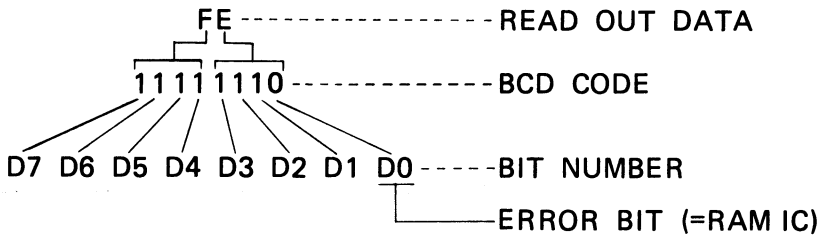


Fig. 10-26

- READ OUT DATA

This data is indicated on the screen only if the data differs from the reversed written data and can point out abnormal RAM IC (= bit number).



Suppose all RAMs and its circuit are normal, read out data will be "11111111" which is the reversed data of "00000000".

- WRITE DATA

This fixed data (00) is reversed before write and then it is written in the RAMs.

10-12. I/O INTERFACE CHECK

This program operation checks I/O interface signals including interrupt signals which are output through I/O slots with the I/O interface check tool (pack) installed in a slot that is going to be checked.

Firstly, 8-bit data generated by the ROMs is transmitted through address outputs $\overline{A}15$-$\overline{A}8$ from the CPU then switching its stream to 8-bit data lines, the data is returned to the CPU to be compared with the originally transmitted data. At this time, the lower 8-bit data ($\overline{A}7$-$\overline{A}0$) is fixed as "00".

After the above performance is completed, by changing-over the higher 8-bit address to the lower 8-bit address, the same is executed for address lines ($\overline{A}7$-$\overline{A}0$). The change-over is done by a flip-flop gate in the tool.

1) Install the tool in one of the following slots
2) Enter 02 [ ]

Slot number { 0, 2, 4, 6, 1, 3, 5, 7 } (Refer to diagram below for slot number.)

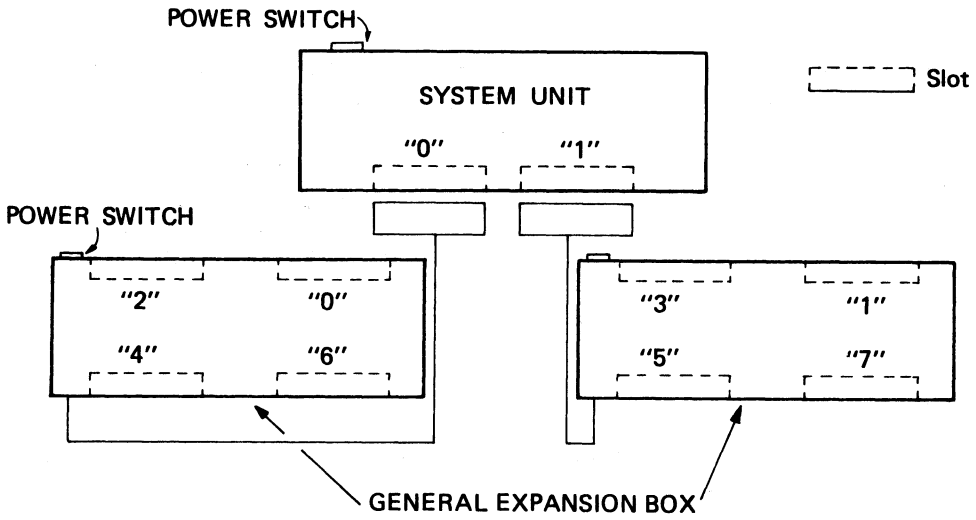


Fig. 10-27

NORMAL DISPLAY MODE

```
* FP-1000/1100 CHECK 1.1/1.6 *
A LPA 02 2A 40
A DVC 02 18
A LPA 02 42 03
C      _
```

Fig. 10-28

EXPLANATION OF ERROR STATUS

Example: With the tool installed in slot No. 0 of system unit, the display mode below is indicated on the screen after entering 02 and [ENTER] .

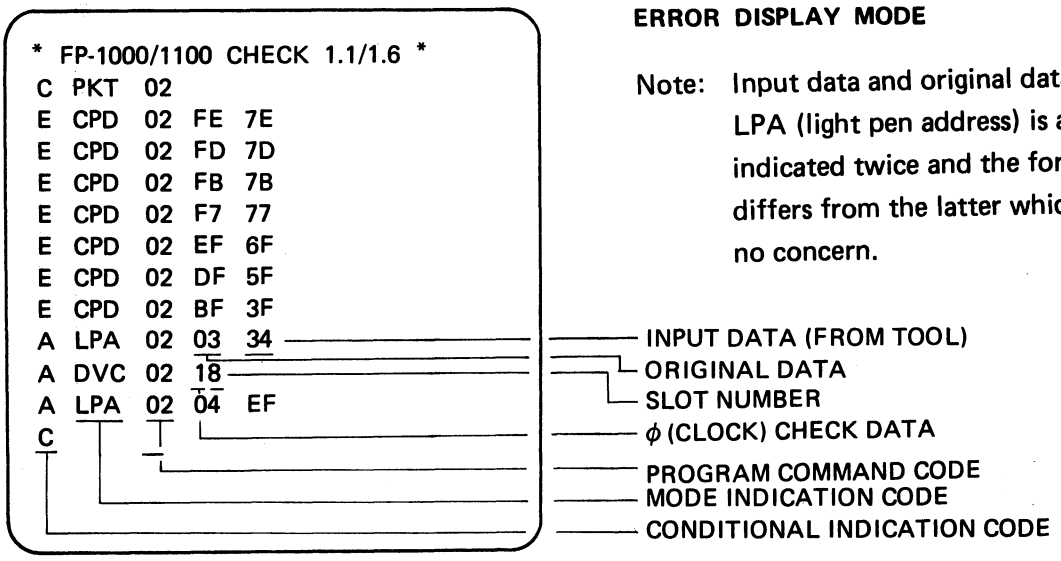
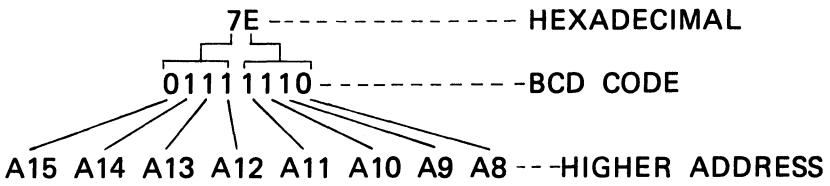


Fig. 10-29

- INPUT DATA

  This data transmitted from the tool consists of two digit hexadecimal numerals and should be compared with the original data.



- ORIGINAL DATA

  This data generated by the ROMs should be compared with input data for analysis of trouble.

- SLOT NUMBER

  The number in hexadecimal presents slot location where the tool (pack) is being installed.

  8 : slot in system unit
  9 : slot in general expansion box

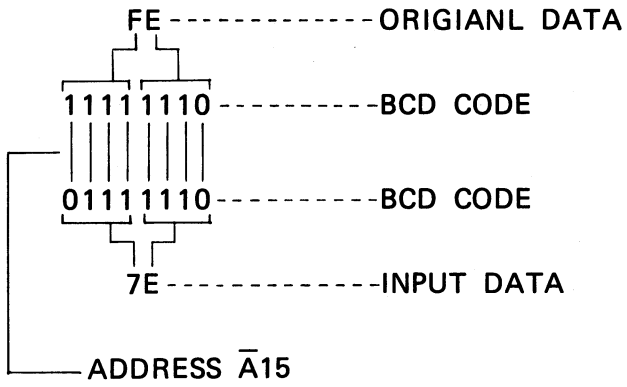
- φ (CLOCK) CHECK DATA

  This data indicates condition of clock output from the system unit in two:

  1 : Normal
  3 : Abnormal

ANALYSIS OF THE TROUBLE

Since the original data and the input data should be the same on the screen as long as the I/O interface circuit is operating normally, the input data should have been "FE", "FD", "FB", "F7", "EF", "DF" and "BF" respectively instead as shown on the given error example display mode.
To locate the cause of the trouble, the following conversion is essential.



As shown above, the input bit which differs from the original bit is the 1st bit from the left in this case, that is, address $\overline{A15}$ is the cause of the error.

10-13. PRINTER INTERFACE CHECK

This program operation checks printer interface signal outputs with the printer interface check tool (connector) connected with the printer connector which is made specially for this purpose. The output signals of 8-bit data, $\overline{INIT}$ and $\overline{STROBE}$ from the printer interface circuit are converted to be 3-bit input data (to CPU) in the circuit located in the tool. These 3-bit data are input through $\overline{BUSY}$, $\overline{ACKNLG}$ and $\overline{ERROR}$ signal gates.
Converted data is compared with the original data generated by the program ROMs on the screen. Then, by analyzing the difference between the original data and the converted data, the defective location can be traced.
In case no error condition exists, nothing shows except the program command on the screen.

1) Connect the tool
2) Enter 31 ENTER

NORMAL DISPLAY MODE

```
* FP-1000/1100 CHECK 1.1/1.6 *
C PTT 31
C      _
```

Fig. 10-30

ORIGINAL DATA	OUTPUT DATA									INPUT DATA		
	DATA								$\overline{INIT}$	$\overline{BUSY}$	$\overline{ACKNLG}$	$\overline{ERROR}$
	D8	D7	D6	D5	D4	D3	D2	D1				
0	1	1	1	1	1	1	0	0	0	1	1	1
0	1	1	1	1	1	1	0	1	0	1	1	1
0	1	1	1	1	1	1	0	0	1	1	1	1
1	1	1	1	1	1	1	0	1	1	1	1	0
0	1	1	1	1	1	0	1	0	1	1	1	1
2	1	1	1	1	1	0	1	1	1	1	0	1
0	1	1	1	1	0	1	1	0	1	1	1	1
3	1	1	1	1	0	1	1	1	1	1	0	0
0	1	1	1	0	1	1	1	0	1	1	1	1
4	1	1	1	0	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	0	1	1	1	1
5	1	1	0	1	1	1	1	1	1	0	1	0
0	1	0	1	1	1	1	1	0	1	1	1	1
6	1	0	1	1	1	1	1	1	1	0	0	1
0	0	1	1	1	1	1	1	0	1	1	1	1
7	0	1	1	1	1	1	1	1	1	0	0	0

INPUT AND OUTPUT DATA

EXPLANATION OF ERROR STATUS

Example: After entering 31 [ENTER] , data is indicated on the screen as shown below.

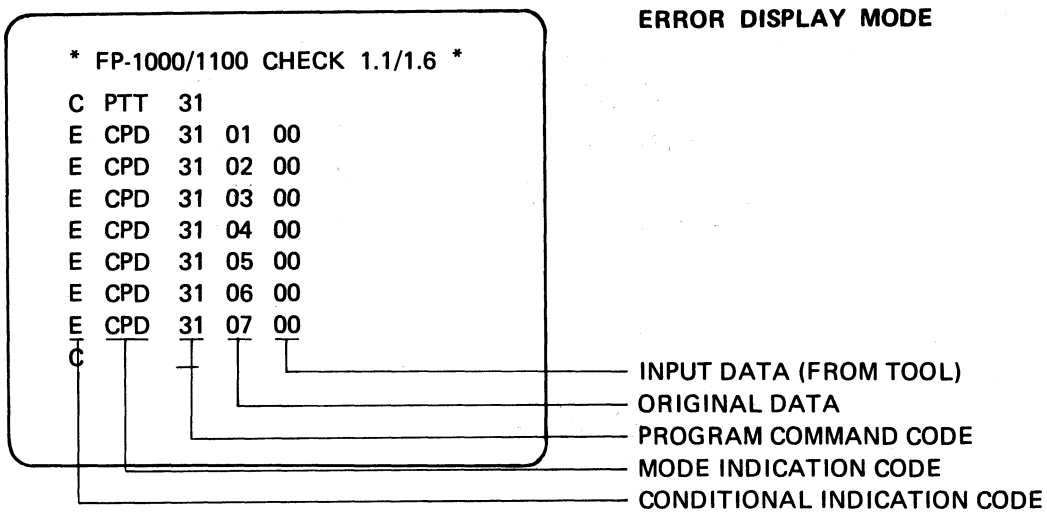
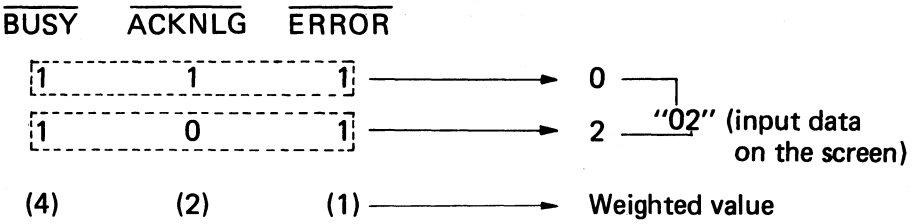


Fig. 10-31

- INPUT DATA

  This data transmitted from the tool consists of three bits and each bit has a weighted value ($\overline{BUSY} \rightarrow 4$, $\overline{ACKNLG} \rightarrow 2$, $\overline{ERROR} \rightarrow 1$). These three bits transform data indicated as input data on the screen.



- ORIGINAL DATA

  This data which is generated by the ROMs is indicated between the program command code and input data to be compared with the input data for analysis. The data is indicated in two digit hexadecimal numerals.

ANALYSIS OF THE TROUBLE

If all input data indicate "00" only, the chances are, data which cause output $\overline{Q}$ to be high must be low level (GND). So that all outputs, $\overline{BUSY}$, $\overline{INIT}$ and $\overline{STROBE}$ are forced to be high resulting in all input data becoming "00". Or $\overline{INIT}$ signal which can reset the flip-flop (SN74LS74N) must always be low or $\overline{STROBE}$ signal which enables printing possible must always be high.

Refer to "CIRCUIT DIAGRAM FOR THE TOOL" and "IC CONFIGURATION AND FUNCTION TABLE" for signal transformations.

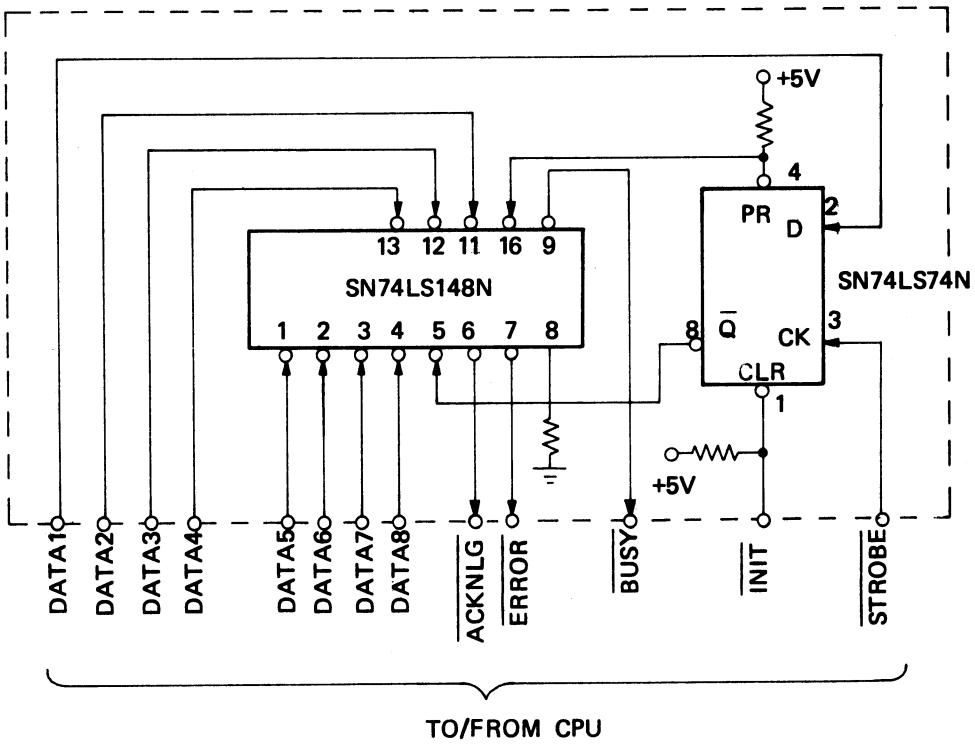
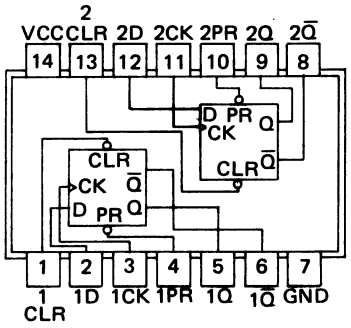


Fig. 10-32 CIRCUIT DIAGRAM FOR THE TOOL

SN74LS74N

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$



SN74LS148N

FUNCTION TABLE

INPUTS									OUTPUTS				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

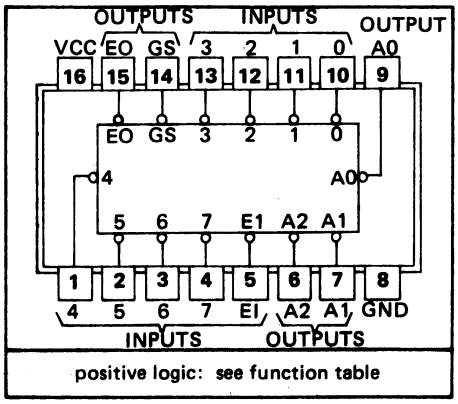


Fig. 10-33 IC CONFIGURATION AND FUNCTION TABLE

10-14. FDD CHECK

This program operation writes and reads data on a designated track or sector, then compares it with the original data. An error mode display is indicated only if data from the floppy disk drive differs from the original.

- WRITE/READ MODE 1

This mode writes data on all sectors of tracks 00, 13 and 27 of side Nos. 0 and 1 in both drives Nos. 0 and 1.
After that, data from both drives is compared with the original data in the write buffer.

1) Insert a formatted floppy disk sheet in drive Nos. 0 and 1.
2) Install mini floppy disk drive unit (FP-1020FD) in slot No. 2.
3) Turn on the power switch of the disk unit first, then the system unit.
4) Enter 1410 [ ][ ] [ENTER]

Any combination of 0 ~ F.

NORMAL DISPLAY MODE

The screen shows that data "FF" is written and read without any error.

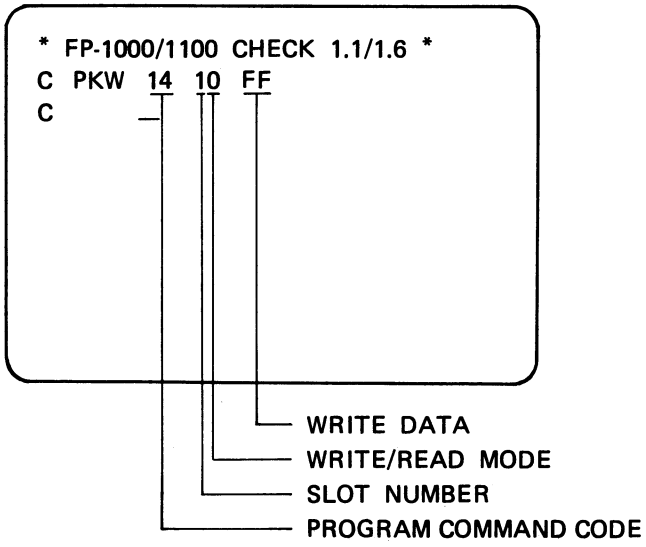


Fig. 10-34

- WRITE/READ MODE 2

This mode can write any data (combination of 0 to F) on designated sector and read that data to compare with the original written data.

1) Repeat operation steps 1) to 3) in "WRITE/READ MODE 1".
2) Enter 1413 [ ][ ] [ENTER] (To set data in write buffer)

DATA

3) Enter 1414 [ ][ ] [ENTER] (To write data in designated sector)

Sector number: 01 to 10

4) Enter 1416 [ ][ ] [ENTER] (To read back data from the sector which is designated in step 3))

Sector number (enter the same number in step 3))

ERROR DISPLAY MODE

To end the program execution,
depress the [BREAK] key.

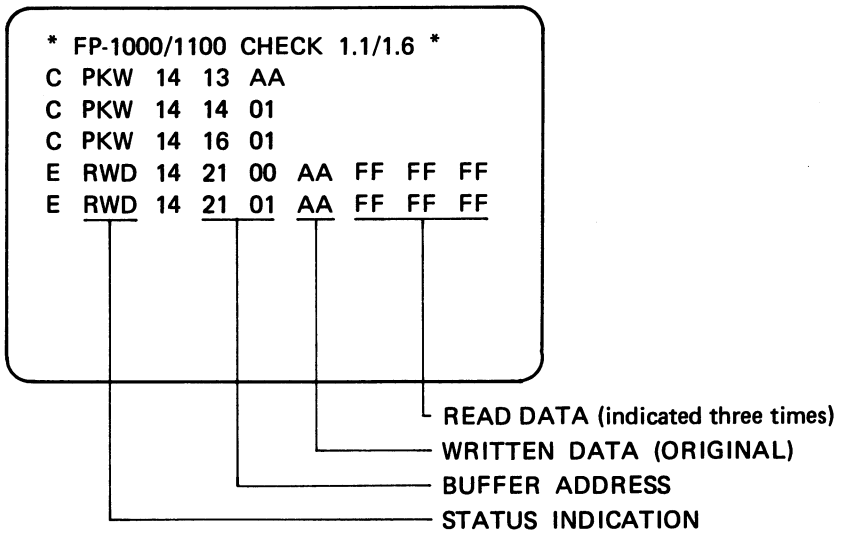


Fig. 10-35

- WRITE/READ MODE 3

This mode can write data and read in all sectors of a designated track to compare with the original data.

1) Repeat operation steps 1) to 3) in "WRITE/READ MODE 1" and step 2) in "WRITE/READ MODE 2".

2) Enter 1418 [ ][ ] [ENTER] (To write data in designated track)

TRACK NUMBER: 00 to 27

3) Enter 141A [ ][ ] [ENTER] (To read back data from the track which is designated in step 2))

TRACK NUMBER (enter the same track with step 2))

PARTS LIST
FP1000/FP1100

Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price J.F. Yen (¥) (FOB: JAPAN)	RANK
		MAIN P.C.B. G205-1					
	2001 1475	LSI	μPD780C-1	1		1,680	B
☆	2001 3800	I.C. (ROM)	HN61256PA51	1		1,350	B
☆	2001 3869	I.C.(EP-ROM)	HN46332G	1		1,140	B
☆	2009 1216	I.C.(RAM)	HM4864-2	8		3,000	B
☆	(2009 1325)	(I.C.(RAM)) or	(μPD4164D-3)	(8)		(2,775)	B
☆	(2101 9461)	(I.C.(RAM)) or	(TMM4164P-3)	(8)		(1,170)	B
	2110 3152	Bipolar I.C.	SN7493AN	1		126	B
☆	2111 0418	Bipolar I.C.	HD7417P	1		146	B
	2111 0663	Bipolar I.C.	HD74LS04P	5		36	B
	2111 0710	Bipolar I.C.	HD74LS32P	4		61	B
	2111 0809	Bipolar I.C.	HD74LS30P	1		53	B
	2111 0892	Bipolar I.C.	HD74LS157P	2		147	B
	2111 0949	Bipolar I.C.	HD74LS367P	6		138	B
	2111 2101	Bipolar I.C.	SN74LS00N	2		93	B
	2111 2119	Bipolar I.C.	SN74LS02N	1		93	B
	2111 2178	Bipolar I.C.	SN74LS74AN	3		117	B
	2111 2496	Bipolar I.C.	SN74LS174N	1		453	B
	2111 2852	Bipolar I.C.	SN74LS244N	1		504	B
	2111 2895	Bipolar I.C.	SN74LS148N	1		288	B
	2111 5291	Bipolar I.C.	SN74LS139N	1		230	B
☆	2184 1005	Bipolar I.C.	HD74S74	1		168	B
☆	2184 2301	Bipolar I.C.	M74LS273P	2		390	B
	2200 3577	Transistor	2SA1015	1	(10)	10	B
	2220 2375	Transistor	2SC945	1	(10)	9	B
	2600 2516	Carbon film resistor	R-25-100-J (100ohm, ¼W)	1	(10)	2	X
	2600 4110	Carbon film resistor	R-25-470-J (470ohm, ¼W)	1	(10)	2	X
	2600 4918	Carbon film resistor	R-25-1K-J (1Kohm, ¼W)	1	(10)	2	X
	2602 4919	Carbon film resistor	ELR-25-1K-J (1Kohm, ¼W)	12	(10)	2	X
	2614 0013	Carbon film resistor	R-25-10K-J (10Kohm, ¼W)	4	(10)	2	X
	2614 0170	Carbon film resistor	R-25-330-J (330ohm, ¼W)	2	(10)	2	X
	2614 0323	Carbon film resistor	R-25-3.3K-J (3.3Kohm, ¼W)	6	(10)	2	X
	2614 0404	Carbon film resistor	R-25-47-J (47ohm, ¼W)	2	(10)	2	X
	2614 0498	Carbon film resistor	R-25-4.7K-J (4.7Kohm, ¼W)	1	(10)	2	X
☆	2614 0528	Carbon film resistor	R-25-150-J (150ohm, ¼W)	1	(10)	2	X
	2614 0234	Carbon film resistor	R-25-1K-J (1Kohm, ¼W)	3	(10)	2	X
	2720 1954	Module resistor	MS1038 (10Kohm x 8)	1	(10)	20	X
	2720 2233	Module resistor	MS1028 (1Kohm x 8)	1	(10)	20	X

Notes: ☆ – parts newly employed
Q'ty – quantity used per unit
* – minimum order quantity per supply

Rank A : Essential
B : Stock recommended
C : Others
X : No stock recommended

Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price J.F. Yen (¥) (FOB: JAPAN)	RANK
☆	2730 0009	Module resistor	MT3314 (330ohm x 4)	1	(10)	15	X
☆	2807 0322	Electrolytic capacitor	10RE33 (33μF, 10V)	1	(10)	9	X
☆	2818 0144	Ceramic capacitor	HE60SJYB222K (2,200pF, 50V)	1	(10)	3	X
☆	2818 0233	Ceramic capacitor	HE12SJYB103K (0.01μF, 50V)	1	(10)	6	X
☆	2890 7150	Ceramic capacitor	FK20Y5V1H104Z (0.1μF, 50V)	20	(10)	16	X
☆	3500 4122	P.C.B. connector	PB21-56LT1	2	(10)	525	C
☆	3610 6735	I.C. Socket	DICA-24C-T1	1		68	X
☆	3610 6751	I.C. Socket	DICA-40C-T1	1		114	X
	3840 1246	Fasten knob	2207-2	2	(10)	3	X
☆	4306 5193	P.C.B. (without component)	G205-1	1		3,094	X
	6002 1279	FPC holder	P4320-1	1	(10)	14	X
	6002 4171	FPC (Flexible printed cable)	P4538-1	1		98	B
	6392 4202	Check pin	M4K3968	6	(10)	3	X
		SUB P.C.B. G205-2					
☆	2002 0016	LSI (CPU)	μPD7801G101	1		1,200	B
	2009 1211	LSI (FDC)	HD46505SP	1		1,800	B
	2100 3735	I.C.	TC4024BP	1		204	B
☆	2100 3948	I.C.	TC40H368P	2		132	B
☆	2101 8601	I.C. (EP-ROM)	HN462732G	1		1,050	B
	2110 3152	Bipolar I.C.	SN7493AN	1		126	B
☆	2110 3535	Bipolar I.C.	SN74157N	1		263	B
☆	2110 3764	Bipolar I.C.	SN7416N	2		165	B
	2111 0051	Bipolar I.C.	HD7400P	1		44	B
☆	2111 0418	Bipolar I.C.	HD7417P	2		146	B
	2111 0663	Bipolar I.C.	HD74LS04P	3		36	B
	2111 0710	Bipolar I.C.	HD74LS32P	4		61	B
	2111 0736	Bipolar I.C.	HD74LS08P	4		42	B
	2111 0850	Bipolar I.C.	HD74LS93P	2		132	B
	2111 0884	Bipolar I.C.	HD74LS151P	1		90	B
	2111 0892	Bipolar I.C.	HD74LS157P	2		118	B
☆	2111 0949	Bipolar I.C.	HD74LS367P	2		138	B
	2111 2101	Bipolar I.C.	SN74LS00N	3		74	B
	2111 2119	Bipolar I.C.	SN74LS02N	1		74	B
	2111 2135	Bipolar I.C.	SN74LS10N	1		56	B
	2111 2178	Bipolar I.C.	SN74LS74AN	6		94	B
	2111 2496	Bipolar I.C.	SN74LS174N	2		154	B
	2111 2607	Bipolar I.C.	SN74LS175N	4		191	B
	2001 3796	I.C. (ROM)	HN46332PA40	1		900	B

Notes: ☆ — parts newly employed
Q'ty — quantity used per unit
* — minimum order quantity per supply

Rank A : Essential
B : Stock recommended
C : Others
X : No stock recommended

Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price J.F. Yen (¥) (FOB: JAPAN)	RANK
	2111 5177	Bipolar I.C.	SN74LS240N	1		334	B
	2111 5533	Bipolar I.C.	SN74LS153N	4		114	B
	2111 5703	Bipolar I.C.	SN74LS145N	2		160	B
	2120 8086	I.C.	LM393P	1		79	B
☆	2120 8663	I.C.	μPC7095H	1		195	B
☆	2184 1005	Bipolar I.C.	HD74S74	3		168	B
☆	2184 2301	Bipolar I.C.	M74LS273P	2		390	B
☆	2184 2310	Bipolar I.C.	M74LS393P	1		408	B
☆	2184 2322	Bipolar I.C.	M74LS27P	2		44	B
☆	2184 2329	Bipolar I.C.	M74LS86P	2		45	B
☆	2184 2337	Bipolar I.C.	M74LS11P	1		41	B
	2220 2375	Transistor	2SC945	2	(10)	9	B
	2220 2405	Transistor	2SC945	1	(10)	9	B
☆	2220 2430	Transistor	2SC1216	1	(10)	90	B
	2230 3295	Transistor	2SD1111	1	(10)	28	B
	2300 1241	Diode	1S2075K	10	(10)	5	B
☆	2520 2082	Crystal oscillator	HC-43/U (15.97M)	1	(10)	165	X
	2600 2516	Carbon film resistor	R-25-100-J (100ohm, ¼W)	1	(10)	2	X
	2614 0013	Carbon film resistor	R-25-10K-J (10Kohm, ¼W)	19	(10)	2	X
	2614 0021	Carbon film resistor	R-25-100K-J (100Kohm, ¼W)	3	(10)	2	X
	2614 0081	Carbon film resistor	R-25-330K-J (330Kohm, ¼W)	1	(10)	2	X
	2614 0099	Carbon film resistor	R-25-38K-J (39Kohm, ¼W)	1	(10)	2	X
	2614 0145	Carbon film resistor	R-25-100-J (100ohm, ¼W)	5	(10)	2	X
	2614 0170	Carbon film resistor	R-25-330-J (330ohm, ¼W)	2	(10)	2	X
	2614 0188	Carbon film resistor	R-25-390-J (390ohm, ¼W)	1	(10)	2	X
	2614 0218	Carbon film resistor	R-25-68-J (68ohm, ¼W)	1	(10)	2	X
☆	2614 0226	Carbon film resistor	R-25-750-J (750ohm, ¼W)	5	(10)	2	X
	2614 0234	Carbon film resistor	R-25-1K-J (1Kohm, ¼W)	9	(10)	2	X
	2614 0242	Carbon film resistor	R-25-1M-J (1Mohm, ¼W)	1	(10)	2	X
	2614 0277	Carbon film resistor	R-25-2.2K-J (2.2Kohm, ¼W)	3	(10)	2	X
	2614 0293	Carbon film resistor	R-25-220K-J (220Kohm, ¼W)	1	(10)	2	X
	2614 0323	Carbon film resistor	R-25-3.3K-J (3.3Kohm, ¼W)	11	(10)	2	X
☆	2614 0358	Carbon film resistor	R-25-47K-J (47Kohm, ¼W)	2	(10)	2	X
☆	2614 0366	Carbon film resistor	R-25-68K-J (68Kohm, ¼W)	1	(10)	2	X
☆	2614 0404	Carbon film resistor	R-25-47-J (47ohm, ¼W)	1	(10)	2	X
	2614 0447	Carbon film resistor	R-25-150K-J (150Kohm, ¼W)	1	(10)	2	X
	2614 0463	Carbon film resistor	R-25-270K-J (270Kohm, ¼W)	1	(10)	2	X
☆	2614 0471	Carbon film resistor	R-25-270-J (270ohm, ¼W)	1	(10)	2	X

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	2614 0528	Carbon film resistor	R-25-150-J (150ohm, ¼W)	2	(10)	2	X
	2614 0536	Carbon film resistor	R-25-680-J (680ohm, ¼W)	1	(10)	2	X
	2614 0544	Carbon film resistor	R-25-1.2K-J (1.2Kohm, ¼W)	1	(10)	2	X
☆	2614 0552	Carbon film resistor	R-25-2K-J (2Kohm, ¼W)	1	(10)	2	X
☆	2614 0579	Carbon film resistor	R-25-470-J (470ohm, ¼W)	1	(10)	2	X
	2614 0773	Carbon film resistor	R-25-27-J (27ohm, ¼W)	1	(10)	2	X
☆	2614 1079	Carbon film resistor	R-25-620-J (620ohm, ¼W)	1	(10)	2	X
	2614 5074	Carbon film resistor	ELR-25-1K-J (1Kohm, ¼W)	26	(10)	2	X
	2614 5091	Carbon film resistor	ELR-25-10K-J (10Kohm, ¼W)	1	(10)	2	X
	2720 1954	Module resistor	MS1038 (10Kohm x 8)	3	(10)	20	X
	2720 2161	Module resistor	MS1024 (1Kohm x 4)	1	(10)	12	X
	2720 2233	Module resistor	MS1028 (1Kohm x 8)	2	(10)	20	X
	2720 2535	Module resistor	MS1039 (10Kohm x 9)	1	(10)	22	X
☆	2720 3116	Module resistor	MT3315 (330ohm x 5)	1	(10)	17	X
☆	2720 3141	Module resistor	MT7518 (750ohm x 8)	1	(10)	23	X
☆	2720 3167	Module resistor	MT33110 (330ohm x 10)	1	(10)	27	X
	2807 0013	Electrolytic capacitor	10RE47 (47μF, 10V)	1	(10)	8	X
☆	2807 0209	Electrolytic capacitor	16RE100 (100μF, 16V)	3	(10)	14	X
☆	2807 0322	Electrolytic capacitor	10RE33 (33μF, 10V)	1	(10)	9	X
	2818 0110	Ceramic capacitor	HE50SJYB102K (1,000pF, 50V)	4	(10)	3	X
	2818 0144	Ceramic capacitor	HE60SJYB222K (2,200pF, 50V)	1	(10)	3	X
	2818 0390	Ceramic capacitor	RT-HE40TKYB221K (220pF, 50V)	2	(10)	4	X
☆	2818 0403	Ceramic capacitor	RT-HE60TKYB222K (2,200pF, 50V)	3	(10)	4	X
	2818 0411	Ceramic capacitor	RT-HE40TKYB331K (330pF, 50V)	9	(10)	3	X
	2818 0420	Ceramic capacitor	RT-HE40TKYB471K (470pF, 50V)	1	(10)	4	X
	2818 0446	Ceramic capacitor	RT-HE40TKYB101K (100pF, 50V)	1	(10)	3	X
	2818 0471	Ceramic capacitor	RT-HE80TKYB472K (4,700pF, 50V)	1	(10)	4	X
☆	2818 0519	Ceramic capacitor	RT-HE60TKYB182K (1,800pF, 50V)	1	(10)	4	X
☆	2818 0535	Ceramic capacitor	RT-HE10TKYB822K (8,200pF, 50V)	1	(10)	6	X
	2818 2082	Ceramic capacitor	RT-HE70TKYF103Z (0.01μF, 50V)	1	(10)	3	X
☆	2818 2112	Ceramic capacitor	RT-HE13TKYF473Z (0.047μF, 50V)	3	(10)	6	X
	2818 3046	Ceramic capacitor	HE60SJCH470K (47pF, 50V)	2	(10)	4	X
	2818 3208	Ceramic capacitor	RT-HE50TKCH330-J (33pf, 50V)	2	(10)	4	X
☆	2890 7150	Ceramic capacitor	FK20Y5V1H104Z-P (0.1μF, 50V)	79	(10)	16	X
	3120 6022	Relay	BR211AD005-M	1		162	X

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☆	3420 4047	Slide switch	HSW0700-01-010	6	(10)	51	C
☆	3440 2043	Push switch	ESB-62133	1		53	C
	6213 1098	Push button A41	E41063-1	1	(10)	4	C
☆	3500 3622	Pin ass'y 15P	IL-G-15P-S3L2-E	1	(10)	46	X
☆	3510 3236	P.C.B. connector (36 pin)	57L-40360-2700	1		59	C
☆	3510 7550	P.C.B. connector (36 pin)	HBLB31S-2J	1		67	C
	3540 3035	Pin ass'y (5P)	5275-05A	1	(10)	23	C
☆	3610 6042	I.C. socket	QU-1C-L64T1	1		750	X
☆	3612 0142	DIN connector 8P	TCS4480-01-1011	2		71	C
☆	3612 0151	DIN connector 5P	TCS4450-01-1011	1		54	C
	3840 1246	Fasten tab	2207-2	2	(10)	3	X
☆	4306 5194	P.C.B. (without component)	G205-2	1		6,308	X
☆	5580 0014	Connector cap	57-36-S	1		83	X
☆	6002 5517	Earth spring	P4593-1	2	(50)	15	X
☆	6392 4202	Check pin	M4K3968	10	(100)	4	X
		DIFFERENCE PARTS IN FP-1100 AND FP-1000		FP1000	FP1100		
☆	2001 1963	I.C. (RAM)	μPD416C-3	8	24	338	B
	2111 2852	Bipolar I.C.	SN74LS244N	1	3	403	B
☆	2184 0075	Bipolar I.C.	SN74LS166AN	1	3	219	B
☆	3610 6760	I.C. socket	DICA-16C-T1	1	3	46	X
☆	6002 4197	Earth terminal G205	P4478-1	2	2	(10) 13	X
	2602 7314	Carbon film resistor	ELR-25-10K-J (10Kohm, ¼W)	0	1	(10) 2	X
		P.C.B. G205-SP-1					
	2111 2585	Bipolar I.C.	SN74LS123N	1		173	B
	2600 6112	Carbon film resistor	R-25-3.3K-J (3.3Kohm, ¼W)	1		(10) 2	X
	2600 7518	Carbon film resistor	R-25-12K-J (12Kohm, ¼W)	1		(10) 2	X
	2804 5069	Electrolytic capacitor	10RE47 (47μF, 10V)	1		(10) 6	X
	2818 0225	Ceramic capacitor	HE805JYB472K (4,700pF, 50V)	1		(10) 4	X
	2818 2040	Ceramic capacitor	HE70SJYF103Z (0.01μF, 50V)	1		(10) 5	X
☆	4306 5206	P.C.B. (without component)	G205-SP-1	1		15	X
		POWER SUPPLY CIRCUIT BOARD (G205-S1)					
	2120 8094	I.C.	LM358P	1		102	B
	2300 1021	Diode	1S2075K	1		(10) 4	B
	2310 3681	Zener diode	RD4.3EN2	1		(10) 9	B

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	2600 7313	Carbon film resistor	R-25-10K-J (10Kohm, ¼W)	1	(10)	2	X
	2600 3911	Carbon film resistor	R-25-390-J (390ohm, ¼W)	1	(10)	2	X
	2600 3318	Carbon film resistor	R-25-220-J (220ohm, ¼W)	1	(10)	2	X
	2600 5914	Carbon film resistor	R-25-2.7K-J (2.7Kohm, ¼W)	1	(10)	2	X
	2800 4976	Electrolytic capacitor	16RE33 (33μF, 16V)	1	(10)	7	X
	2804 5123	Electrolytic capacitor	10RE33 (33μF, 10V)	1	(10)	22	X
	2818 0071	Ceramic capacitor	HE40SJYB331K (330pF, 50V)	1	(10)	3	X
	2818 0144	Ceramic capacitor	HE60SJYB222K (2,200pF, 50V)	1	(10)	3	X
	2818 0365	Ceramic capacitor	RT-HE50TKYB102K-T (1,000pF, 50V)	1	(10)	3	X
	3590 0560	Connector ass'y	5196-05 E31549-3	1		133	C
	2120 8621	I.C.	μPC7912H	1		221	B
	2200 3534	Transistor	2SA1015-Y	3	(10)	11	B
☆	2300 9129	Diode stack	SIVB10	1	(10)	42	B
☆	2300 9145	Diode stack	S4VB10-E4001	1	(10)	108	B
☆	2310 6591	Zener diode	RD5.1EN3-TN-T	1	(10)	11	B
	2600 9715	Carbon film resistor	R-25-100K-J (100Kohm, ¼W)	1	(10)	2	X
	2600 5311	Carbon film resistor	R-25-1.5K-J (1.5Kohm, ¼W)	2	(10)	2	X
	2600 6716	Carbon film resistor	R-25-5.6K-J (5.6Kohm, ¼W)	1	(10)	2	X
	2600 2516	Carbon film resistor	R-25-100-J (100ohm, ¼W)	2	(10)	2	X
	2600 4918	Carbon film resistor	R-25-1K-J (1Kohm, ¼W)	3	(10)	2	X
	2600 6317	Carbon film resistor	R-25-3.9K-J (3.9Kohm, ¼W)	2	(10)	2	X
☆	2700 3028	Metal film resistor	ERX-2AN-J-OR22	2	(10)	17	X
☆	2770 6029	Variable resistor	SR19R-2.2KB (2.2Kohm, 0.15W)	2	(10)	45	X
☆	2804 5573	Electrolytic capacitor	25RPE2200 (2,200μF, 25V)	1	(10)	132	X
	2804 6332	Electrolytic capacitor	25L10000SC (10,000μF, 25V)	1	(10)	365	X
	2804 5093	Electrolytic capacitor	25RE33 (33μF, 25V)	1	(10)	8	X
	2804 5051	Electrolytic capacitor	16RE10 (10μF, 16V)	1	(10)	9	X
	2804 4933	Electrolytic capacitor	16RE100 (100μF, 16V)	1	(10)	11	X
	2812 7022	SC capacitor	SC45D1E473Z (0.047μF, 25V)	2	(10)	5	X
	2818 0390	Ceramic capacitor	RT-HE40TKYB221K-T (220pF, 50V)	1	(10)	4	X
	3630 2747	Fuse	SS-2-5A	1	(10)	26	B
	3631 0014	UL time-lag fuse	UL-TSC-2A	1	(10)	35	B
	3631 0022	UL time-lag fuse	UL-TSC-3A	1	(10)	39	B
	3640 2314	Fuse clip	UF-0017	2	(10)	5	X
	3640 2331	Fuse clip	UF-0033	4	(10)	3	X
☆	4306 5208	P.C.B. (without component)	G205-S1	1		89	X
	6392 4202	Check pin	M4K3968	4	(100)	3	X

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		POWER SUPPLY CIRCUIT BOARD (G205-S2)					
	2830 4081	Mylar capacitor	630MW473M	3	(10)	24	X
	2830 7021	MP capacitor	PME265MA447	2	(10)	68	X
	3020 2066	Noise filter	UF2426C-801Y2R5	1		132	X
	3020 2082	Noise filter	TF2317C-100Y2R5	1		59	X
☆	3440 5280	Push switch	SDL-1P	1		113	C
	3640 2314	Fuse clip	UF-0017	2	(10)	4	X
☆	4306 5167	P.C.B. (without component)	G205-S2	1		203	X
☆	3630 3107	UL fuse	ST4-1.6A	1	(10)	38	B
☆	3630 8141	SEMKO Fuse	EAK-0.8A (T)	1	(10)	33	B
☆	2700 2871	Metal film resistor	RK14B3A-2.2MJ	1	(10)	90	X
		POWER SUPPLY CIRCUIT BOARD (G205-S3)					
	2320 3154	LED	TLG114A	1	(10)	31	B
☆	4306 5209	P.C.B. (without component)	G205-S3	1		33	X
		Power supply unit					
☆	2300 9153	Diode stack	S5VB10 (F4002)	1	(10)	146	B
☆	2804 6324	Electrolytic capacitor	16L22000SC (22,000μF, 16V)	1	(10)	468	B
☆	3000 2385	Power transformer	TE-205-2E	1		2,009	C
	5041 5171	Screw (+)	3 x 6 ZMC-3	4	(50)	2	X
	5161 3066	Screw (+)	4 x 8 ZMC-3	4	(50)	2	X
	5161 3210	Screw (+)	3 x 5 ZMC-3	2	(50)	2	X
	5161 3317	Screw (+)	3 x 6 ZMC-3	2	(50)	2	X
	5161 3325	Screw (+)	3 x 35 ZMC-3	4	(50)	5	X
	5161 3333	Screw (+)	3 x 80 ZMC-3	1	(50)	5	X
	5161 4089	Screw (+)	3 x 10	1	(50)	2	X
	5161 4488	Screw (+)	3 x 60	1	(50)	5	X
	5430 0093	Flange nut	M3	1	(50)	3	X
☆	6002 3051	Spacer G205	P4459-1	1	(10)	36	X
☆	5900 1609	Circuit board supporter	LCBS-3N	4	(10)	18	X
☆	6002 5665	Spacer A G205	P4606-1	1	(10)	41	X
☆	6002 5673	P.C.B. fixing plate G205	P4608-1	1		450	X

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☆	6020 7305	Power switch cap G205	P4479A-1	1	(10)	20	X
☆	6020 7445	Power chassis G205	P2259A-1	1		278	X
		(1) Europe					
☆	3230 1304	Cooling fan	PXJ-43-B3	1		2,430	X
	5041 5252	Screw (+)	3 x 5 ZMC-3	2	(50)	2	X
	5161 3139	Screw (+)	4 x 6 ZMC-3	1	(50)	2	X
		(2) U.S.A. and CANADA					
	3230 1291	Cooling fan	PXJ-44-B1	1			X
	5041 5252	Screw (+)	3 x 5 ZMC-3	6	(50)	2	X
	5161 3139	Screw (+)	4 x 6 ZMC-3	1	(50)	2	X
	5161 3295	Screw (+)	3 x 5 ZMC-3	2	(50)	2	X
☆	6002 2985	Noise filter cover	P3487-1	1	(10)	89	X
☆	6002 3042	Power switch cover	P4458-1	1	(10)	44	X
		(3) U.K.					
	5041 5252	Screw (+)	3 x 5 ZMC-3	2	(50)	2	X
	5161 3139	Screw (+)	4 x 6 ZMC-3	1	(50)	2	X
		(4) Other areas					
	3600 1046	Voltage selector	S-J2875-05	1		117	X
	5041 5023	Screw (+)	2.6 x 6 ZMC-3	2	(50)	2	X
	5041 5252	Screw (+)	3 x 5 ZMC-3	4	(50)	2	X
	5161 3139	Screw (+)	4 x 6 ZMC-3	1	(50)	2	X
☆	6002 2977	Noise filter cover G205	P3486-1	1	(10)	177	X
		PACK HOLDER					
☆	2230 1314	Transistor	2SD587M-(Q, R)	1	(10)	135	B
☆	2230 3619	Transistor	2SD1193	2	(10)	191	B
	5161 4437	Screw pan (+)	3 x 12	2	(50)	2	X
	5161 4461	Screw pan (+)	3 x 14	4	(50)	2	X
	5210 0224	Screw pipe	3 x 6 x 8	4	(50)	5	X
	5430 0093	Flange nut	M3	2	(50)	3	X
☆	6020 7275	Heat sink plate G205	P3591A-1	1		410	X
		P.C.B. FIXING PLATE					
	5161 3031	Screw pan (+)	3 x 10, ZMC-3	4	(50)	2	X
	5210 0275	Screw pipe	3 x 6 x 10	1	(50)	5	X
☆	5900 1609	P.C.B. supporter	LCBS-3N	2		18	X
☆	6002 5568	P.C.B. holding screw	P4603-1	1		300	X
☆	6020 7127	P.C.B. fixing plate G205	P2199A-1	1		270	X

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		UPPER CASE UNIT					
5	5430 0093	Flange nut	M3	5	(50)	3	X
4 ☆	6002 2993	Case support plate G205	P3508-1	1		60	X
☆	6002 3026	Front seal D G205	P3517-1	1	(10)	38	X
☆	6002 3123	Front seal A G205	P4498-1	1	(10)	5	X
1 ☆	6025 3021	Upper case G205	P189B-1	1		1,755	X
2 ☆	6002 2888	Upper case G205A	P186-1 (FP1000)	1		375	X
3 ☆	6002 2896	Upper case G205B	P186-2 (FP1100)	1			X
		LOWER CASE SECTION					
	3660 3011	Lug terminal	1.25-4	2	(10)	2	X
	3660 3046	Lug terminal	2-4	6	(10)	3	X
9 ☆	3660 8013	Earth terminal	T-10	2	(10)	78	X
	5041 5155	Screw pan (+)	3 x 8 ZMC-3	2	(10)	2	X
10	5111 5023	Tapping screw (+)	3 x 8 ZMC-3	20	(50)	2	X
	5111 5511	Tapping screw (+)	2.5 x 6 ZMC-3	2	(50)	2	X
	6002 3107	Slide switch label G205	P4504-1	1	(10)	5	X
	6002 3115	Earth metal G205	P4505-1	1	(10)	13	X
	6002 4138	Earth metal G205	P4505-2	1	(10)	13	X
10	5111 5023	Tapping screw (+)	3 x 8 ZMC-3	8	(50)	2	X
☆	6002 5550	Reinforce metal G205	P4595-1	2	(10)	8	X
6	6020 6881	Lower case G205B	P194A-2	1		659	X
7 ☆	6029 1616	Rear panel A G205	P188C-1	1		915	X
8 ☆	6029 1624	Rear panel B G205	P188C-2 (U.S.A. & CANADA only)	(1)		660	X
☆	6002 4154	FCC label	P4540-1 (U.S.A. & CANADA only)	(1)	(10)	8	X
12	5150 0920	Bind tapping screw (+)	3 x 8 ZMC-3	7	(50)	2	X
11	5150 0954	Bind tapping screw (+)	3 x 10 ZMC-3	5	(50)	2	X
☆	6002 5657	Rubber foot B G205	P4605-1	5	(10)	10	X
☆	6002 2969	Slot cover G205	P3481-1	2		25	X
☆	6002 3131	Carl cord holder G205	P4480-1	1	(10)	8	X
☆	6002 5533	FG label G206H	P4597-1	1	(10)	9	X
☆	6002 5584	Static electricity cover G205	P1131-1	1		4,500	X
☆	3700 9601	Power cord	P-VCTFK-AB (Japan)	1		164	X
☆	3700 9725	Power cord	CLASS-1-BA (Europe)	1		375	X
☆	3700 9733	Power cord	SVT-BA (U.S.A. & CANADA)	1		375	X
☆	3700 9741	Power cord	LD3BS-BA (U.K.)	1		225	X
☆	3700 9717	Power cord	VCTF-BA (Other areas)	1		326	X

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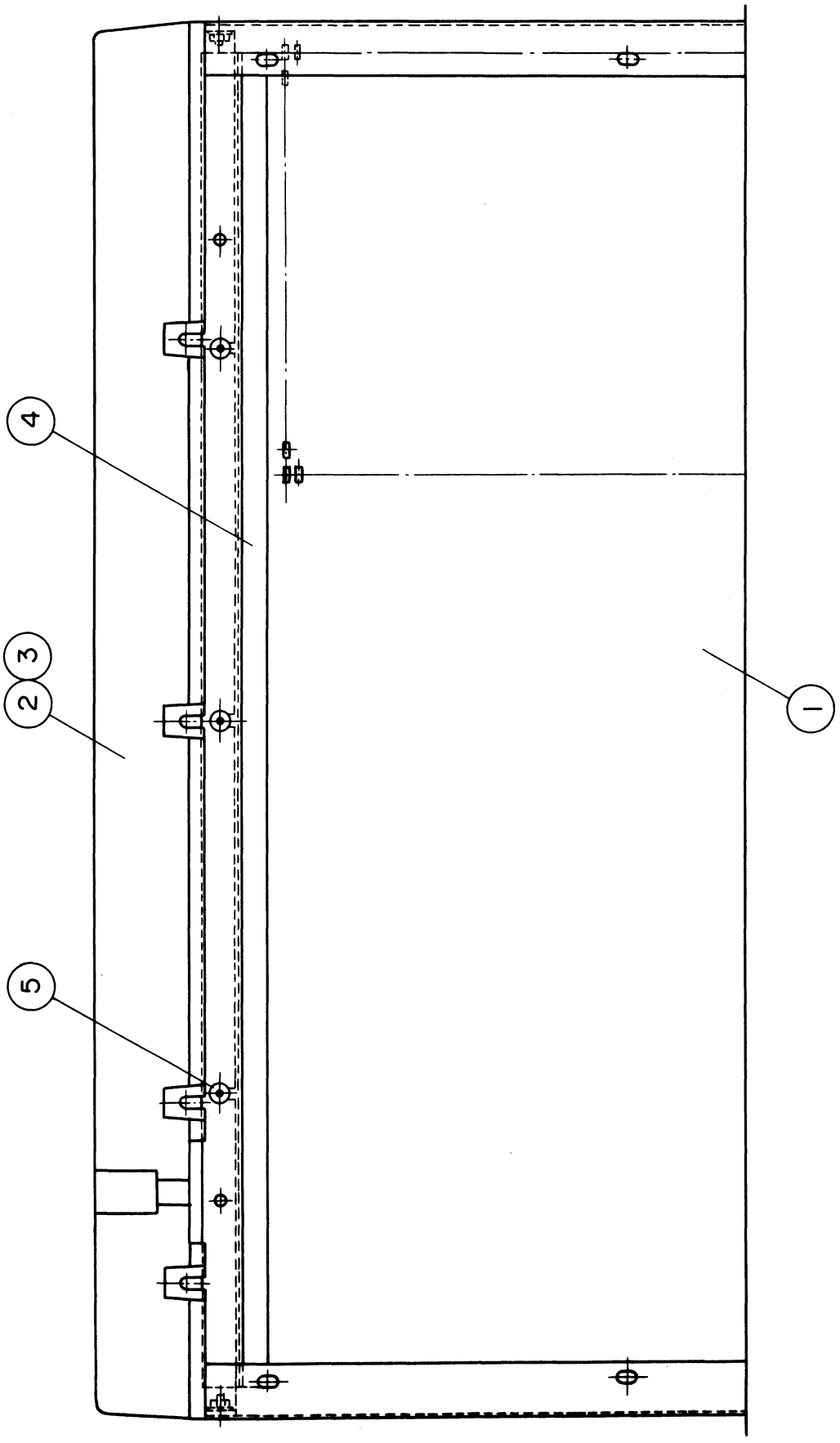
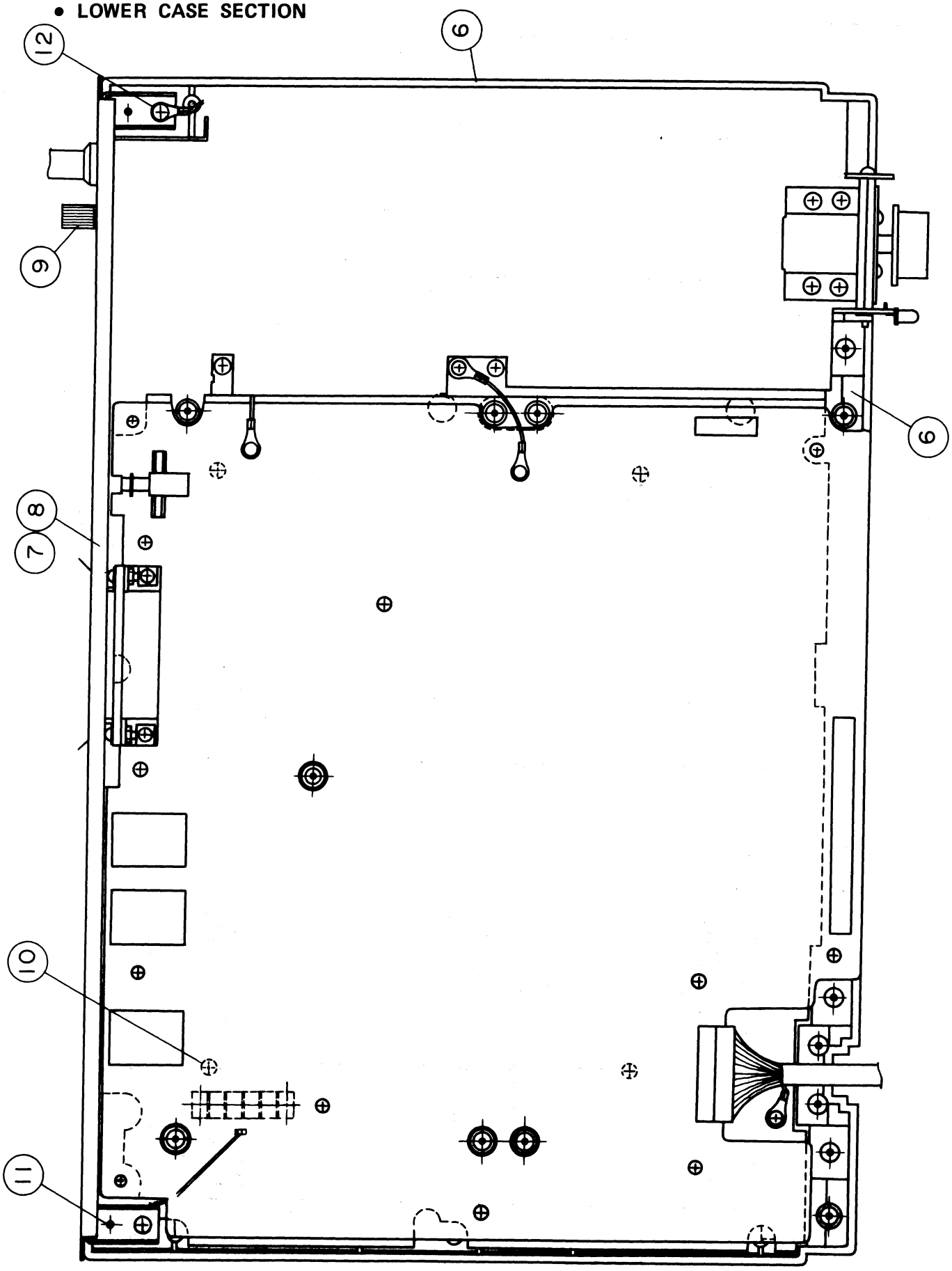
EXPLODED DRAWING 1

- **UPPER CASE**



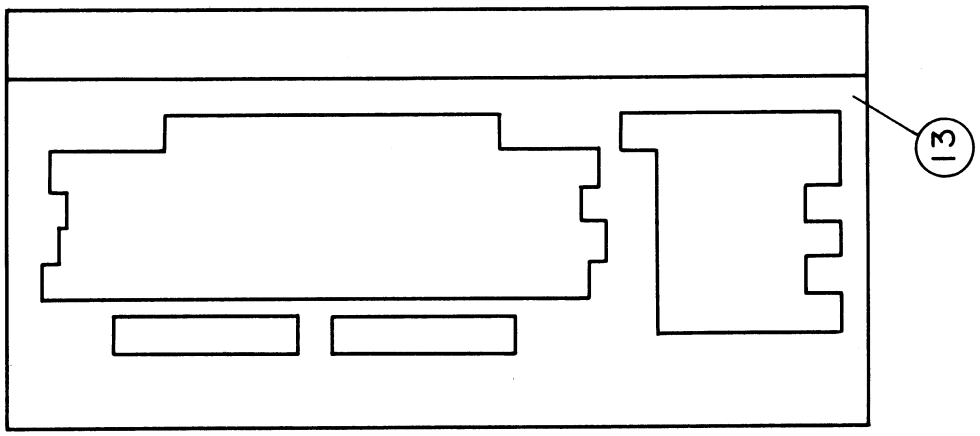
EXPLODED DRAWING 2

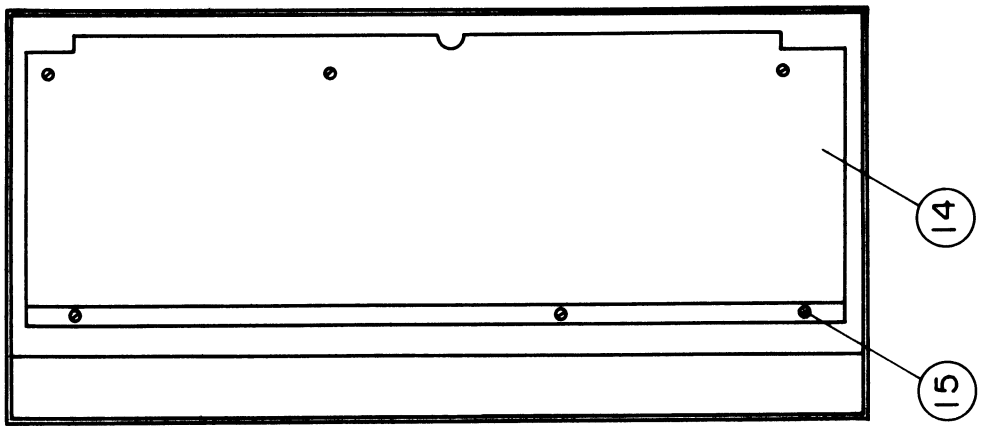
- **LOWER CASE SECTION**

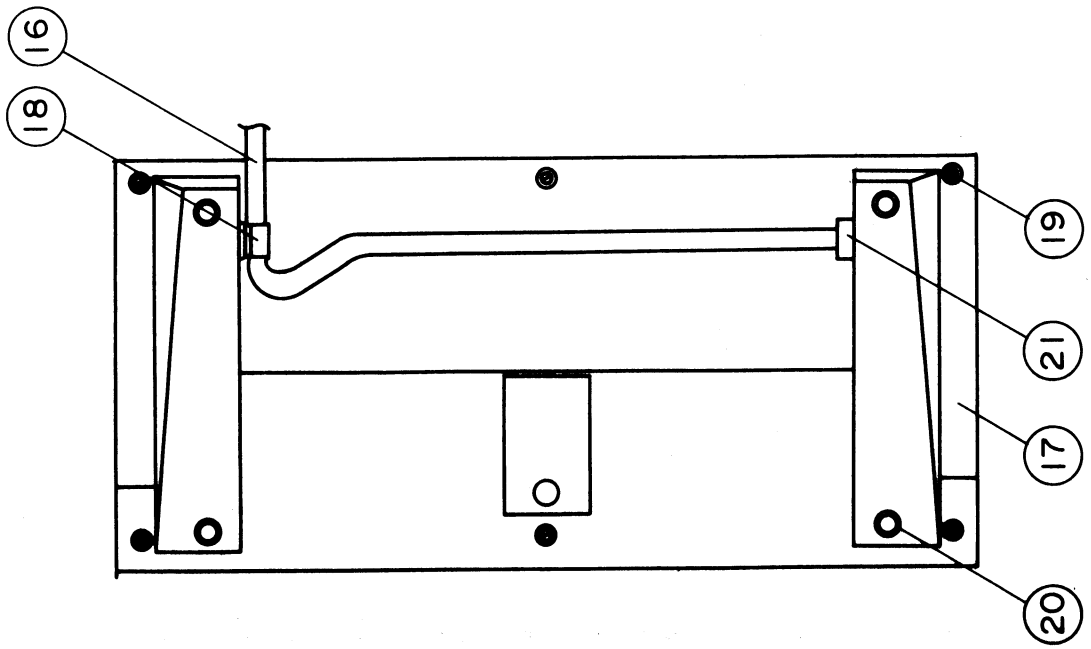


EXPLODED DRAWING 3

- **KEYBOARD UNIT**



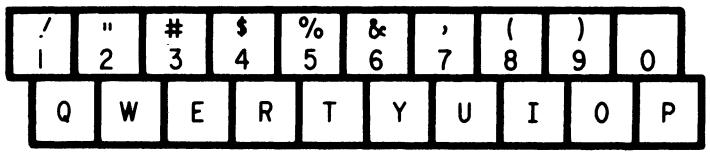




ASCII KEY TOP DRAWING

(22)

(23)



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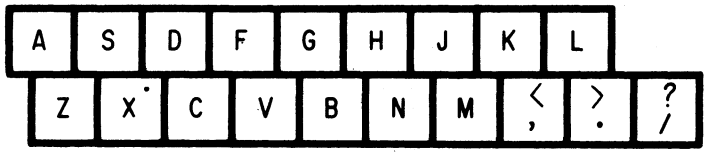

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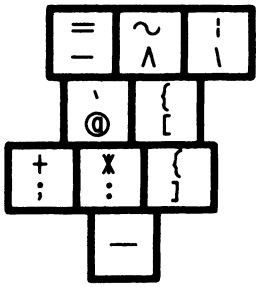

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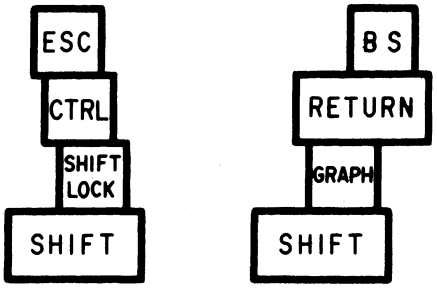

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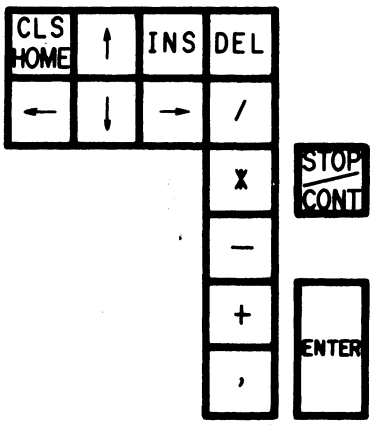

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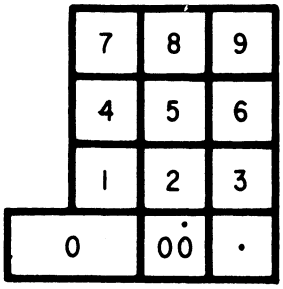

Your constructive comments and suggestions concerning the contents of this service manual will assist us in our continuous efforts to improve the quality, the accuracy and the usefulness of this service manual.
If you have any comments and/or suggestions, please mail them to:

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PRINTED IN JAPAN

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