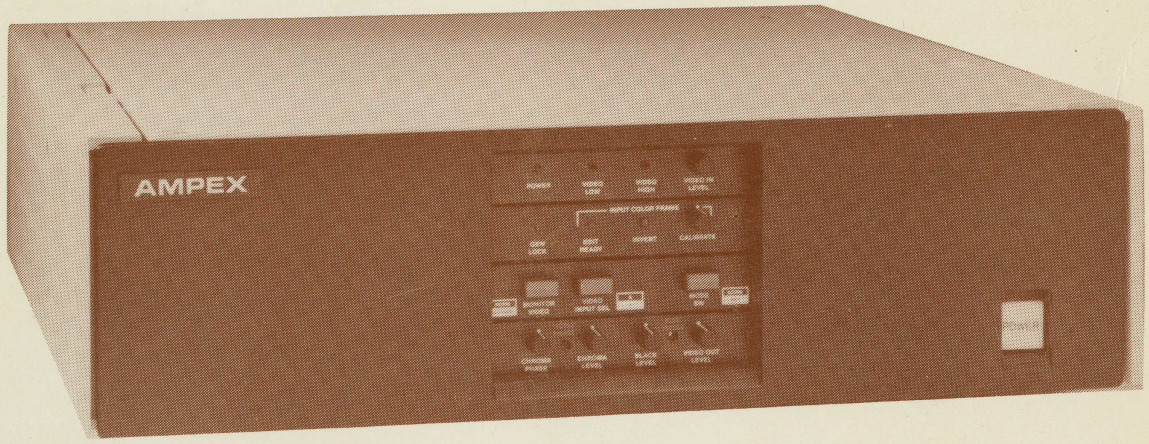
TBC-80

DIGITAL TIME-BASE CORRECTOR

INSTALLATION AND OPERATION



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Issued: April 1983

TBC-80
DIGITAL TIME-BASE CORRECTOR

INSTALLATION AND OPERATION MANUAL

AMPEX CORPORATION
AUDIO-VIDEO SYSTEMS DIVISION

Prepared by

AVSD Technical Publications
Ampex Corporation
401 Broadway
Redwood City, CA 94063

Catalog No. 1809591-01
Issued: April 1983

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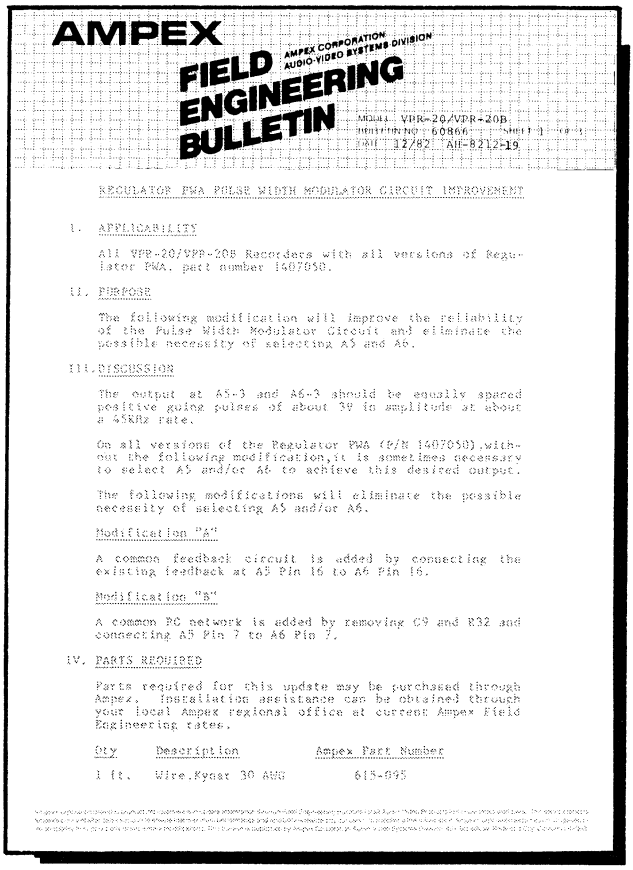

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AMPEX CORPORATION
AUDIO-VIDEO SYSTEMS DIVISION

FIELD ENGINEERING BULLETIN

MODEL VPR-20/VPR-20B

DATE 12/82 AH-8212-19

REGULATOR PWA PULSE WIDTH MODULATOR CIRCUIT IMPROVEMENT

I. APPLICABILITY

All VPR-20/VPR-20B Recorders with all versions of Regulator PWA, part number 1407050.

II. PURPOSE

The following modification will improve the reliability of the Pulse Width Modulator Circuit and eliminate the possible necessity of selecting A5 and A6.

III. DISCUSSION

The output at A5-3 and A6-3 should be equally spaced positive going pulses of about 3V in amplitude at about a 45KHz rate.

On all versions of the Regulator PWA (P/N 1407050), without the following modification, it is sometimes necessary to select A5 and/or A6 to achieve this desired output.

The following modifications will eliminate the possible necessity of selecting A5 and/or A6.

Modification "A"

A common feedback circuit is added by connecting the existing feedback at A5 Pin 16 to A6 Pin 16.

Modification "B"

A common PC network is added by removing C9 and R32 and connecting A5 Pin 7 to A6 Pin 7.

IV. PARTS REQUIRED

Parts required for this update may be purchased through Ampex. Installation assistance can be obtained through your local Ampex regional office at current Ampex Field Engineering rates.

Qty	Description	Ampex Part Number
1 ft.	Wire, Kynar 30 AWG	615-095

To receive these bulletins, send us the following information:

Owner's Name
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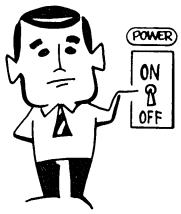
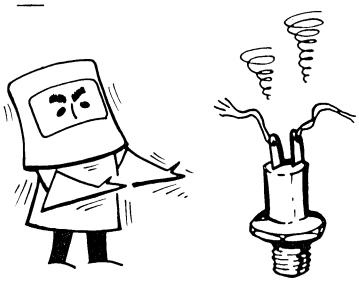
SAFETY AND FIRST AID SUGGESTIONS

Regardless of how well electrical equipment is designed, personnel can be exposed to **dangerous electrical shock** when protective covers are removed for maintenance or other activities. Therefore, it is incumbent on the user to see that all safety regulations are consistently observed and that each individual assigned to the equipment has a clear understanding of first aid related to electrical hazards.

In addition, the following safety practices must be followed:



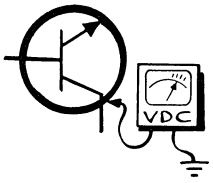
1 Do not attempt to adjust unprotected circuit controls or to dress leads with power **on**.



2 Do not touch heavily loaded or overheated components without precaution to avoid burns.

3 Do not assume that all danger of electrical shock is removed when power is **off**. Charged capacitors can retain dangerous voltages for a long time after power is removed. These capacitors should be discharged through a suitable resistor before any circuit points are touched.

4 Always avoid placing parts of the body in series between ground and circuit points.



5 Remember that some semiconductor cases and solid-state circuits carry high voltages.

6 Don't take chances. Be fully trained. Ampex equipment should be operated and maintained by fully qualified personnel.

If someone seems unable to free himself while receiving an electrical shock, **turn power off** before attempting to render aid. A muscular spasm or unconsciousness can make a victim unable to free himself from the electrical power.

WARNING

DO NOT TOUCH VICTIM OR HIS CLOTHING BEFORE POWER IS REMOVED OR YOU MAY ALSO BECOME A SHOCK VICTIM.

If power cannot be removed immediately, **very carefully** loop a length of dry nonconducting material (such as rope, insulating material, or clothing) around the victim and pull him free of the power. Carefully avoid touching him or his clothing until free of power. Immediately start the appropriate first aid procedures.

GOOD PRACTICES

In maintaining the equipment covered in this manual, please keep in mind the following standard good practices:

1 When connecting any instrument (oscilloscope, waveform monitor, etc.) to a high-frequency output, use the appropriate termination resistor at the input of the instrument, unless the instrument is terminated internally.

2 When inserting or removing printed wiring assemblies (PWAs), cable connectors, or fuses, always turn off power to the affected portion of the equipment. After power is removed, allow sufficient time for the power supplies to bleed down before reinserting PWAs.

3 When troubleshooting, remember that FETs and other metal-oxide-semiconductor (MOS) devices may appear defective because of leakage between traces or component leads on the printed wiring board. Clean the printed wiring board and recheck the MOS device before assuming it is defective.

4 When replacing MOS devices, follow standard practices to avoid damage caused by static charges and soldering.

5 When removing components from PWAs (particularly ICs), use care to avoid damaging PWA traces.

TABLE OF CONTENTS

TABLE OF CONTENTS
(Continued)

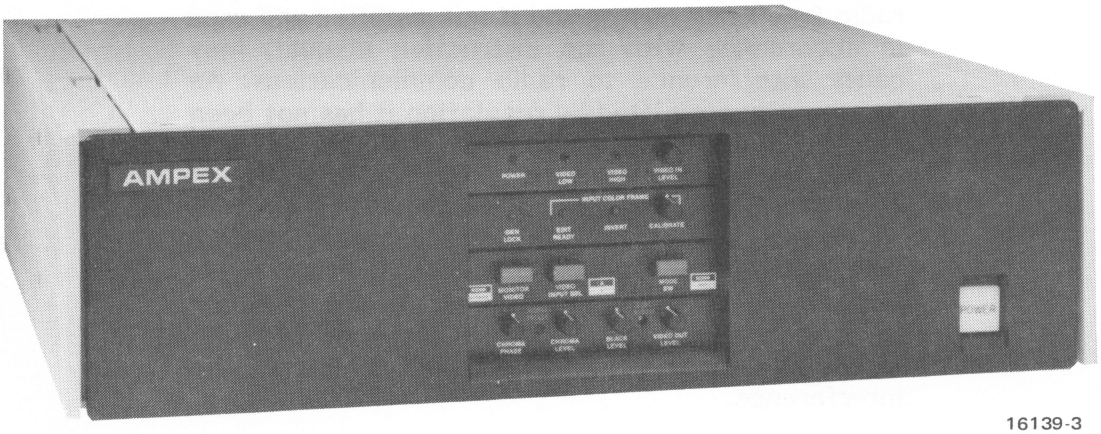
LIST OF ILLUSTRATIONS

LIST OF TABLES

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

TBC-80



16139-3

TBC-80 Digital Time-Base Corrector

SECTION 1
GENERAL INFORMATION

1-1 INTRODUCTION

The four sections of this manual provide information necessary to install and operate the NTSC version of the TBC-80 Digital Time-Base Corrector (DTBC), Ampex Part No. 1451600.

Section 1, *General Information*, is an introduction to the TBC-80, its features and system specifications. Section 2, *Installation*, provides information on TBC-80 physical installation, electrical and interface connections, and checkout procedures required to install and ensure proper operation of the TBC-80. Section 3, *Operation*, describes the TBC-80 operator controls and indicators. Section 4, *Technical Information*, explains theory of operation and alignment procedures necessary to test and maintain the TBC-80 during normal operation.

1-2 GENERAL DESCRIPTION

The following paragraphs describe some of the features, functions, and physical aspects of the system.

1-3 Features

The TBC-80 Digital Time-Base Corrector affords correction over a 14-line window, slow-motion processing to 1-1/2X forward, and recognizable pictures in shuttle to 300 in/s. The TBC-80 also allows dropout replacement from the adjacent line without horizontal shift.

1-4 Functional Description

The TBC-80 Digital Time-Base Corrector (see Figure 1-1) receives off-tape video from a nonsegmented helical-scan video tape recorder. The off-tape video signal is sampled at four times the subcarrier frequency by a sampling clock signal derived from the burst of the incoming off-tape video. The resulting analog video sample goes to an analog-to-digital converter which converts it to an 8-bit binary number corresponding to the analog level. Synchronous to the off-tape timing, this digital data is written sequentially into memory. The stored data is subsequently read out of memory in the same sequence as it is written. The read timing is derived from the station reference video and the output data is synchronous to the reference video. The 8-bit data is converted to an analog level. These samples are filtered to provide the video signal. Blanking and sync are inserted on the resultant video to form the composite video signal.

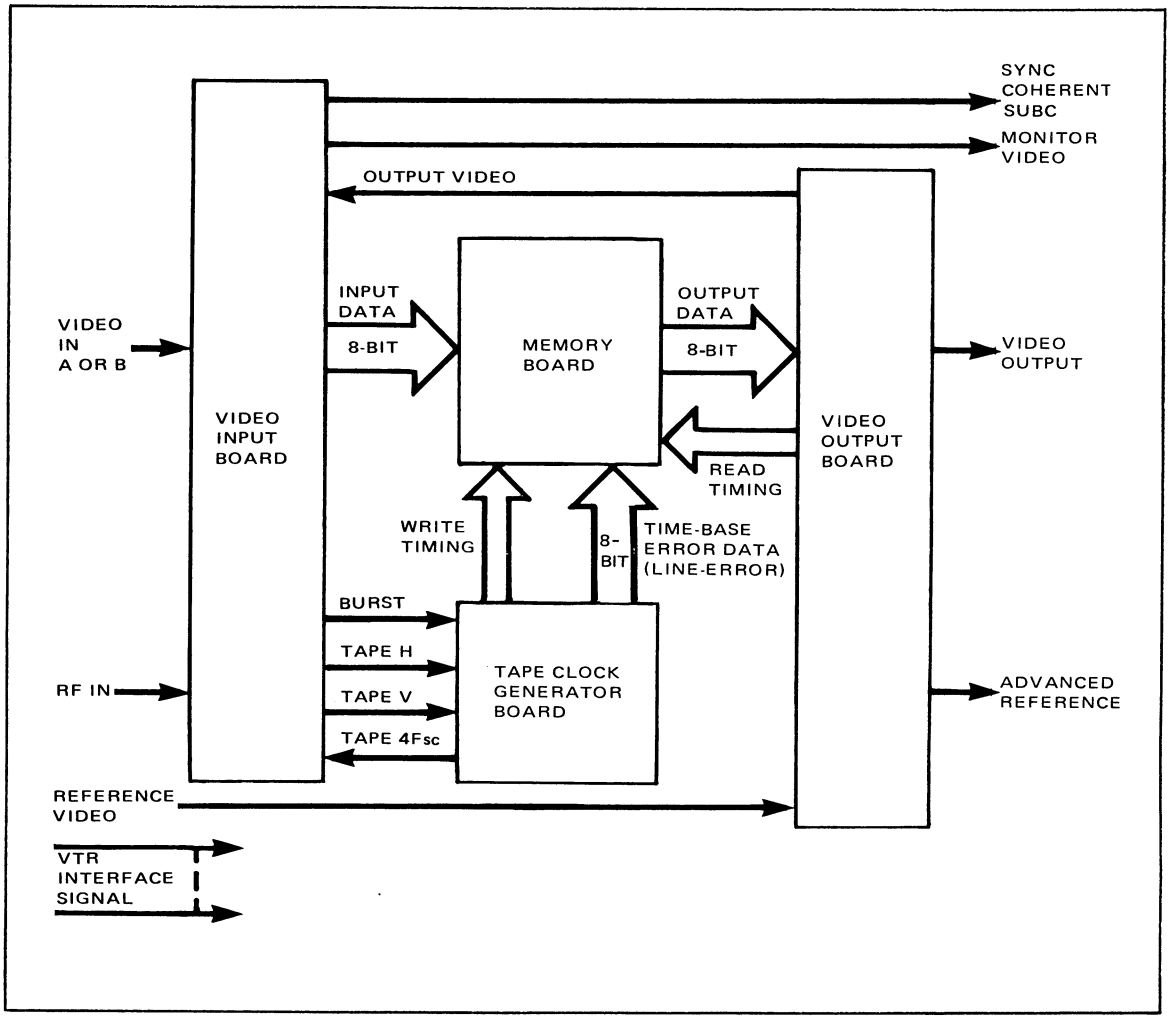


Figure 1-1. TBC-80 Overall Block Diagram

1-5 Physical Description

The TBC-80 is a self-contained unit that includes a power supply. The unit is housed in its own cabinet. The electronic circuits are contained on four individual printed wiring assemblies (PWAs) which plug into a Motherboard PWA. Table 1-1 is a listing of the individual PWAs and their Ampex part numbers. The interface connectors are located at the rear of the cabinet and are mounted directly on the Motherboard PWA.

1-6 TYPICAL APPLICATIONS

The TBC-80 Digital Time-Base Corrector is a compact, economical, high-performance time-base corrector for use with SMPTE C, SMPTE U, and SMPTE H VTRs. The TBC-80 is ideally suited as a companion to the AMPEX VPR-80. Additionally, the TBC-80 allows switch-selectable operation of the AMPEX VPR-80

Table 1-1. TBC-80 Printed Wiring Assemblies

Ampex Part No. 1451601, NTSC Kit:	
A1	Video Input PWA 1451641
A2	Tape Clock PWA 1451643
A3	Memory PWA 1451646
A4	Video Output PWA 1451649

and SMPTE U-format (3/4 in.) or H-format (1/2 in.) VTR when dubbing from two sources. Interconnections are described in detail in Section 2, *Installation.*

1-7 SPECIFICATIONS

Specifications and performance characteristics of the TBC-80 Digital Time-Base Corrector are listed in Table 1-2. These specifications are subject to change without notice or obligation.

Table 1-2. TBC-80 Specifications

Physical Characteristics	
Height:	5.968 in. (151.59 mm)
Width:	20.80 in. (528.32 mm)
Length:	17 in. (431.80 mm)
Weight:	18 kg (40 lbs)
Operating Temperature:	0° to +40° C
Operating Humidity:	10% to 90% relative (non-condensing)
Power Requirements	
Input Power:	50 Hz to 60 Hz, single phase, 150W 90 Vac to 140 Vac or 190 Vac to 250 Vac
System Interface	
Video In A and B:	1 Vp-p, 75Ω
Reference Video In:	1 Vp-p, 75Ω
RF Input:	0.1V to 2.0V
VTR Interface Signals:	Step back, step back 2, sync retard, playback vertical, fast shuttle, edit mute, slow-motion, dropout pulse, head switch/vertical dropout, 2H gate, step forward sync head process, zero offset.

(Continued next page)

Table 1-2. TBC-80 Specifications (Continued)

System Interface (Continued)	
Video Out I:	1.0 Vp-p composite 75Ω
Video Out II:	1.0 Vp-p composite 75Ω 0.7 Vp-p non-composite 75Ω
Monitor Video Out:	1.0 Vp-p composite 75Ω
Advanced Reference Out:	Black burst locked eight lines in advance of the reference generator. 0.3V, 75Ω
Sync Coherent Subcarrier Out:	2.0V subcarrier, 75Ω
Operational Characteristics	
Bandwidth:	Flat to 4.2 MHz, ±0.5 dB
*Signal-to-Noise Ratio:	56 dB
**Differential Phase:	2°
**Differential Gain:	2%
Transient Response (2T pulse and bar K factor):	1%
Correction Range:	±8 horizontal lines
Output Jitter:	±2.5 ns color; ±10 ns monochrome

*VTR-TBC system signal-to-noise ratio is determined primarily by VTR performance.

**Defined as the degradation to the differential gain of the input video signal, measured with ramp and subcarrier amplitude equal to that of the color burst.

SECTION 2
INSTALLATION

2-1 INTRODUCTION

The TBC-80 Digital Time-Base Corrector can be installed by the customer. This section of the manual provides the procedures required to do so. The following paragraphs describe physical set up, electrical and interface connections, checkout and system verification procedures necessary to ensure proper installation. To assist in troubleshooting equipment malfunctions detected at the time of installation, references are included to applicable paragraphs.

2-2 UNPACKING

The TBC-80 is shipped from the factory in a specially constructed packing case. Exercise caution in unpacking to prevent damage to the cabinet finish or accessory parts. Check the contents of the packing case and packing materials for accessory items. Check all items against the packing list to ensure the shipment is complete. Carefully examine the contents for damage that may have occurred during shipment. Notify the carrier and the Ampex representative of any shortage or damage.

2-3 INSTALLATION CONSIDERATIONS

The following paragraphs describe location and equipment requirements for installation and operation of the TBC-80.

2-4 Location

The TBC-80 should be located in a well-ventilated and relatively dust-free environment. The area should not be close to any strong electromagnetic fields. Common sources of interference include fluctuating loads (such as heavy-duty transformers and motors) and radio transmitting equipment. The unit should be mounted in a cabinet that is located in a vibration-free environment. Figure 2-1 shows physical clearances recommended to allow for air flow and signal connections at the connector panel.

2-5 Cables

Video input and output cables should be Belden No. 8281 coaxial cable or equivalent. The 37-pin D-type connector cable that mates with the TBC-80 VTR interface is shown in Figure 2-2. Coaxial cables and connectors that interface with the TBC-80 are to be supplied by the user.

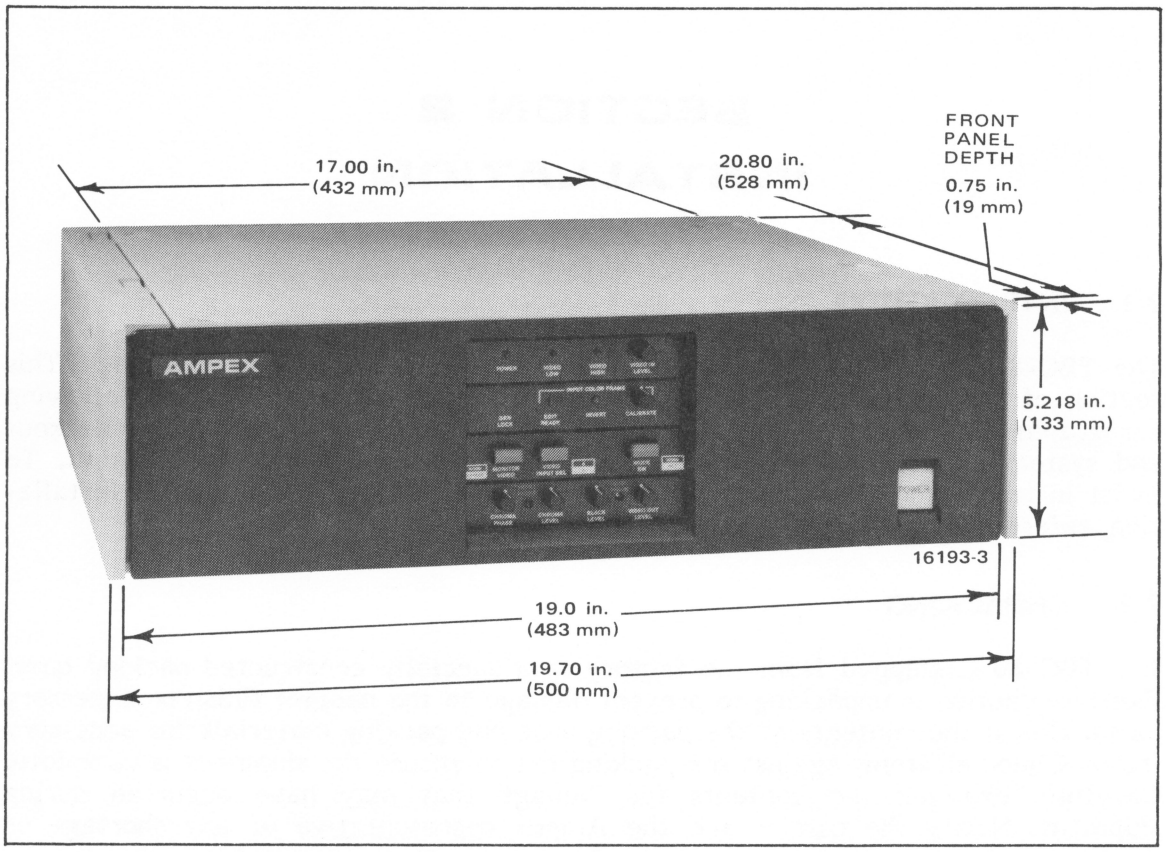


Figure 2-1. Installation Photograph, TBC-80 DTBC

2-6 Tools and Test Equipment

Table 2-1 is a listing of recommended tools and test equipment for installing and maintaining the TBC-80.

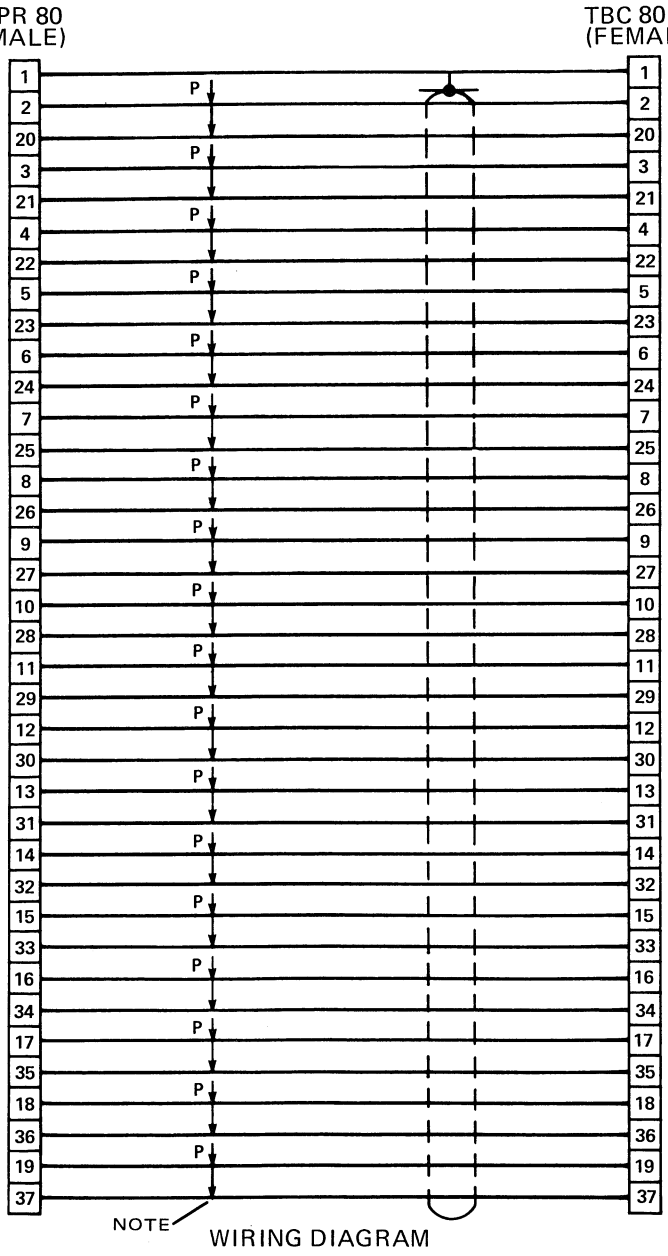
2-7 Power Requirements

95 Vac to 140 Vac or 190 Vac to 250 Vac; single-phase, three-wire, 50 Hz to 60 Hz, 150W

To select the appropriate voltage, remove the jumper plug located on the rear panel and reinsert it so that the proper line voltage is displayed in the cover when the jumper plug is in place on the rear panel (see Figure 2-3).

2-8 Input/Output Connections

All connections to the TBC-80 are made to BNC-type connectors and a 37-pin D-type connector located on the rear panel. Figure 2-3 is a view of the TBC-80 rear panel showing the location of power and signal connectors. Table 2-2 is a list of the BNC-type signal connectors and their functions. Table 2-3 is a list of the 37-pin D-type signals and functions.



NOTES: 1. TWIST 3-4 TURNS PER INCH.

2. CABLE IS BELDEN; TYPE 45 WITH SHIELDED DRAIN WIRE TO PIN 1. MALE CONNECTOR IS BELDEN; RS-449 SERIES D, 37 POSITION. FEMALE CONNECTOR IS BELDEN; RS-449 SERIES D, 37 POSITION.

Figure 2-2. Typical TBC-80 Connector Cable

Table 2-1. Recommended Tools and Test Equipment

Equipment	Type/Functions
Digital Voltmeter	Dc voltage accuracy to four places in the 0-20V range (HP 3465).
Oscilloscope	Dual-channel, 50 MHz bandwidth, 5 ns/div, 5 mV/div, A+B display mode, delayed sweep (Tektronix 465).
Vectorscope	Composite video and vector displays, differential gain and phase measurement, external and internal phase reference (Tektronix 520).
Signal Sources	Color bars, color black (switchable R-Y, B-Y components) variable setup level, 0-50% APL flat field, locked/unlocked subcarrier, modulated/unmodulated ramp, unmodulated stairstep (Tektronix 140 series).
Color Video Monitor	Standard monitor for viewing stable color bars (Tektronix 650).
Dropout Test Tape	For C — format, Ampex Part No. 498625.
Extender Card	Ampex Part No. 1451725 (supplied).
Tuning Tool	AF — 12H (Technitool).

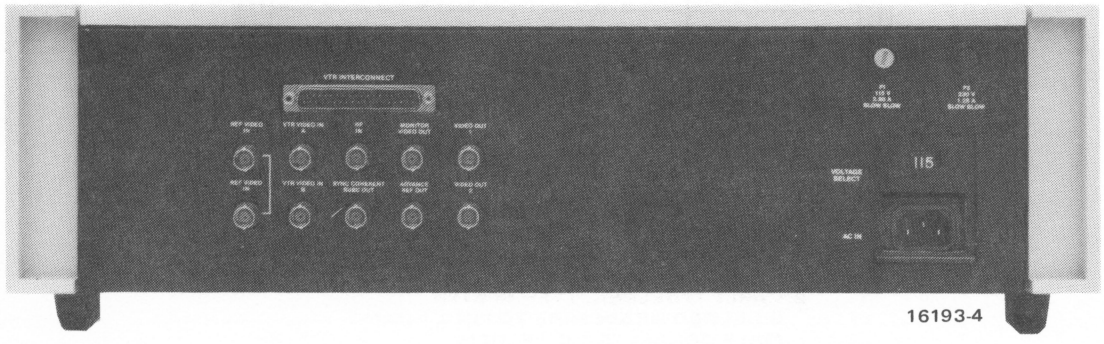


Figure 2-3. TBC-80, Rear Panel

Table 2-2. Rear Panel BNC Connector Signal Descriptions

Signal	Description
Video In A and B:	1 Vp-p, 75Ω
Reference Video In:	1 Vp-p, 75Ω
RF Input:	0.5V to 2.0V (for dropout compensation)
Video Out I:	1.0 Vp-p composite, 75Ω
Video Out II:	1.0 Vp-p composite or 0.7 Vp-p non-composite, 75Ω
Monitor Video Out:	1.0 Vp-p composite, 75Ω
Advanced Reference Out:	Black burst locked eight lines in advance of the reference generator. 0.3V, 75Ω
Sync Coherent Subcarrier Out:	1.0V subcarrier, 75Ω

Table 2-3. Rear Panel 37-Pin D-Type Connector Signals

Pin	Signal	Pin	Signal
1	Ground	20	Step Back 1
2	Ground	21	Step Back 2
3	Ground	22	(not used)
4	(not used)	23	Sync Retard
5	Edit Mute	24	Tachometer
6	Fast Shuttle	25	Head Switch/Vertical
7	Ground		Dropout
8	Ground	26	Playback Vertical
9	Zero Offset	27	Slow Motion
10	Ground	28	2H Gate
11	Ground	29	Dropout Pulse
12	Up/Down	30	Sync Head Processor
13	(not used)	31	Step Forward 1
14	Ground	32	Step Forward 2
15	Ground	33	(not used)
16	Ground	34	(not used)
17	Ground	35	(not used)
18	Ground	36	(not used)
19	Ground	37	(not used)

2-9 SETUP

The following paragraphs describe the initial procedures required to install the TBC-80.

2-10 TBC-80 To VPR-80 Installation

Prepare the TBC-80 for operation with the VPR-80 as follows:

STEP 1 Ensure that TBC-80 and VPR-80 power is off.

STEP 2 Interconnect TBC-80 with the VPR-80 as shown in Figure 2-4.

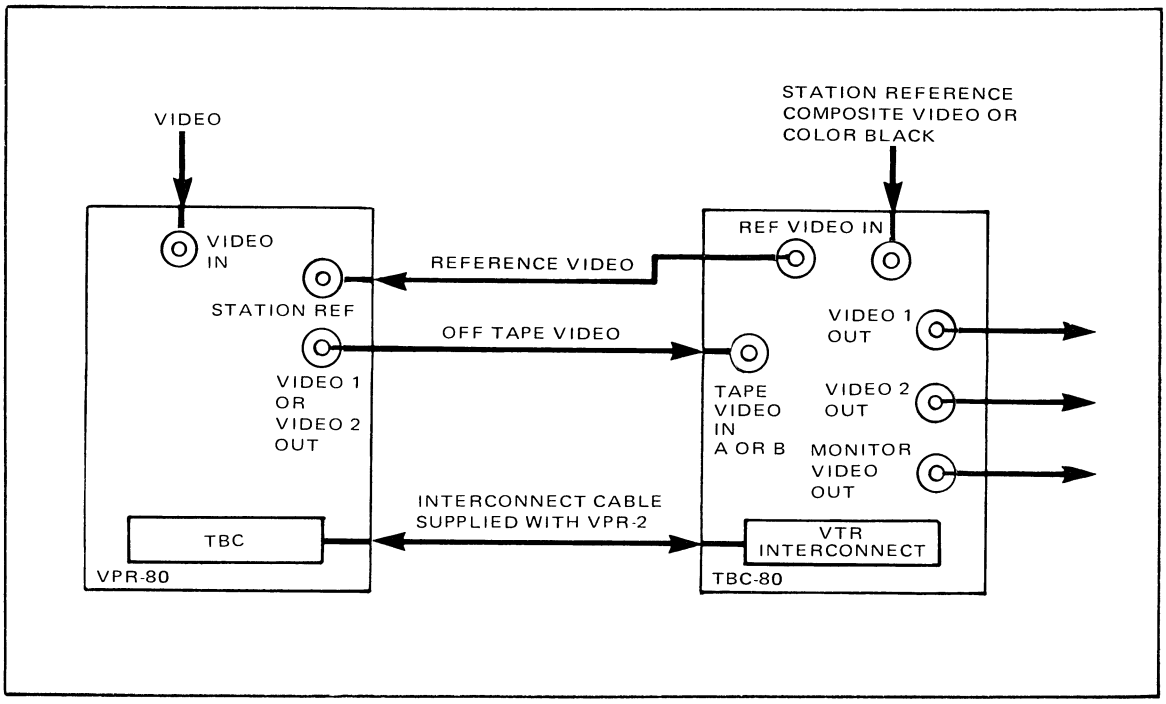


Figure 2-4. TBC-80 Interconnections

STEP 3 Set MODE switch on front panel of TBC-80 to NORM position.

STEP 4 Switch power on to TBC-80 and VPR-80.

STEP 5 Connect a waveform monitor or oscilloscope to video output connector of VPR-80 using a 75Ω terminator at input. Verify that signal level is 1.0 Vp-p with input color bar signal.

STEP 6 Record and play back a 1-minute segment of color-bar signal. During playback, signal should have a 1.0 Vp-p amplitude with correct chroma levels. If color-bar signal is not correct, adjust VPR-80.

STEP 7 Connect waveform monitor or oscilloscope to VIDEO OUT I on TBC-80 using a 75Ω termination at input. Check that burst and sync signals are 0.3 Vp-p; if they are not, see paragraph 4-11 for information on adjustment of these levels.

STEP 8 Proceed with *Normal Operation* procedures described in paragraph 3-6.

2-11 TBC-80 To Single-Wire Heterodyne VTR Installation

Prepare the TBC-80 for operation with a single-wire heterodyne VTR as follows:

STEP 1 Ensure that TBC-80 and VTR power is off.

STEP 2 Interconnect TBC-80 with VTR as shown in Figure 2-5.

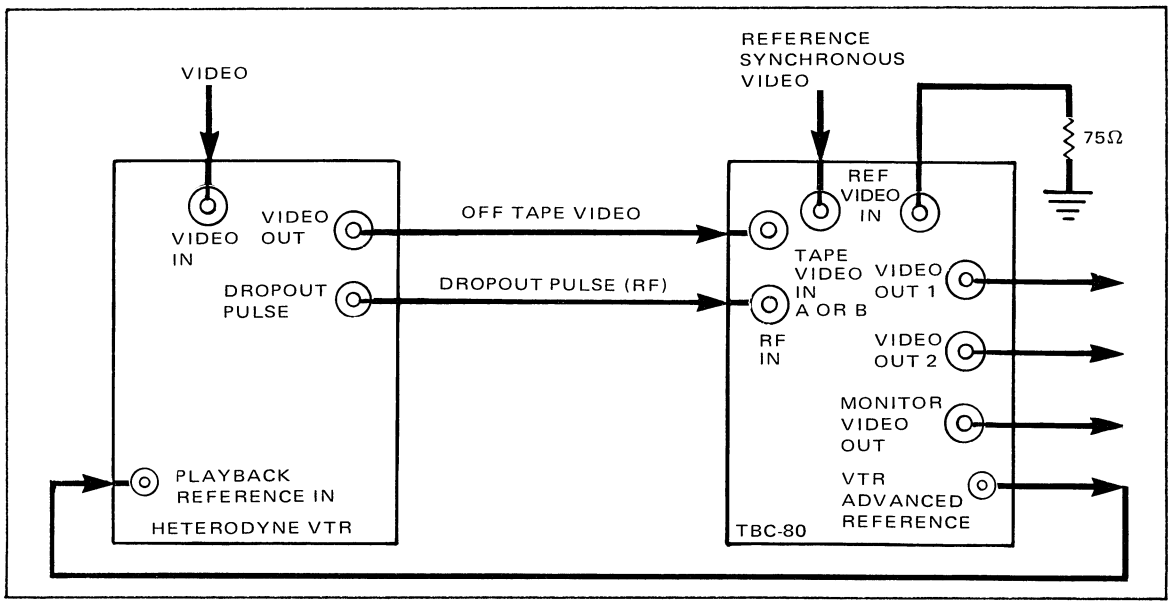


Figure 2-5. TBC-80 One-Wire Heterodyne Interconnections

STEP 3 Set MODE switch on front panel of TBC-80 to HET position.

STEP 4 Set heterodyne one-wire/two-wire switch S1 on Video Input PWA to the one-wire position.

STEP 5 Apply power to TBC-80 and VTR.

STEP 6 Connect a waveform monitor or oscilloscope to video output connector of VTR using 75Ω terminator at input. Verify signal level is 1.0 Vp-p with input color bar signal.

STEP 7 Record and play back a 1-minute segment of color-bar signal. During playback, signal should have a 1.0 Vp-p amplitude with correct chroma levels. If color-bar signal is not correct, adjust VTR.

STEP 8 Connect waveform monitor or oscilloscope to VIDEO OUT I on TBC-80 using a 75Ω termination at input. Check that burst and sync signals are 0.3 Vp-p; if they are not, see paragraph 4-11 for information on adjustment of these levels.

STEP 9 Proceed with *Normal Operation* procedures of paragraph 3-6.

2-12 TBC-80 To Two-Wire Heterodyne VTR Installation

Prepare TBC-80 for operation with a two-wire heterodyne VTR using Figure 2-6 and following steps 1 through 3 of paragraph 2-11 above. Set switch S1 on Video Input PWA to two-wire position and proceed with steps 5 through 9 above (paragraph 2-11).

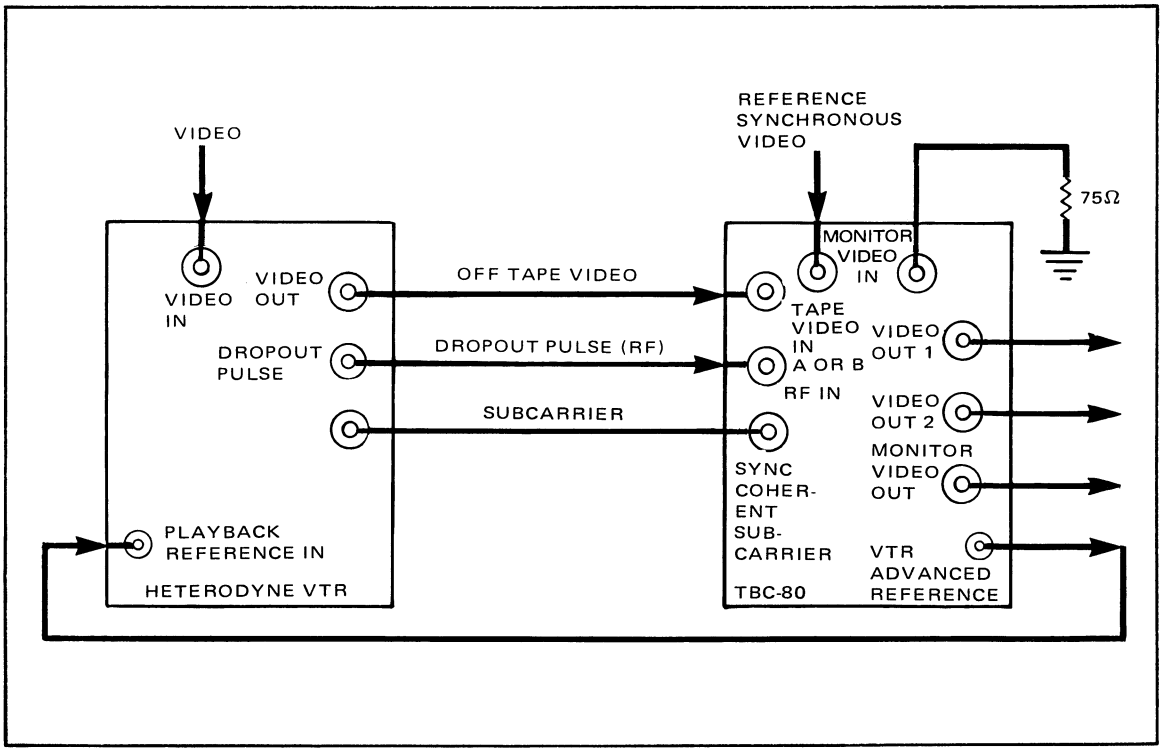


Figure 2-6. TBC-80 Two-Wire Heterodyne Interconnections

2-13 TBC-80 To Heterodyne VTR and VPR-80 Installation

Prepare the TBC-80 for operation with heterodyne VTR and VPR-80 as follows:

STEP 1 Ensure that TBC-80 and VTR power is off.

STEP 2 Interconnect TBC-80 with both VTRs as shown in Figure 2-7.

STEP 3 Set heterodyne one-wire/two-wire switch S1 on Video Input PWA to one-wire position.

STEP 4 Apply power to TBC-80 and both VTRs.

STEP 5 Connect a waveform monitor or oscilloscope to video output connector of VPR-80 using a 75Ω terminator at input. Verify that signal level is 1.0 Vp-p.

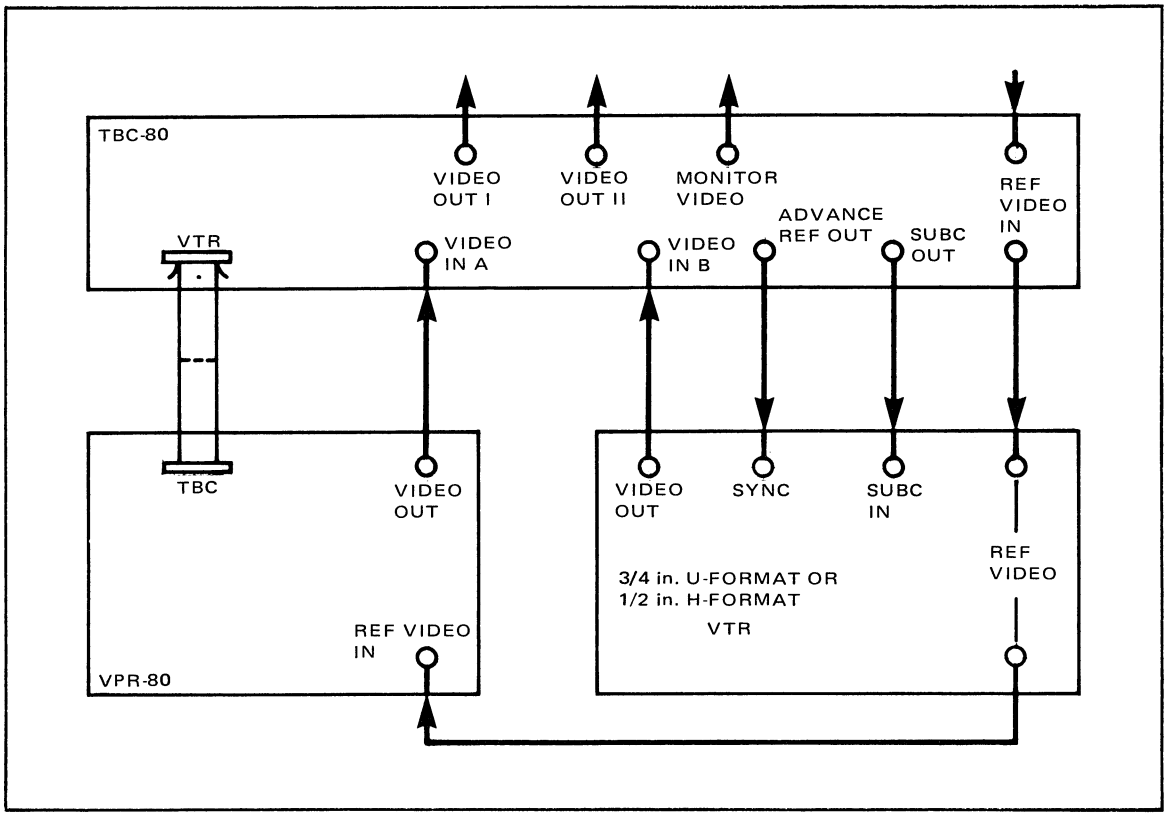


Figure 2-7. TBC-80 to VPR-80 and Heterodyne VTR Interconnections

STEP 6 Record and play back a 1-minute segment of color-bar signal. During playback, signal should have a 1.0 Vp-p amplitude with correct chroma levels. If color-bar signal is not correct, adjust VPR-80.

STEP 7 Connect a waveform monitor or oscilloscope to video output connector of heterodyne VTR using a 75Ω terminator at input. Verify that signal level is 1.0 Vp-p.

STEP 8 Record and play back a 1-minute segment of color-bar signal. Color-bar signal during playback should have a 1.0 Vp-p amplitude with correct chroma levels. If signal is not correct, adjust heterodyne VTR.

STEP 9 Connect waveform monitor or oscilloscope to video-out I on TBC-80 using a 75Ω termination at input. Check that burst and sync signals are 0.3 Vp-p. Switch input signals by setting VIDEO INPUT SEL switch on front panel to A or B position and the MODE SW switch to NORM/HET position. If burst and sync levels are not 0.3 Vp-p, see paragraph 4-11 for information on adjustment.

STEP 10 Proceed with *Normal Operation* procedures of paragraph 3-6.

SECTION 3
OPERATION

3-1 INTRODUCTION

This section provides a description of the TBC-80 controls. Only those controls or functions accessable to the operator are described.

3-2 PRIMARY CONTROLS AND INDICATORS

Table 3-1 is a listing of front panel controls/indicators and their functions. (See also Figure 3-1.)

Table 3-1. Primary Operating Controls and Indicators

Control/Indicator	Description
POWER switch	Applies primary power to TBC-80.
POWER indicator	Lighted when +5 Vdc is available.
VIDEO LOW indicator	Lighted when nominal input signal level is less than 0.8 Vp-p.
VIDEO HIGH indicator	Lighted when nominal input signal level is greater than 1.25 Vp-p.
VIDEO IN LEVEL potentiometer	Provides ±3 dB range of adjustment for input video level. Used in special cases in conjunction with VIDEO LOW and VIDEO HIGH indicators.
GEN LOCK indicator	Lighted when an acceptable gen lock signal is supplied to TBC-80.
INPUT COLOR FRAME:	
EDIT READY indicator	Indicates TBC-80 properly color framed.
INVERT indicator	Indicates input sch deviation in excess of ±90°.
CALIBRATE potentiometer	Calibrates edit ready indicator for a specific sch phase (detent = RS170A).

(Continued next page)

Table 3-1. Primary Operating Controls and Indicators (Continued)

Control/Indicator	Description
MONITOR VIDEO switch	Selects monitor video output signal. In NORM (normal) position, processed TBC-80 video is selected. In BYPASS position, video input from VTR is routed to monitor video output.
VIDEO INPUT SEL switch	Selects tape video input signal from tape video A or B input jack.
MODE SW switch	Selects processing of direct color video in NORM position or heterodyne video in the HET (heterodyne) position.
CHROMA PHASE potentiometer	Adjusts phase of picture chrominance information with respect to color burst (±25°) during playback.
HORIZ PHASE switch	Adjusts output sync tuning relative to reference sync in steps of subcarrier cycles.
CHROMA LEVEL potentiometer	Adjust chroma level ±3 dB.
BLACK LEVEL potentiometer	Adjusts difference level between black and blanking levels.
SUBC PHASE potentiometer	Adjusts color subcarrier phase of video output signal with respect to its reference subcarrier with a full cycle.
VIDEO OUT LEVEL potentiometer	Adjusts level of video output signal (nominal 1.0V).

3-3 SECONDARY CONTROLS AND INDICATORS

Table 3-2 is a listing of PWA card-edge controls and indicators and their functions. (See also Figure 3-2.)

3-4 PRELIMINARY SETUP

Use the following tests to verify operation of the TBC-80. Each test requires that the initial installation procedures be completed and the unit be powered on.

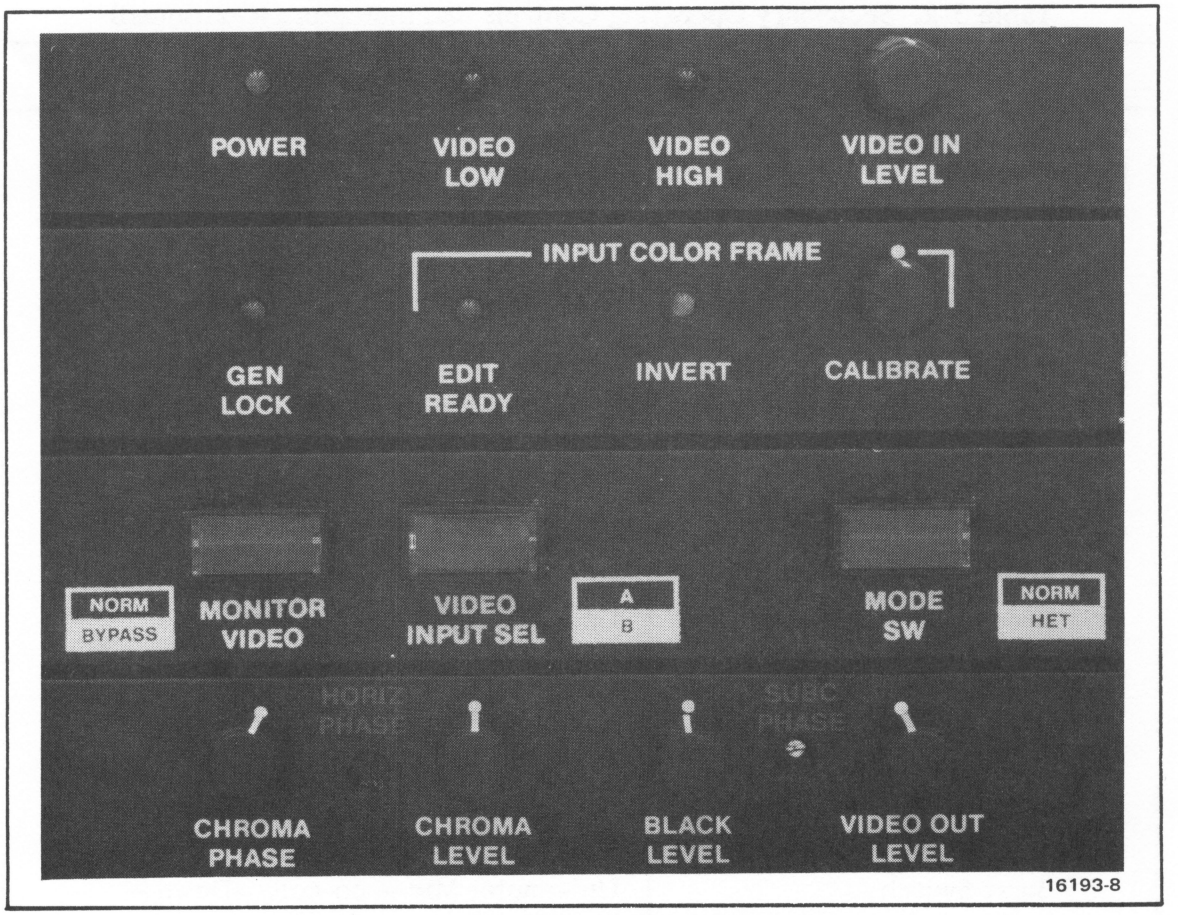


Figure 3-1. TBC-80 Primary Controls

Table 3-2. Secondary Operating Controls and Indicators

Control/Indicator	Description
Video Input PWA:	
S1 Heterodyne 1-wire/2-wire	In heterodyne operation, selects between 1-wire, 2-wire operation.
Tape Clock PWA:	
R224 Phase Comparator Center	Maintenance adjustment.
R223 Heterodyne Burst/Sync Phase	Maintenance adjustment.
R222 Vertical Delay	Maintenance adjustment.

(Continued next page)

Table 3-2. Secondary Operating Controls and Indicators (Continued)

Control/Indicator	Description
Tape Clock PWA: (Continued)	
DS1 Search Indicator	Indicates extended search VCO operation.
S1 Tape VCO Int/Ext	Selects between TBC-80 internal and external (VPR-80) VCO switching.
Memory PWA:	
DS1 Memory Center Indicators	Indicate memory read-write condition. Left read faster than write; right write faster than read.
S3 Horizontal Position	Nominal positions.
S2 Velocity Compensator	Up - enable; Down - disable.
S1 Dropout Compensator	Up - enable; Down - disable.
Video Output PWA:	
S1 Vertical Blanking — wide	Adjustable width vertical blanking heterodyne mode.
S2 Vertical Blanking — normal	Adjustable width vertical blanking Norm, SMPTE A or C mode.
S5 Burst Switch	Up — auto; Mid — on-color; Down — monochrome.
R117 H Blanking Leading Edge	Non-RS170A reference input.
R118 H Blanking Trailing Edge	Maintenance adjustment.
R119 Input Sync/Burst	Maintenance adjustment.
R437 Burst Phase	Maintenance adjustment.
R437 Burst Phase	Maintenance adjustment.
R439 Output Sync/Burst	Allows adjustment for non-RA170A output.

3-5 System Phase Adjustment

To permit synchronous operation of VTR and the TBC-80 with the station reference, adjust TBC-80 to match the phase of the external station reference as follows:

STEP 1 Connect a dual-trace oscilloscope to video output of external signal source and video output of TBC-80. Terminate both video signals with a 75Ω resistor at scope.

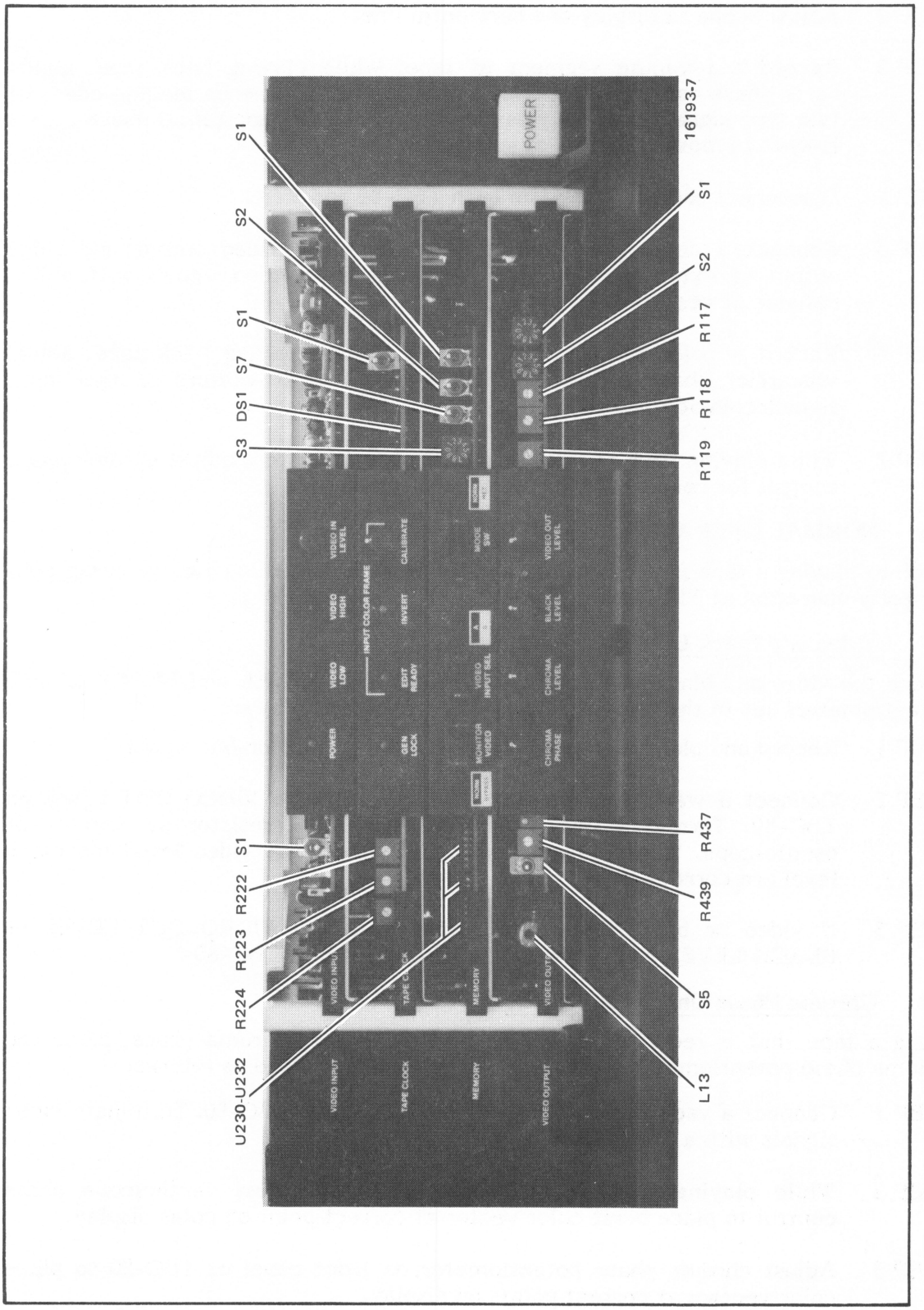


Figure 3-2. TBC-80 Secondary Controls

STEP 2 Adjust scope to display one horizontal line.

STEP 3 Record a 1-minute segment of tape. While playing back tape, adjust horiz phase control on TBC-80 control panel to line up leading edges of two sync signals as closely as possible. (Adjusting horizontal phase causes H-sync to move in cycles of subcarrier.)

STEP 4 Disconnect oscilloscope from both TBC-80 and VTR.

STEP 5 Connect a dual-input vectorscope to TBC-80 video output and video output of external reference. Terminate both video signals with a 75Ω resistor at vectorscope.

STEP 6 Record a color-bar segment of tape. While playing back tape, adjust subcarrier phase control on TBC-80 until burst vectors of two input signals coincide.

STEP 7 While playing back recording made in previous step, adjust chroma phase control for coincidence of color-bar vectors.

3-6 NORMAL OPERATION

Prior to playing a tape for correction, use the steps in the following two paragraphs to verify operation of TBC-80.

3-7 Video and Black Level Unity Adjustments

Check the video and black levels with the VIDEO OUT LEVEL and BLACK LEVEL potentiometers set to the unity position and proceed as follows:

STEP 1 Record and play back a 1-minute segment of a color-bar signal.

STEP 2 Connect a waveform monitor or oscilloscope to VIDEO OUT I jack on TBC-80. Terminate video signals with a 75Ω resistor at monitor or oscilloscope. While playing back tape, check that video level and black level are correct.

STEP 3 If video or black levels are incorrect, adjust VIDEO OUT LEVEL or BLACK LEVEL potentiometers on front panel of TBC-80.

3-8 Chroma Phase Unity Adjustment

Using a tape that is recorded with the correct burst-to-chroma phase, place the chroma phase potentiometer in the unity position and proceed as follows:

STEP 1 Connect a vectorscope to VIDEO OUT I jack on TBC-80. Terminate video signals with a 75Ω resistor at vectorscope.

STEP 2 While playing back tape to be corrected, adjust vectorscope phase control to place burst color vector at correct point on polar display.

STEP 3 Adjust chroma phase potentiometer on front panel of TBC-80 to place color vectors at correct points on display.

SECTION 4
TECHNICAL INFORMATION

4-1 INTRODUCTION

Section 4 describes the functional operation of the TBC-80 and the interrelationship of the PWAs associated with the system. This section also contains block diagrams of the overall system and individual PWAs that comprise the TBC-80.

4-2 TECHNICAL DESCRIPTION

4-3 Overall Functional Description

The TBC-80 provides correction of time-base errors of non-segmented helical-scan videotape recorders over a range greater than 12 horizontal lines. A time-base error within this range can be corrected to within 2.5 ns for color signals and to within 40 ns for monochrome signals. When used with the Ampex VPR series production recorders, the TBC-80 also provides color processing to 1-1/2X forward and monochrome pictures at shuttle speeds to 300 in/s. Figure 4-1 is a block diagram of the TBC-80. The following paragraphs describe the overall signal flow and operation of individual board assemblies of the system.

The Video Input PWA receives the off-tape video from a nonsegmented helical-scan video tape recorder. The Video Input PWA buffers the off-tape video and clamps it to a zero-volt reference level. The video input also strips burst, horizontal sync, and vertical sync information from the input video. The color burst, tape-H, and tape-V are sent to the Tape Clock Generator PWA. The clamped video signal is sampled at four times the subcarrier frequency by a sampling clock signal derived from the burst of the incoming off-tape video. The resulting analog video sample goes to an A/D converter which converts it to an 8-bit binary number corresponding to the analog level. The resulting 8-bit data is sent to the Memory PWA.

The Memory PWA receives the 8-bit video samples, tape-synchronous write timing, and time-base error data from the Tape Clock Generator PWA, and reference-synchronous read timing from the Video Output PWA. The Memory PWA contains a 16-line random access memory, buffer registers, and associated read-write control circuits, which store the incoming data sequentially into the random access memory synchronous to the tape-derived timing. The memory provides an 8-line delay of the data before it is read from the 16-line memory in the same order as it is written. The read timing is derived from the station reference video and the output data is thus synchronous to the reference video. The output data is sent to the dropout compensator circuits, the velocity compensator circuits, and subsequently to the Video Output PWA.

The Video Output PWA receives the 8-bit digital video data and the station reference video. The station reference video goes to the reference sync generator circuits, which provide the read timing to the memory, to the advanced reference output from the TBC-80, and to the Video Output PWA's internal timing signals. The 8-bit data from the Memory PWA goes to a D/A converter where it is converted to an analog level. These samples are filtered to provide the resultant video signal. Blanking and sync are inserted on the resultant video to form the composite video signal that is provided at the output of the TBC-80.

4-4 Video Input PWA

The Video Input PWA (Figure 4-2) receives RF dropout, video in A, and video in B signals from the video tape recorder. The video input also receives sync coherent subcarrier from the Tape Clock Generator PWA and composite video from the Video Output PWA. The video input provides selection of either video-in A or B signal for processing by the TBC-80. The selected video input signal goes to the monitor video switching and to the input amplifier. The monitor video switch provides selection of either the input or output video signal as the buffered monitor video out.

The selected off-tape video is amplified to standard amplitude levels and clamped to a zero-volt reference. In direct color, this signal goes to the A/D converter circuits and tape timing circuits.

During slow-motion the color processing circuits maintain the correct chroma phasing to simulate the four-field color frame of the NTSC signal. This is done by separating the chrominance information from the luminance and then reinserting the inverted or noninverted chrominance via an electronic switch.

When used in heterodyne mode, the signal is routed to color processing circuits where a sync-coherent chroma reference is established. In a heterodyne mode, color processing circuits strip the chrominance from the selected video signal and demodulate the chrominance with the burst-locked crystal oscillator from the Tape Clock Generator PWA. The chrominance information is then remodulated, using tape-H synchronous subcarrier, and reinserted into the luminance signal to produce a standard signal input to the A/D converter and tape timing circuits.

The video input also strips burst, horizontal sync, and vertical sync information from video. The burst, tape-H, and tape vertical are sent to the Tape Clock Generator PWA. The A/D circuits buffer and clamp the A/D input video. The clamped A/D input video signal is sampled at four times the subcarrier frequency by a sampling clock signal derived from the burst of the incoming off-tape video and goes to an A/D converter which converts it to an 8-bit binary number corresponding to the analog level. The resulting 8-bit data is buffered in an 8-bit latch and, if no dropout is detected, the contents of the latch are enabled to the Memory PWA. Dropout information from the VTR is detected by circuits on the video input. The detected dropout is used to set and enable a latch on video input that provides a binary count of 255 (all 8-bits high) at the output of the data to the Memory PWA. This replaces the data from the A/D converter latches to denote a dropout condition on that line sample.

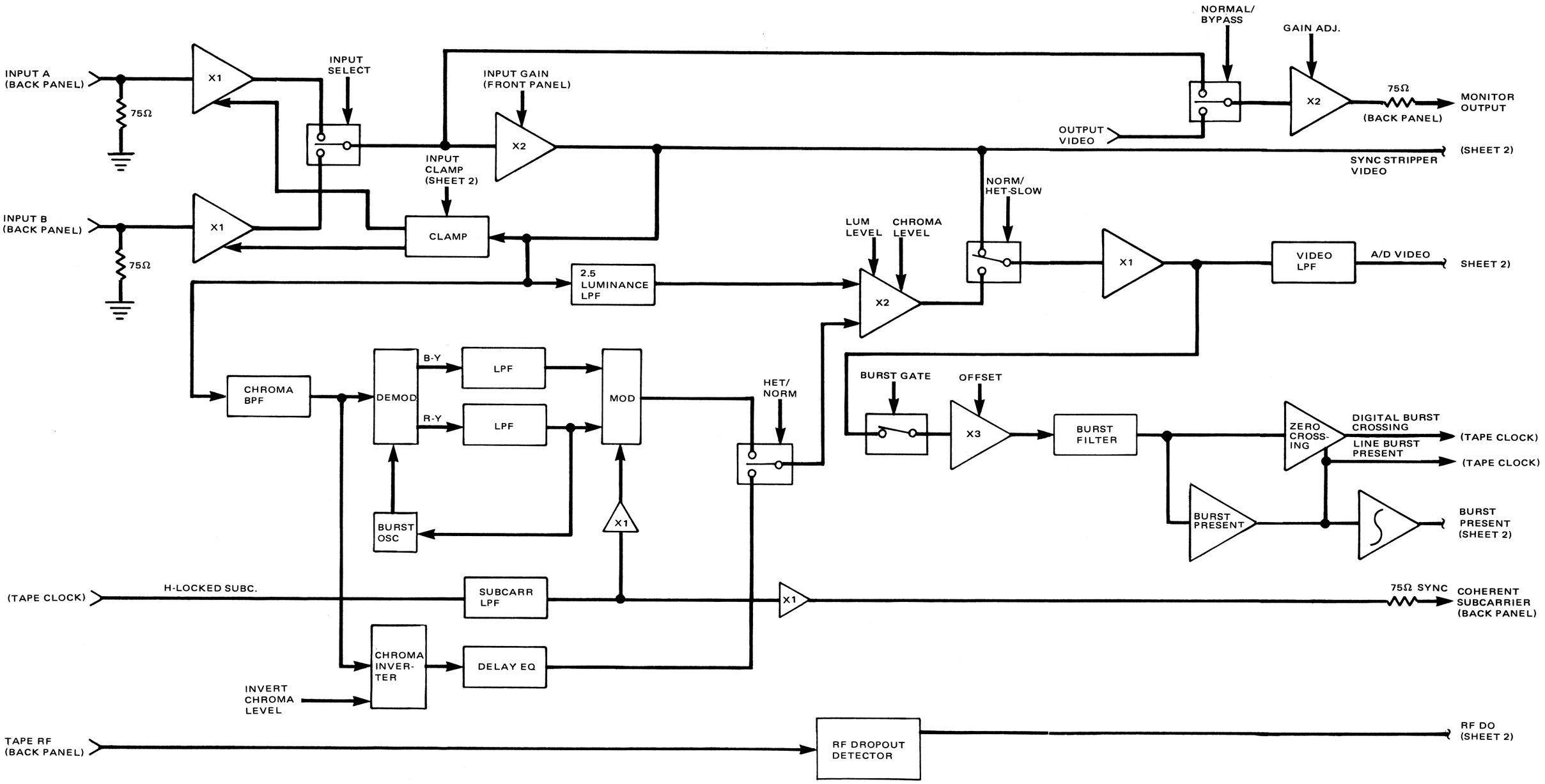


Figure 4-2.
TBC-80 Video Input PWA, Block Diagram
(Sheet 1 of 2)

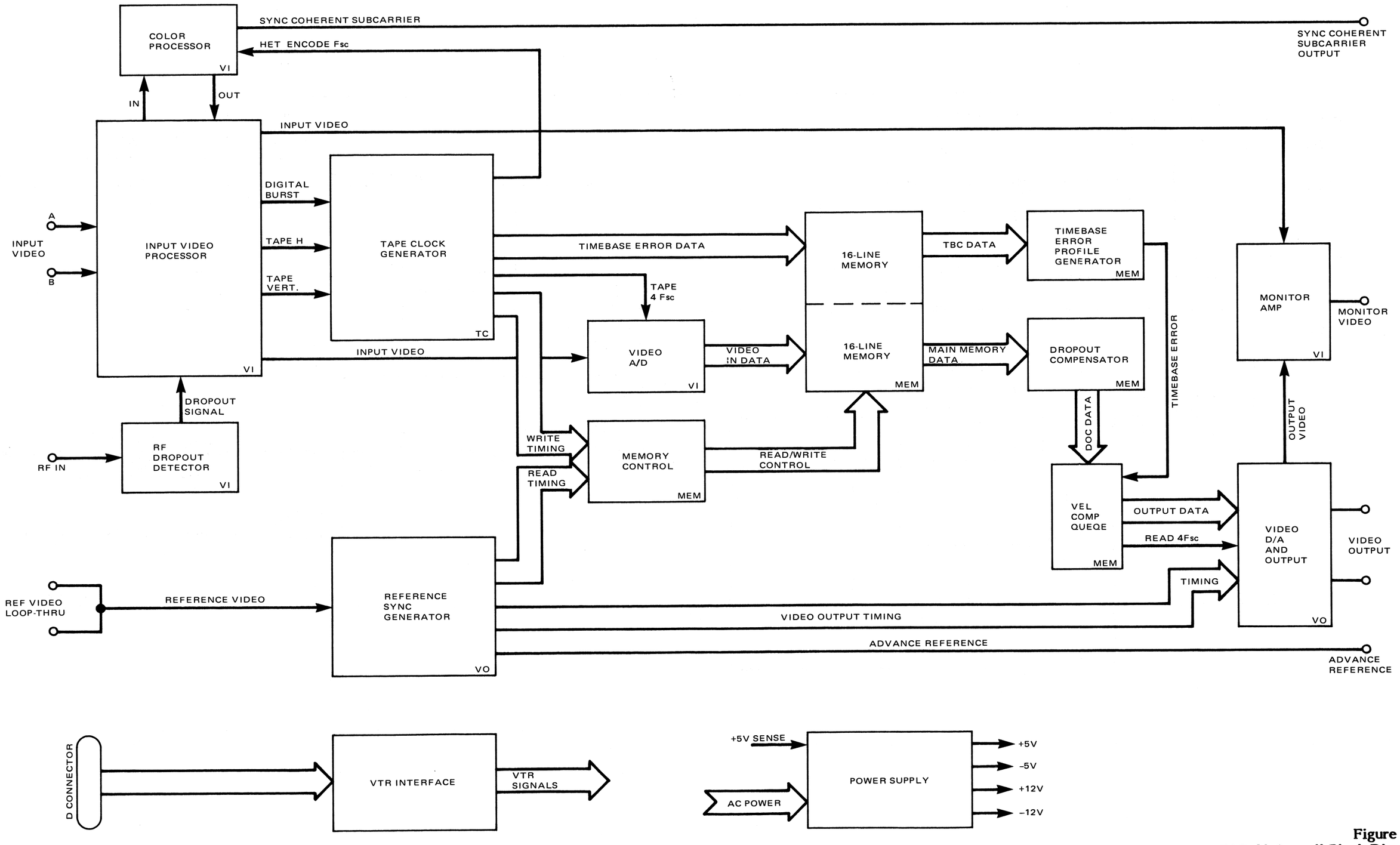


Figure 4-1.
TBC-80 Overall Block Diagram

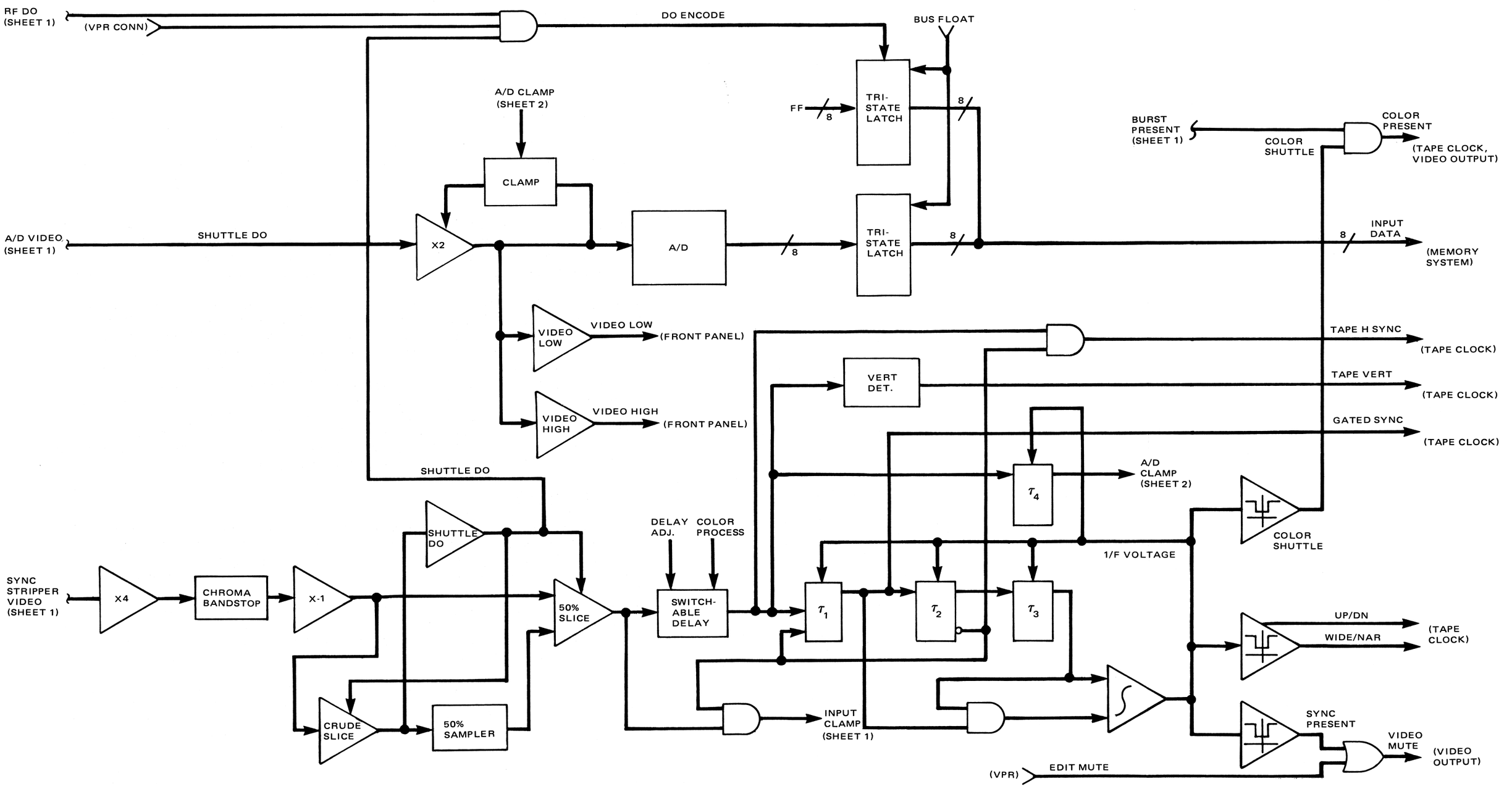


Figure 4-2.
TBC-80 Video Input PWA, Block Diagram
(Sheet 2 of 2)

4-5 Tape Clock PWA

The Tape Clock PWA (Figure 4-3) receives burst, tape-H, and tape vertical from the Video Input PWA and provides the time-base error data and write timing for the Memory PWA. The tape clock also generates the tape 4Fsc signal used by A/D converters on the Input Video PWA. The Tape Clock PWA contains tape vertical and horizontal processing, normal and search VCOs, and VCO error measurement circuits.

The tape vertical processing circuits generate the tape vertical timing and dropout signals. The tape-H processing circuits generate the write-timing and line-error sample to the Memory PWA. The normal and search VCOs generate the tape 4Fsc timing and heterodyne encode Fsc timing as selected via the VCO output circuits.

The normal VCO is locked to the off-tape burst crossing and is selected when the VTR is in normal and slow-motion operation. The search VCO is locked during shuttle operation. The error voltage is generated by a digital phase comparator that detects the difference between the count for a single line interval and the actual arrival of the off-tape horizontal pulse. Thus, the tape horizontal comparator and tape VCO circuits are functionally interdependent. In normal mode, with color present, the tape horizontal comparator compares the phase between the VCO and the burst from the Video Input PWA on a line-by-line basis. The difference signal is ramped to provide the line error voltage which is converted, via an A/D, converter to an 8-bit line error sample. This 8-bit sample is then sent to the Memory PWA where it is stored with the corresponding line video samples.

4-6 Memory PWA

The Memory PWA (Figure 4-4) receives the 8-bit data from the Video Input PWA, tape-synchronous write timing and time-base error data from the Tape Clock Generator PWA, and reference-synchronous read timing from the Video Output PWA. The Memory PWA contains a 16-line random access memory, buffer registers, and associated read-write control circuits. The read-write control circuits provide the timing and addressing operations for the memory circuits. The data is stored sequentially into the random access memory synchronous to the tape-derived timing, and read sequentially from the random access memory synchronous to the reference.

The 8-bit data from the Video Input PWA is received by the write-in buffer, which stores the samples in groups of 13 8-bit samples. The resulting 104-bit word is then written into the 16-line memory. As each line is written into memory, the time-base error is also stored with the data for the corresponding line.

The memory provides an 8-line delay of the data before it is read from the 16-line memory. The data is read from memory in the same order as it is written, in groups of 104 bits at a time. The read timing is derived from the station reference video and therefore the output data is synchronous to the reference video. The 104-bit data output from the 16-line memory goes to a parallel-to-serial converter that converts the 104-bit data to 13 groups of 8-bit data. This 8-bit data from the parallel-to-serial converter is supplied to the dropout compensator circuits before

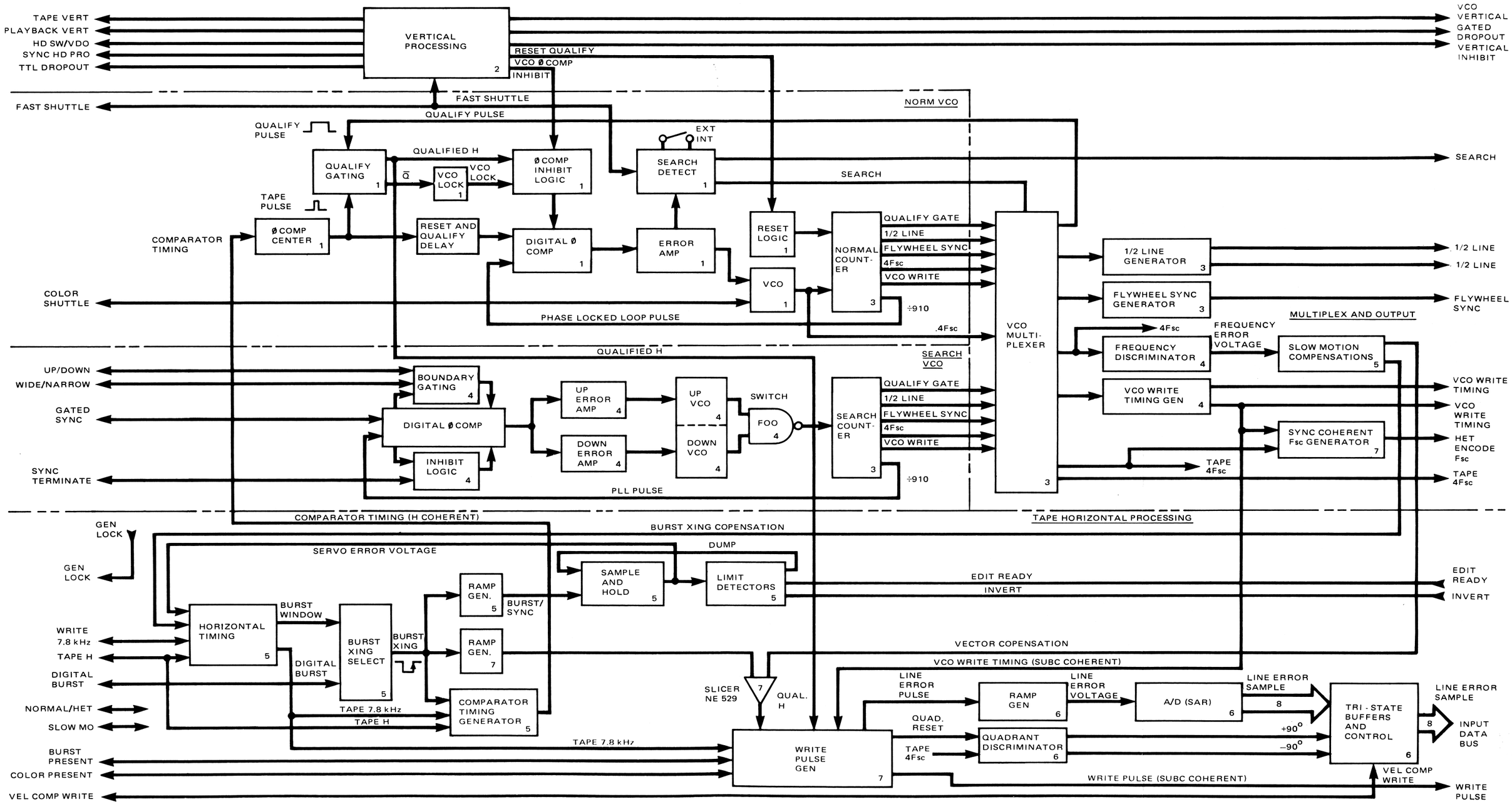


Figure 4-3.
TBC-80 Tape Clock PWA, Block Diagram

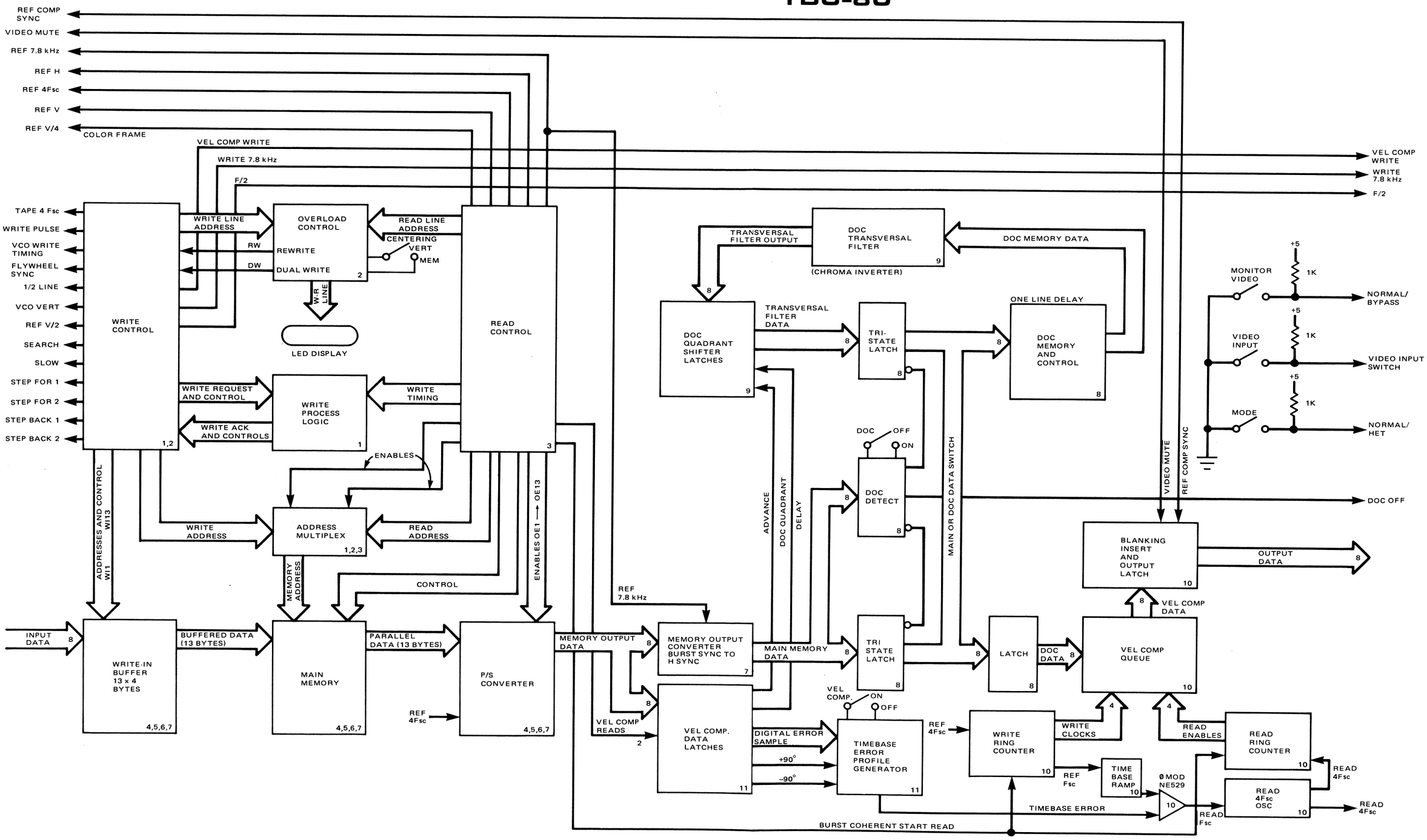


Figure 4-4.
TBC-80 Memory PWA, Block Diagram

passing to the velocity compensator. The dropout compensator recirculates one line of digital video. When dropout compensation is enabled and a video sample of 255 (all ones) is detected, the corresponding data from the previous line is substituted. Otherwise the 8-bit data is passed through to the velocity compensator circuits.

The velocity compensator circuits, when enabled, sample the line error and generate a time-base error signal, which is applied to the 4X subcarrier (4Fsc) read clock. The data into the velocity compensator circuits is written in with the reference 4Fsc timing. The data out of the velocity compensator circuits is read out with the read 4Fsc clock corrected by the time-base error. The data from the velocity compensator goes to the blanking insert and to output latches where reference blanking is inserted into the serial data stream. The output of the latches, an 8-bit data stream, goes to the Video Output PWA.

4-7 Video Output PWA

The Video Output PWA (Figure 4-5) receives the 8-bit data from the Memory PWA and the reference video from the station reference video. The 8-bit data from the Memory PWA is latched into the Video Output PWA by the read 4Fsc clock. The latched data is converted from TTL levels to MECL levels, which go to a digital-to-analog converter. The MECL-level 8-bit data is converted to an analog voltage. These samples are filtered to provide the resultant video signal. Blanking, sync, and burst are inserted on the resultant video to form the composite video signal that is provided at the output of the TBC-80.

The blanking, sync, and burst signals, in addition to the read timing for the Memory PWA, are generated by the reference sync generator circuit. The reference sync generator, on the Video Output PWA, receives the reference video. Reference video is processed to to extract the basic timing signals. The reference video goes to sync and burst stripping circuits.

The output of the sync stripper is sent to a sync generator, which provides the reference horizontal and reference H/2 (7.8 kHz). This sync generator provides all reference timing signals for insertion into the filtered D/A converter signal via the buffer/line drivers.

4-8 SERVICE INFORMATION

This section contains general and system level maintenance procedures, jumper options, and motherboard pin descriptions.

4-9 Preventive Maintenance

The TBC-80 requires no periodic maintenance except normal cleaning. Wipe the front panel with a dry cloth as required. As a confidence check, the operational verification procedures may be performed prior to critical program sessions.

4-10 General Considerations

When performing tests, adjustments, or repairs on the TBC-80 the following general precautions and considerations should be followed.

CAUTION

TO PREVENT POSSIBLE DAMAGE TO ELECTRICAL COMPONENTS, ALWAYS TURN TBC-80 POWER OFF BEFORE REMOVING OR INSTALLING A PWA.

When connecting any instrument, such as a waveform monitor, vectorscope, or oscilloscope to a video output connector, ensure that the video signal is terminated using a 75Ω 1% precision resistor.

Insulated gate (MOS/CMOS) field-effect semiconductor devices are extremely susceptible to damage from static-charge buildup. Use care when handling to avoid possible static-charge damage to the device, especially when the humidity is 30% or less. Persons handling such devices should be grounded through a 1M resistor in series to ground. When replacing these devices, ensure that all leads of the device are shorted together (usually by the conductive material in which they are packed) until installed into the PWA.

All pulse width measurements are made at the 50% amplitude level. All rise and fall times are measured from the 10% to 90% amplitude levels. All scope probes used to view waveforms are 10:1 ratio probes. When making dual-trace measurements, the probe lengths should be equal.

4-11 Preliminary Requirements

Note

Unless otherwise noted, all measurements are made with the TBC-80 in EE and NORMAL mode.

STEP 1 Video Output and Video Input PWAs must be aligned before proceeding with alignment procedures for Tape Clock PWA.

STEP 2 Verify that input to ref input and tape input jacks conforms to RS170A input standards and DS1 on Video Output PWA is lighted.

STEP 3 Using differential input (A-B) on monitor oscilloscope, verify that position of monitor-out sync coincides with ref-in and that the sync-to-burst relation conforms to RS170A.

STEP 4 On Memory PWA, verify that horizontal position S3 switch is set to 8.

STEP 5 Verify that all front panel controls are set to unity gain.

4-12 System Test Level Adjustments

STEP 1 Monitor TP14 on Video Output PWA.

STEP 2 Adjust A/D clamp R213 on Video Input PWA, and identify inserted reference level by fact that it does not shift.

STEP 3 Adjust R213 until digitized back porch is same as reference level.

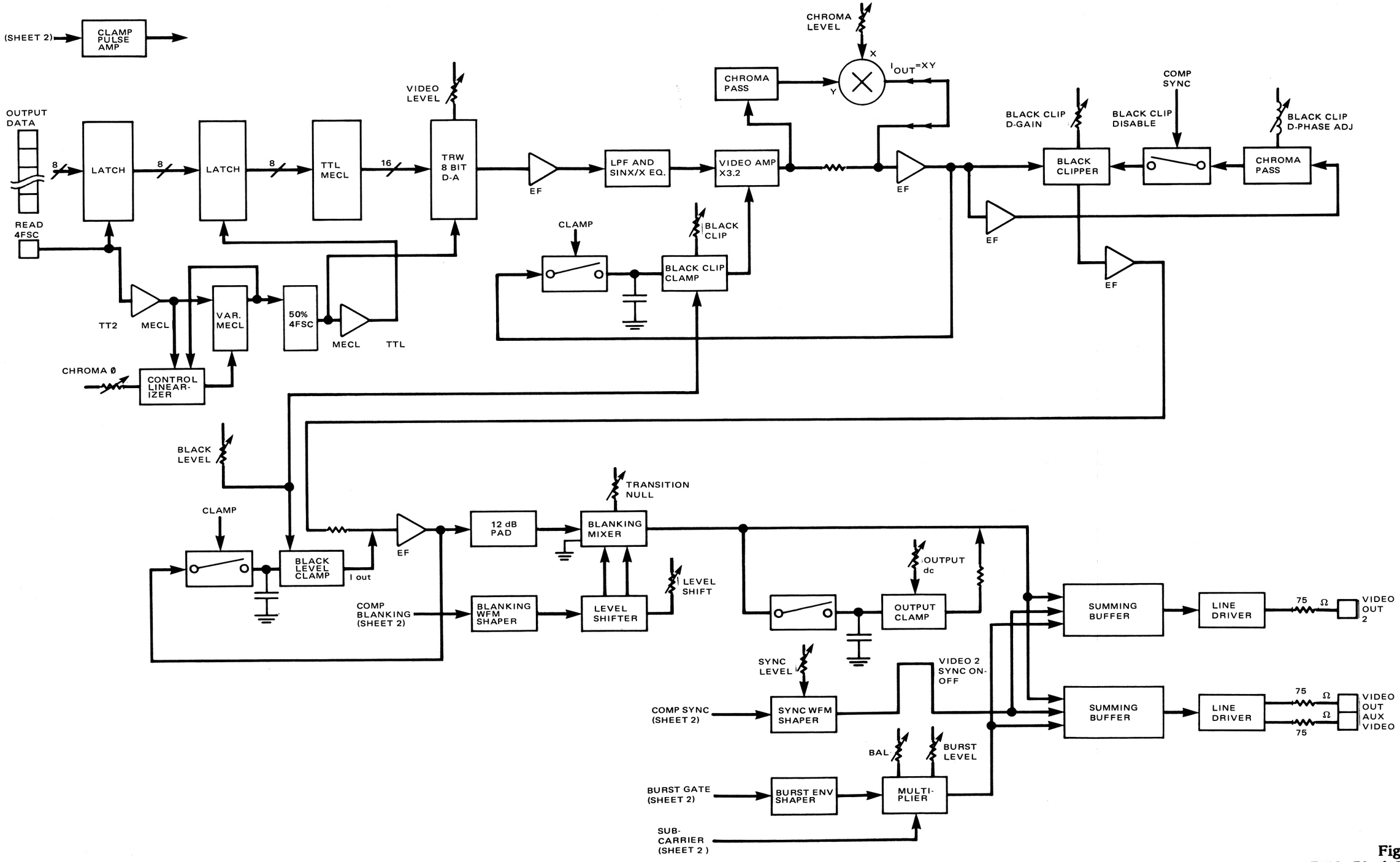


Figure 4-5.
TBC-80 Video Output PWA, Block Diagram (Sheet 1 of 2)

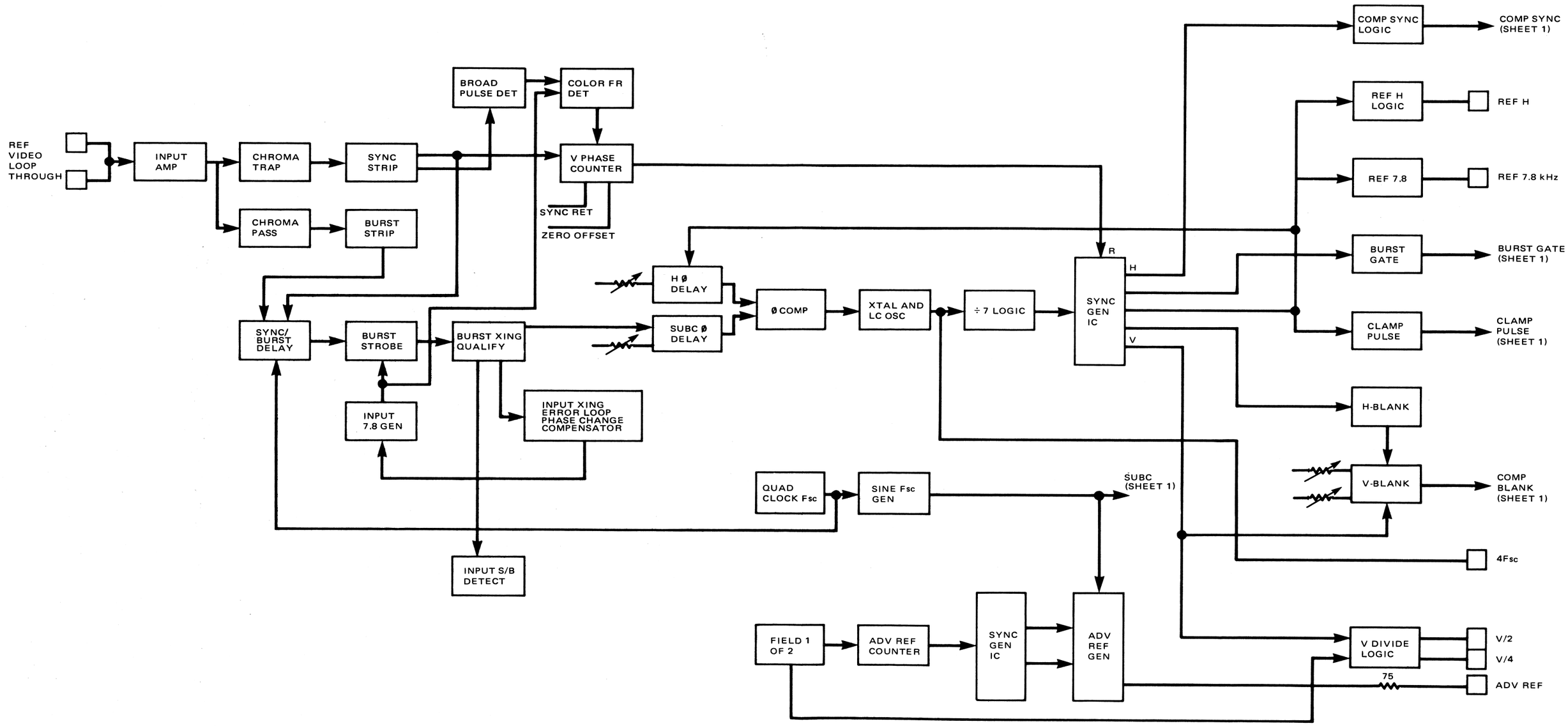


Figure 4-5.
TBC-80 Video Output PWA, Block Diagram
(Sheet 2 of 2)

STEP 4 Check output black level at this point and readjust video output R359 if necessary.

STEP 5 On video out, monitor the collector of Q25 and adjust R481 until pulse starts 0.2 µs after inserted reference level (as seen at TP10).

STEP 6 With reference video going through system, adjust S4 and R347 until burst-to-chroma phase is correct.

STEP 7 Using a waveform monitor on A-B, set system output phase with respect to reference as follows:

a. Set horizontal phase S3 to 8.

b. Adjust subcarrier phase R301 so that output and reference bursts cancel.

c. Set R428 so leading edges of sync line up exactly.

d. Using a spectrum analyzer, insert a swept frequency signal in VIDEO IN A, and monitor output at VIDEO OUT I.

e. Adjust L3 and L9 on video output board for maximum flatness.

4-13 Power Supply Alignments and Checks

Before proceeding with alignments, or if power supply problems are suspected, a check of the individual supply voltages can be made at the Motherboard PWA pins. The following list shows the dc voltages with their respective pin locations on the motherboard noted parenthetically. Also shown is the resistance of the analog A, digital D, and chassis E grounds to the individual voltage sources.

CAUTION

TO PREVENT POSSIBLE DAMAGE TO THE TEST EQUIPMENT OR UNIT, REMOVE PRIMARY POWER FROM THE UNIT BEFORE MEASURING RESISTANCE BETWEEN THE VARIOUS GROUNDS AND THE INDIVIDUAL VOLTAGES.

All voltage and resistance measurements should be made with a digital voltmeter and should indicate within 5% of the indicated values listed below.

Voltage	Res to A Gnd (Ω)	Res to D Gnd (Ω)	Res to E Gnd (Ω)
+12V (5-8)	275	1000	4000
-5V (87-88)	3500	4500	400
-12V (93-96)	200	900	4000
+5V (105-107)	10k	10k	6k
+5V (193-196)	1000	1500	5000

4-14 Selectable Jumper Options

Figures 4-6 through 4-9 show the locations of the jumper options on the individual PWAs. Tables 4-1 through 4-4 are lists of the individual jumpers and their recommended settings. If a problem is encountered during installation or after maintenance on any PWA, check the jumper selection on the individual assemblies. The jumper options should coincide with the normal settings of the jumper or a specific option as required by the particular system configuration.

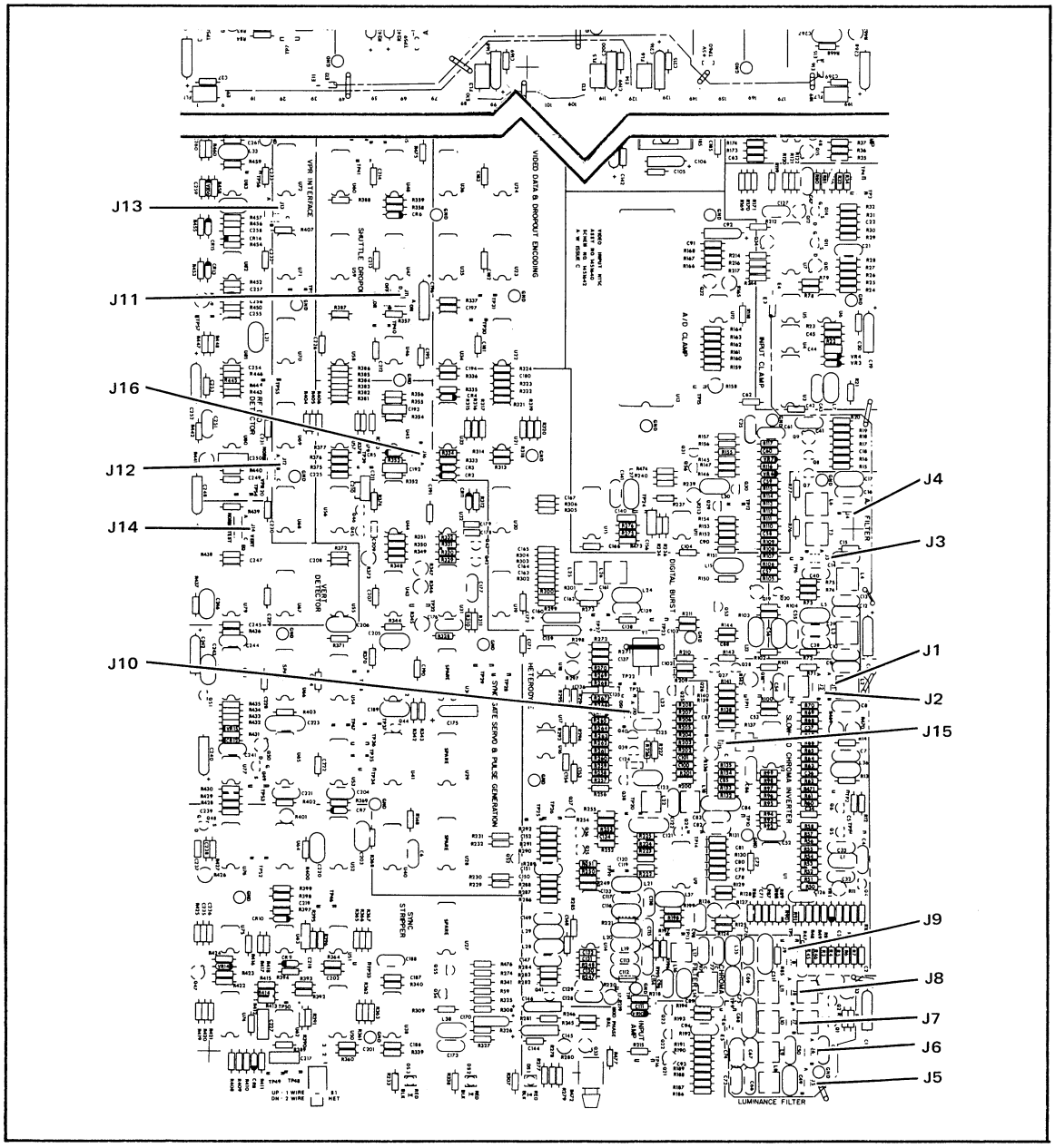


Figure 4-6. TBC-80 Video Input PWA, Jumper Locations

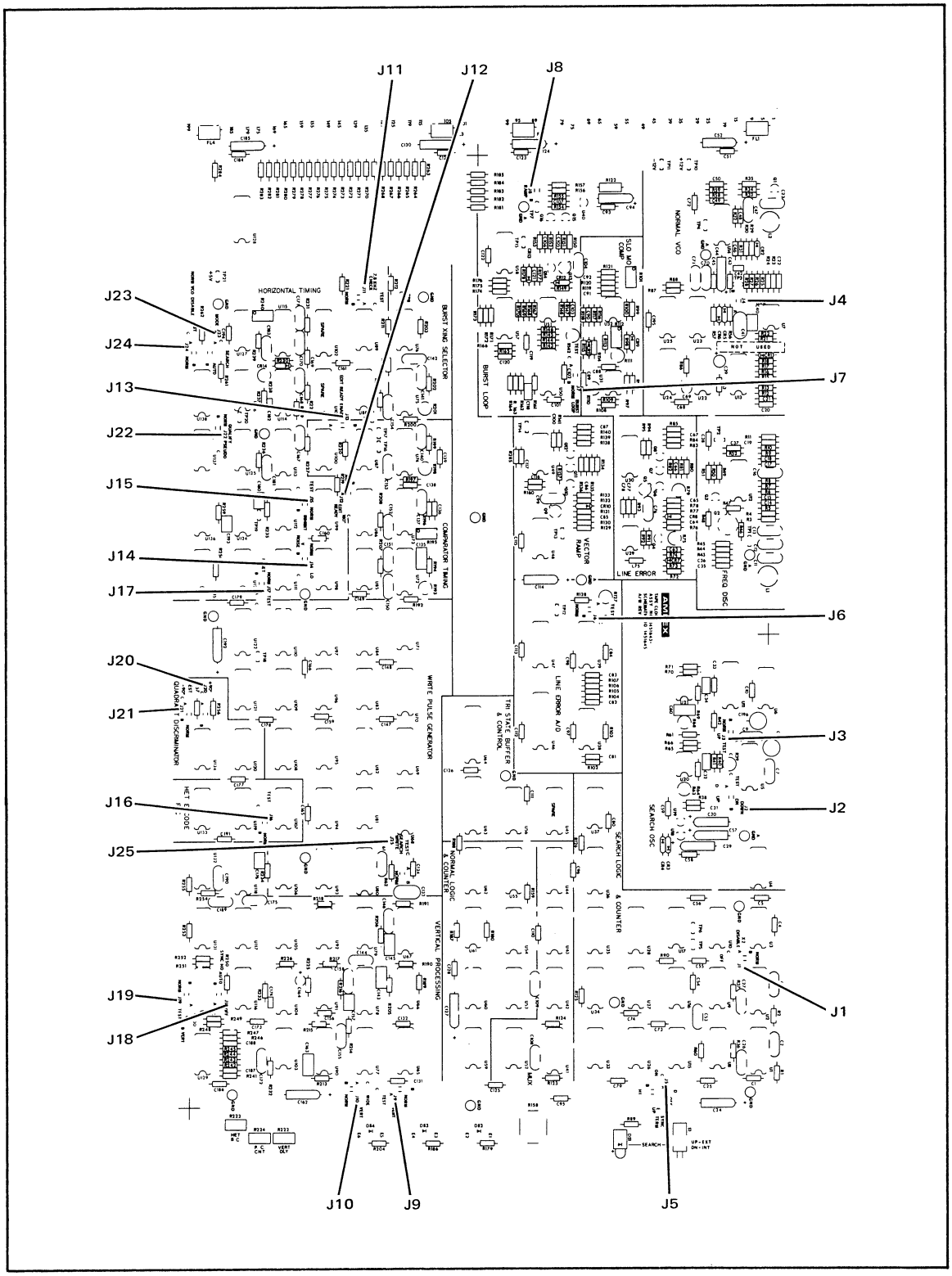


Figure 4-7. TBC-80 Tape Clock PWA, Jumper Locations

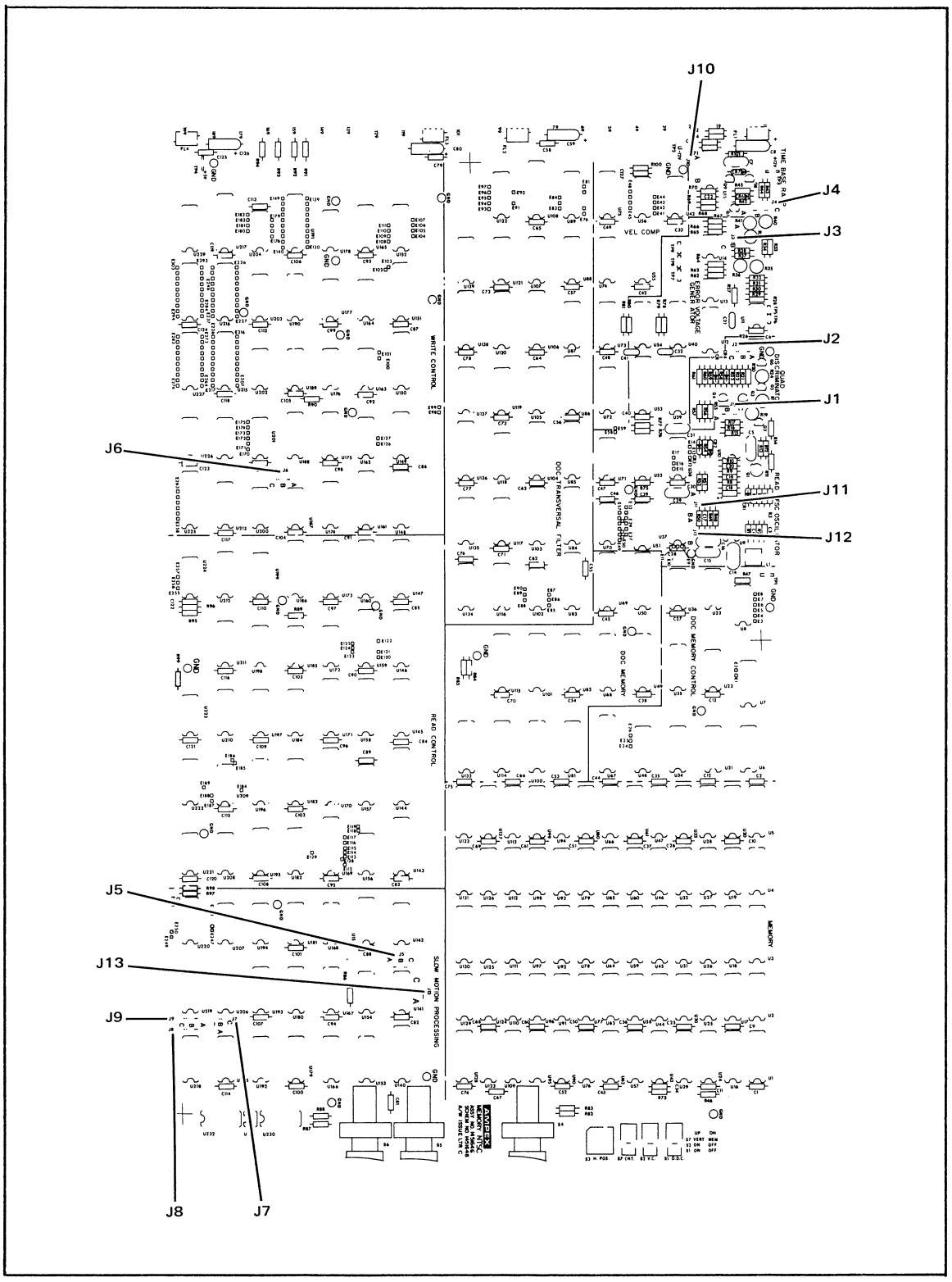


Figure 4-8. TBC-80 Memory PWA, Jumper Locations

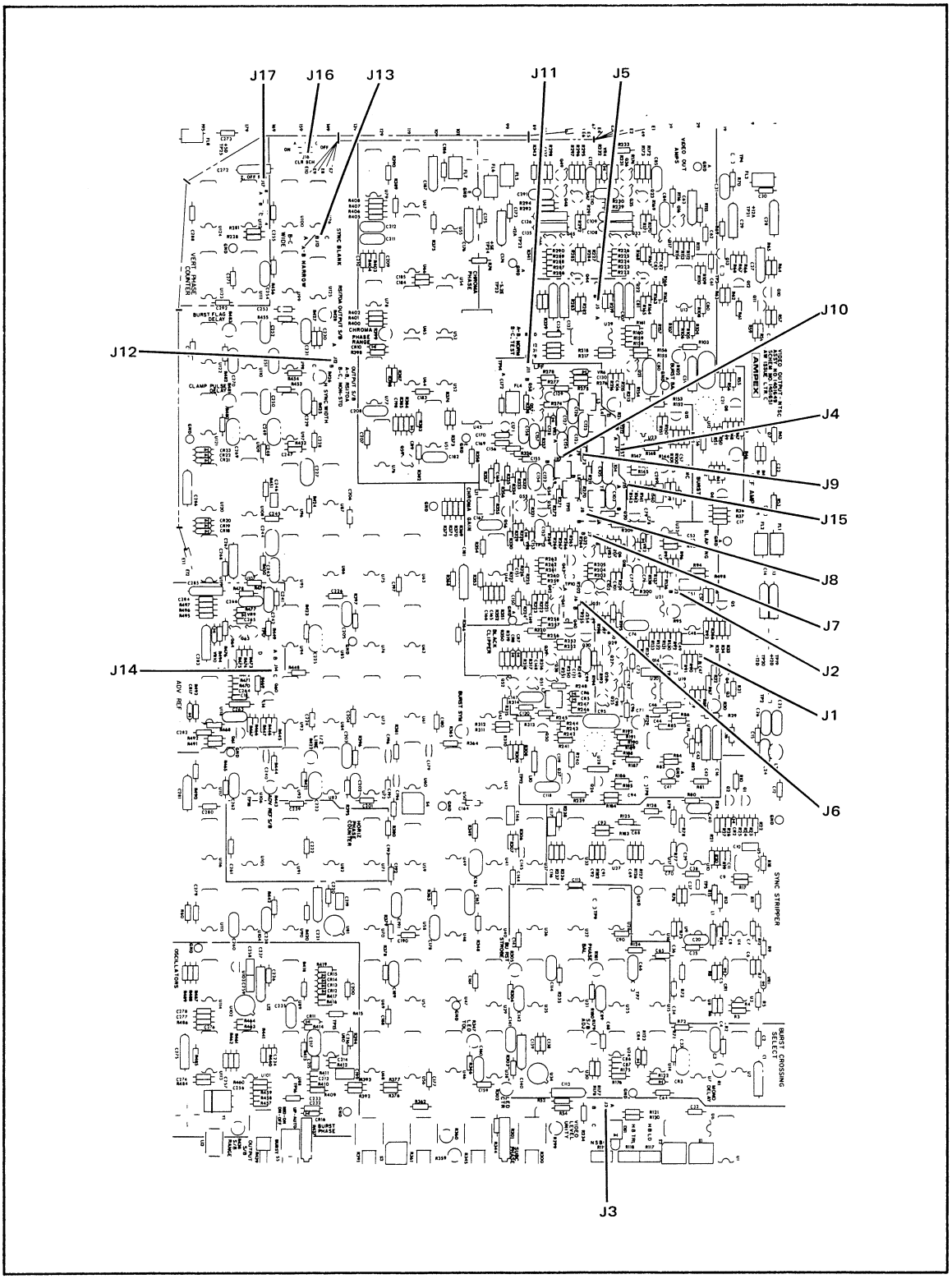


Figure 4-9. TBC-80 Video Output PWA, Jumper Locations

Table 4-1. Video Input PWA — Jumper Locations

Jumper	Position	Setting	Description
J1	A-B Out	Normal Test	Maintenance only.
J2	A-B Out	Test Normal	Maintenance only.
J3	A-B Out	Test Normal	Maintenance only.
J4	A-B Out	Normal Test	Maintenance only.
J5	A-B Out	Test Normal	Maintenance only.
J6	A-B Out	Test Normal	Maintenance only.
J7	A-B Out	Normal Test	Maintenance only.
J8	A-B Out	Normal Test	Maintenance only.
J9	A-B Out	Test Normal	Maintenance only.
J10	A-B Out	Test Normal	Maintenance only.
J11	A-B B-D B-C	Normal Option Option	 Search dropout disable. Fast search dropout disable.
J12	A-B B-C	Normal Option	 VPR-20 RF dropout.
J13	A-B B-C	Normal Option	 Heterodyne encode 180°.
J14	A-B B-C	Normal Option	 Broadpulse tape vertical.
J15	A-B A-C	Normal Test	Maintenance only.
J16	A-B Out	Normal Test	Maintenance only.

Table 4-2. Tape Clock PWA — Jumper Locations

Jumper	Position	Setting	Description
J1	A-B B-C	Normal Test	Maintenance only.
J2	A-B A-C	Normal Test	Maintenance only.
J3	A-B A-C	Normal Test	Maintenance only.
J4	A-B A-C	Normal Test	Maintenance only.
J5	A-B A-C A-D A-E	Normal Test Test Test	Maintenance only.
J6	A-B A-C	Normal Test	Maintenance only.
J7	A-B A-C	Normal Test	Maintenance only.
J8	A-B Out	Normal Test	Maintenance only.
J9	A-B A-C	Normal Test	Maintenance only.
J10	A-B A-C	Normal Option	Non-standard vertical transitions — noise in picture.
J11	A-B A-C	Normal Test	Maintenance only.
J12	A-B A-C	Normal Option	180° edit frame timing.
J13	A-B Out	Normal Test	Maintenance only.
J14	A-B A-C	Normal Test	Maintenance only.

(Continued next page)

Table 4-2. Tape Clock PWA — Jumper Locations (Continued)

Jumper	Position	Setting	Description
J15	A-B A-C	Normal Test	Maintenance only.
J16	A-B A-C	Normal Test	Maintenance only.
J17	A-B A-C	Normal Test	Maintenance only.
J18	A-B A-C	Normal Option	Non-sync head VTR.
J19	A-B A-C	Normal Test	Maintenance only.
J20	A-B A-C	Normal Test	Maintenance only.
J21	A-B A-C	Normal Test	Maintenance only.
J22	A-B A-C	Normal Test	Maintenance only.
J23	A-B A-C A-D	Normal Test Test	Maintenance only.
J24	A-B A-C	Normal Test	Maintenance only.

Table 4-3. Memory PWA — Jumper Locations

Jumper	Position	Setting	Description
J1	A-B B-C	Normal Test	Read 4Fsc oscillator frequency at pins 113/114, adjust L1 for 14.3 MHz. (TTL levels).
J2	B-C A-B	Normal Test	Disable ±90° velcomp current sources.
J3	A-B B-C	Normal Test	Disables velocity compensation.

(Continued next page)

Table 4-3. Memory PWA — Jumper Locations (Continued)

Jumper	Position	Setting	Description
J4	A-B B-C	Normal Test	Disables time base error. Allows range test on time-base ramp (R40, -270°).
J5	A-B B-C	Normal Test	Disables slow motion processing.
J6	A-B B-C	Normal Test	Disables write phase A, allow testing of write phase B.
J7	A-B B-C	Normal Soft	Selects overload mode. Soft overload is accomplished at the expense of a 2-line reduction in the window.
J8	A-B B-C	Normal Test	Disables RW(+) - rewrite process.
J9	A-B B-C	Normal Test	Disables DW(+) - dual-write process.
J10	A-B B-C		Centering - Vertical. Centering - Memory.
J11	A-B None	Normal Test	Read 4Fsc oscillator feedback enabled.
J12	A-B None	Normal Test	Read 4Fsc oscillator output enabled.

Table 4-4. Video Output PWA — Jumper Locations

Jumper	Position	Setting	Description
J1	A-B B-C	Normal Test	Maintenance only.
J2	A-B B-C	Normal Test	Maintenance only.
J3	A-B B-C	Normal Option	Input reference non-standard RS170A.
J4	A-B Out	Test Normal	Maintenance only.

(Continued next page)

Table 4-4. Video Output PWA — Jumper Locations (Continued)

Jumper	Position	Setting	Description
J5	A-B B-C	Normal Option	Non-sync video 2 output.
J6	A-B B-C	Normal Test	Maintenance only.
J7	A-B Out	Normal Test	Maintenance only.
J8	A-B B-C	Normal Test	Maintenance only.
J9	A-B Out	Normal Test	Maintenance only.
J10	A-B Out	Normal Test	Maintenance only.
J11	A-B B-C	Normal Test	Maintenance only.
J12	A-B B-C	Normal Option	Non-standard RS170A sync/burst.
J13	A-B A-C	Normal Option	Wide vertical blanking.
J14	A-B B-C B-D	Option Option Option	Advance reference -8V composite sync. Advance reference .3V composite sync. Advance reference -8V vertical.
J15	A-B Out	Test Normal	Maintenance only.
J16	A-B B-C	Normal Option	Monochrome search.
J17	A-B B-C	Normal Test	Maintenance only.
J18	A-B Out	Test Normal	Maintenance only.

4-15 TBC-80 Motherboard PWA

Table 4-5 is a list of TBC-80 Motherboard PWA signals and their descriptions.

Table 4-5. TBC-80 Motherboard, Signal Pinouts

Pin	Signal	Source	
1	Analog Ground	Power Supply	
2	↕	↕	
3			
4	Analog Ground		
5	+12 Vdc		
6	↕		
7			
8	+12 Vdc		
9	Analog Ground		
10	↕		
11			
12	Analog Ground	Power Supply	
13	Ref Video In-	J2 & J3 Ref Video	
14	Ref Video In-	↕	
15	Video Ground		
16	Video Ground	J2 & J3 Ref Video	
17	Burst ↑	Video Input	
18	Burst ↓	Video Input	
19	Analog Ground	Video Output	
20	Analog Ground	↕	
21	Aux Video		
22	Aux Video	Video Output	
23	Video Ground	J5 Tape Video in B	
24	Video Ground	↕	
25	Tape Video In		
26	Tape Video In	J5 Tape Video in B	
27	Analog Ground	Power Supply	
28	Analog Ground	Power Supply	
29	Video Ground	J4 Tape Video in A	
30	Video Ground	↕	
31	Tape Video In		
32	Tape Video In	J4 Tape Video in A	
33	Analog Ground	Power Supply	
34	Analog Ground	Power Supply	
35	Sync Coh. Subc. Out	Video Input	(to J7 Sync Coherent Subc Out)
36	Sync Coh. Subc. Out	↕	
37	Analog Ground		
38	Analog Ground	Video Input	
39	RF In	J6 RF In	
40	RF In	J6 RF In	

(Continued next page)

Table 4-5. TBC-80 Motherboard, Signal Pinouts (Continued)

Pin	Signal	Source	
41	RF Ground		
42	RF Ground	J6 RF In	
43	Analog Ground	Power Supply	
44	Analog Ground	Power Supply	
45	Step Forward 2	J1-32	(VTR)
46	Step Forward 1	J1-31	
47	Sync HD Proc.	J1-30	
48	Up/Down	J1-12	
49	Analog Ground	J1-1, 2, 3, 7, 8, 10, 11, 14-19	
50			
51			
52			
53			
54	Analog Ground	J1-1, 2, 3, 7, 8, 10, 11, 14-19	
55	2H Gate	J1-28	
56	Dropout Pulse	J1-29	
57	Slow Motion	J1-27	
58	Zero Offset	J1-9	
59	HD Sw./Vertical Dropout	J1-25	
60	P/B Vertical	J1-26	
61	Tachometer	J1-24	
62	Fast Shuttle	J1-6	
63	Sync Retard	J1-23	
64	Edit Mute	J1-5	
65	Step Back 1	J1-20	
66	Step Back 2	J1-21	(VTR)
67	Analog Ground	Video Output	
68	Analog Ground		(to J9 Adv Rev)
69	Advance Sync Out		
70	Advance Sync Out	Video Output	
71	Video Ground	Video Input	
72	Video Ground		(to J8 Monitor Video)
73	Monitor Video Out		
74	Monitor Video Out	Video Input	
75	Analog Ground	Power Supply	
76	Analog Ground	Power Supply	
77	Video Output II	Video Output	
78	Video Output II		(to J11 Video Out II)
79	Video Ground	Video Output	

(Continued next page)

Table 4-5. TBC-80 Motherboard, Signal Pinouts (Continued)

Pin	Signal	Source
80	Video Ground	Video Output
81	Video Output I	↕
82	Video Output I	(to J10 Video Out I)
83	Video Ground	↕
84	Video Ground	Video Output
85	Analog Ground	Power Supply
86	Analog Ground	↕
87	-5 Vdc	↕
88	-5 Vdc	↕
89	Analog Ground	↕
90	↕	↕
91	↕	↕
92	Analog Ground	↕
93	-12 Vdc	↕
94	↕	↕
95	↕	↕
96	-12 Vdc	↕
97	Analog Ground	↕
98	↕	↕
99	↕	↕
100	Analog Ground	↕
101	Digital ground	↕
102	↕	↕
103	↕	↕
104	Digital Ground	↕
105	+5 Vdc	↕
106	↕	↕
107	↕	↕
108	+5 Vdc	↕
109	Digital Ground	↕
110	↕	↕
111	↕	↕
112	Digital Ground	Power Supply
113	Read 4Fsc	Memory
114	Read 4Fsc	↕
115	DO8	↕
116	DO7	↕
117	DO6	↕
118	DO5	↕
119	DO4	↕
120	DO3	↕
121	DO2	↕
122	DO1	Memory
123	Digital Ground	Power Supply

(Continued next page)

Table 4-5. TBC-80 Motherboard, Signal Pinouts (Continued)

Pin	Signal	Source
124	Digital Ground	Power Supply
125	Reference 4Fsc	Video Output
126	Reference 4Fsc	↕
127	Reference H (-)	↕
128	Reference 7.8 kHz (H/2)	↕
129	Reference V (+)	↕
130	Reference V/2	↕
131	Reference V/4	↕
132	Reference Comp. Sync (-)	Video Output
133	Ref 3.9 kHz (H/4)	not used in NTSC
134	Read Pulse	not used in NTSC
135	Sync Terminate (-)	Video Input
136	Wide (-)	Video Input
137	Normal (+)/Heterodyne (-)	Memory
138	Normal (+)/Bypass (-)	↕
139	Video Input Switch	↕
140	DOC Off (-)	Memory
141	Color Present (+)	Video Input
142	VCO Lock (-)	Tape Clock
143	Search (-)	Tape Clock
144	VCO Up (-)/Down (+)	Video Input
145	Video Mute (-)	Video Input
146	Gen Lock (-)	Video Output
147	Color Shuttle Limit (-)	Video Input
148	Digital Burst	↕
149	No Connection	↕
150	No Connection	↕
151	No Connection	↕
152	No Connection	↕
153	No Connection	↕
154	No Connection	↕
155	Digital Ground	Power Supply
156	Decode Fsc	not used in NTSC
157	Gated DO (-)	Tape Clock
158	Vertical Inhibit (-)	↕
159	VCO Vertical	Tape Clock
160	F/2	Memory
161	Tape V/2	not used in NTSC
162	Tape Vertical	Video Input
163	Burst Present (-)	↕
164	Tape H (-)	Video Input
165	Heterodyne 7.8 kHz	not used in NTSC
166	Write 7.8 kHz	Memory
167	Write 3.9 kHz	not used in NTSC

(Continued next page)

Table 4-5. TBC-80 Motherboard, Signal Pinouts (Continued)

Pin	Signal	Source
168	1/2 Line (-)	Tape Clock
169	Clamp Pulse (-)	↕
170	Flywheel Sync (-)	Tape Clock
171	Gated Sync	Video Input
172	Vel Comp Write (-)	Memory
173	VCO Write Timing (-)	Tape Clock
174	Write Pulse (-)	↕
175	Encode Fsc	
176	Encode Fsc	Tape Clock
177	Digital Ground	Power Supply
178	Digital Ground	Power Supply
179	DI8	Video Input + Tape Clock
180	D17	↕ (Pull up) ↕
181	D16	on
182	DI5	Memory Board)
183	DI4	
184	DI3	
185	DI2	
186	DI1	Video Input + Tape Clock
187	Tape 4Fsc	Tape Clock
188	Tape 4Fsc	Tape Clock
189	Digital Ground	Power Supply
190	↕	↕
191		
192	Digital Ground	
193	+5 Vdc	
194	↕	
195		
196	+5 Vdc	
197	Digital Ground	
198	↕	
199		
200	Digital Ground	Power Supply

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